Role of tuning techniques in advancing the performance of negative capacitance field effecting based full adder

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ABSTRACT

The increasing demand for faster, robust, and efficient device development of enabling technology to mass production of industrial research in circuit design deals with challenges like size, efficiency, power, and scalability. This paper, presents a design and analysis of low power high speed full adder using negative capacitance field effecting transistors. A comprehensive study is performed with adiabatic logic and reversible logic. The performance of full adder is studied with metal oxide field effect transistor (MOSFET) and negative capacitance field effecting (NCFET). The NCFET based full adder offers a low power and high speed compared with conventional MOSFET. The complete design and analysis are performed using cadence virtuoso. The adiabatic logic offering low delay of 0.023 ns and reversible logic is offering low power of 7.19 mw.

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1. INTRODUCTION

The modern embedded systems and signal processing processors demand low power and high speed full adder [1]. Many researchers have developed versions of complete adders using XOR/XNOR gates and complementary metal-oxide semiconductor (CMOS) inverters [2]. The transistor technology and logic utilised to create the complete adder will decide the performance [3]. Transistor scaling is vital to building low-power integrated circuit (IC). Transistors technologies as high-electron-mobility transistor (HEMT), heterojunction bipolar transistor (HBT), metal oxide semiconductor field effect transistor (MOSFET), and negative capacitance field effect transistor (NCFET) [4], [5] facilitate scaling to lower levels [6]. Other than typical full adder design techniques (using XOR/XNOR (or) CMOS inverters), there are some popular digital logics accessible, i.e., efficient charge recovery logic (ECRL), adiabatic logic, dual rail circuits (DRC), and reversible logic [7], [8]. In this paper, we give an examination of the design of a full adder using several transistor technologies and different forms of logic to boost the ability in the elements of delay and power. When compared with the typical XOR operations of full adder cells, adiabatic logic [9], [10] and reversible logic-

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based full adder cells offer outstanding performance. This paper is organized as follows. Section 2 presents the related work. In section 3, problem statement and the proposed method is described. In section 4, design and analysis is presented. In section 5, described results and analysis. Finally, the main conclusion and future directions are parented in section 6.

2. RELATED WORK

Consumer electronics and medical devices use ultra-low-power circuitry. Low-power technology powers CMOS scaling. Digital signal processing uses complex techniques like convolution, which requires efficient arithmetic circuits. As arithmetic circuits become more complicated, power consumption becomes more critical. This complicates arithmetic circuits, making energy usage more important. Cell phones, PDAs, and laptops are in high demand because arithmetic circuits use a low-power full adder [11]. Table 1 show that the ECRL, DRC, secured quasi-adiabatic logic (SQAL), and one-dimensional capacitor (ODC) have been proposed and studied to understand future energy-efficient high-end computing systems.

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Transistor technology</th>
<th>Logic</th>
<th>Number of transistors</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[12]</td>
<td>MOSFET</td>
<td>Hybrid CMOS</td>
<td>10/10</td>
<td>This research suggests triplet design to improve transmission gate (TG) and hybrid CMOS full adder designs in chain and tree topologies. TG and hybrid CMOS full adder can employ this approach.</td>
</tr>
<tr>
<td>[13]</td>
<td>Quantum-dot cellular automata (QCA)</td>
<td>--/--/--</td>
<td>--</td>
<td>Digital logic and arithmetic use the full adder circuit. This study examines QCA-enhanced full adder. This full adder features fewer cells and a shorter latency.</td>
</tr>
<tr>
<td>[14]</td>
<td>MOSFET</td>
<td>Gate diffusion input (GDI)</td>
<td>8/8</td>
<td>Addition is the foundation of arithmetic. This work builds three low-power full adders with full-swing AND, OR, and XOR gates to overcome GDI logic’s threshold voltage problem.</td>
</tr>
<tr>
<td>[15]</td>
<td>MOSFET</td>
<td>MOS current-mode logic</td>
<td>7/7</td>
<td>This work presents a reversible logic full adder for MOS current mode logic (MCML) circuits. Six-input logic gates power the conventional MCML full adder.</td>
</tr>
<tr>
<td>[16]</td>
<td>HEMT</td>
<td>Reversible logic-XOR-MUX-</td>
<td>12/12</td>
<td>Reversible circuits cannot fan-out, but extra gates can. Feynman, TSG, and Peres gates are explained here.</td>
</tr>
<tr>
<td>[17]</td>
<td>MOSFET-</td>
<td>Adiabatic logic-</td>
<td>24/24</td>
<td>Digital technology, especially signal processing, has advanced significantly. Software-defined radio devices must be compact, low power, high-performing, and fast. “Adiabatic” thermodynamic processes do not exchange energy with the outside world; hence no power or energy is lost. This logic decreases power dissipation when switching. It recycles energy from the load capacitance for the following action.</td>
</tr>
<tr>
<td>[18]</td>
<td>Fin field-effect transistor (FinFET)</td>
<td>CMOS-36</td>
<td>11/11</td>
<td>Many computational circuits use full adders. This study uses graphene-dielectric-metal waveguide tuning to create a compact, efficient electro-optical full adder.</td>
</tr>
</tbody>
</table>

Table 1. Full adder design state of art

In arithmetic, addition is a fundamental operation, addition-based operations like subtraction, and multiplication. The full adder is an essential module of the binary adder. Improving the performance of 1-bit full-adder is a top priority that has drawn a lot of research resources [20], [21]. Full adder develops high-performance, low-power systems. Scientists have long prioritised full adder MOSFET threshold voltage.

\[ V_{th} = V_{to} + \gamma (\sqrt{2}\phi_F) + |V_{sb}| - \sqrt{2}\phi_F \]  

Table 2 shows that channel length (L), channel width (W), and gate and drain voltage MOSFET characteristics determine drain current.

Table 2. MOSFET properties

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
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<tbody>
<tr>
<td>Gate width</td>
<td>120 nm</td>
</tr>
<tr>
<td>Gate length</td>
<td>45 nm</td>
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<tr>
<td>Supply voltage</td>
<td>1 V</td>
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<tr>
<td>Threshold voltage</td>
<td>0.7 V</td>
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</tbody>
</table>

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The Boltzmann tyranny limits typical MOSFET subthreshold swing to 60 mV/decade at normal temperature, making it difficult to lower supply voltage and power usage [22]. NCFETs may benefit from future IC nodes [23]. Because of its integrated ferroelectric layer in the gate stacks, an NCFET has a larger switching current ratio [24]–[26] and a steeper subthreshold swing than a MOSFET. In devices and circuits, it improves performance while using less power. The ferroelectric material’s non-stable NCE requires careful CFE-to-underlying MOSFET capacitance matching for NCFET performance [27].

NCFET transistors use a ferroelectric (FE) layer in the transistor gate stack to function at lower VDDs while retaining switching speed [28], [29]. The NCFET’s threshold voltage, drain current, and device parameters are provided in (3), (4), and Table 3.

\[
I_D = \frac{W}{L} \mu_{n,eff} C_{ox} \left[ (V_{GS} - V_T)V_{DS} - \frac{1}{2} V_{DS}^2 \right] 
\]  

\[
V_F = \rho \frac{dQ_F}{dt} + (\alpha Q_F + \beta Q_F^3) 
\]  

The drain current of the NCFET is:

\[
I_D = W Q_i(x_o) V_{ox} F_{sat} 
\]

### Table 3. NCFET properties

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
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<tr>
<td>Gate width</td>
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<tr>
<td>Threshold voltage</td>
<td>0.7 V</td>
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### 3. PROBLEM STATEMENT AND DESIGN METHOD

Portable battery-operated systems are moving towards better speeds, smaller on-chip regions, and lower power consumption [30]–[33]. Convolution, correlation, filtering, and other efficient arithmetic operations are used in modern microprocessors and digital signal processor (DSP). These operations depend on full adders. Power consumption can be reduced by reducing arithmetic operation energy. Low supply voltage and low-frequency input pulses delay and degrade an arithmetic system’s circuits, reducing power consumption. Static and dynamic logic design CMOS full adder cells. Static full adder cells are simpler to develop, more dependable, and consume less power. Several logic topologies created full adder cells. Some topologies perform better than others. Table 4 describes recent real issues. Developing such systems requires full adder cell design with low power consumption and fast speed. Figure 1 illustrates the problem statement using a flowchart.

### Table 4. Problem statement

<table>
<thead>
<tr>
<th>Research challenge</th>
<th>Description</th>
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<tbody>
<tr>
<td>Low power</td>
<td>The selection of optimal transistor technology and reduction of leakage currents helps to reduce the circuit power supply.</td>
</tr>
<tr>
<td>High speed</td>
<td>The selection of design logic helps to achieve the design of high speed full adder.</td>
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Role of tuning techniques in advancing the performance of negative capacitance field … (Ravuri Daniel)
4. DESIGN AND ANALYSIS

4.1. Adiabatic logic

Adiabatic logic controls current flow and reduces energy loss from switching and the capacitor. It's done by recycling circuit energy. This approach recycles energy and slows charge transmission. Vds (nMOS or pMOS) are hard to zero, wasting energy during recovery. Adiabatic circuits enhance silicon area Figure 2. Thus, energy-efficient operation has grown popular. Adiabatic circuits have dissipated less energy than CMOS circuits for over two decades. The inability to consistently construct the power clock in Figure 3 has slowed energy-efficient adiabatic systems' progress. MOSFET and Table 5 function adiabatic logic-based complete adder. Figures 4 and 5 illustrate the NCFET-based adiabatic logic-based complete adder's design and transient response.

![Figure 2. Adiabatic logic based full adder using MOSFET](image)

![Figure 3. Adiabatic logic based full adder using MOSFET transient response](image)

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>C</th>
<th>1</th>
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<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
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</table>
4.2. Reversible logic

The proposed reversible logic based full adder using MOSFET as shown in Figure 6. In this circuit, there are three inputs (A, B, and Cin) representing the two binary numbers to be added and the carry input, and two outputs (Sum and Cout) representing the sum and carry-out of the addition. A reversible full adder using NCFETs as shown in Figure 7 can be implemented using a combination of reversible gates, such as the Toffoli gate or Fredkin gate. These gates can be constructed using NCFETs, but the actual circuit design and fabrication would require specialized expertise and tools. Figure 8 shows transient response of a NCFET refers to how the transistor behaves during the time it takes to transition from one state to another in response to a change in its input or initial conditions.

Figure 4. Adiabatic logic based full adder using NCFET

Figure 5. Adiabatic logic based full adder using NCFET transient response

Figure 6. Full adder using reversible logic by MOSFET
5. RESULTS AND DISCUSSION

In order to design and analyses the simulation of the described full adder circuits, the CADANCE software was used. A MOSFET and an NCFET are used to evaluate the overall adder's performance. MOSFET and NCFET model files used for simulation and design NCFETs perform well in delay and power compared to conventional MOSFETs, as shown in Tables 6 and 7. Respectively of the comprehensive study on adiabatic and reversible logic using 45 nm technology by both MOSFET- and NCFET-based full adder.

<table>
<thead>
<tr>
<th>Table 6. Comprehensive study on adiabatic and reversible logic</th>
</tr>
</thead>
<tbody>
<tr>
<td>Logic</td>
</tr>
<tr>
<td>Transistor technology</td>
</tr>
<tr>
<td>Threshold voltage</td>
</tr>
<tr>
<td>Supply voltage</td>
</tr>
<tr>
<td>No. of transistor</td>
</tr>
<tr>
<td>Power dissipation</td>
</tr>
<tr>
<td>Delay</td>
</tr>
</tbody>
</table>
Table 7. Work comparison with literature

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Mamaghani et al. [32]</th>
<th>Pan and Naeemi [33]</th>
<th>Proposed method</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transistor technology</td>
<td>FinFET</td>
<td>Tunneling FET</td>
<td>NCFET</td>
</tr>
<tr>
<td>Gate length</td>
<td>27 nm</td>
<td>45 nm</td>
<td>45 nm</td>
</tr>
<tr>
<td>Supply voltage</td>
<td>1.75 V</td>
<td>2.5 V</td>
<td>1 V</td>
</tr>
<tr>
<td>Threshold voltage</td>
<td>0.7</td>
<td>0.7</td>
<td>0.7</td>
</tr>
<tr>
<td>Logic</td>
<td>Magnetic</td>
<td>CoMÉT</td>
<td>Adiabatic logic</td>
</tr>
<tr>
<td>No. of transistors</td>
<td>28</td>
<td>21</td>
<td>8</td>
</tr>
<tr>
<td>Power dissipation</td>
<td>746 mw</td>
<td>889.3 mw</td>
<td>552 mw</td>
</tr>
<tr>
<td>Delay</td>
<td>8 ns</td>
<td>54 ns</td>
<td>0.023 ns</td>
</tr>
</tbody>
</table>

Figure 9 shows the power consumption of the proposed logic 1 (552 mW) and logic 2 (7.19 mW) are stands out as the most energy-efficient among existing methods. Figure 10 shows delay of the logic 1 (1.68 ns) and logic 2 (0.023 ns) are exceptionally low delay than the existing methods. The primary takeaways from the performance analysis are that the adiabatic logic-based full adder has a fast processing speed, whereas the reversible logic-based full adder has low overall power consumption.

6. CONCLUSION

NCFETs outperform MOSFETs. Reversible and adiabatic logic evaluated NCFET based complete adder performance. The performance investigation found that the adiabatic logic-based full adder is fast and the reversible logic-based one is low-power. Low-power, high-speed embedded system IC design prefers the given full adder. The choice of NCFET-based full adder, one designed using adiabatic logic and the other using reversible logic, appears to be well-suited for the needs of low-power, high-speed embedded system ICs. NCFET technology's novelty presents fabrication problems that must be overcome to seamlessly incorporate it into semiconductor processes, requiring further research for scalability and cost-effectiveness. Adiabatic and reversible logic architectures have larger circuit sizes than CMOS-based designs, which may limit space-constrained applications. These constraints highlight the need for continual research and innovation to overcome them and maximize NCFET technology's potential.
NCFET-based full adder designs have several promising futures. First, more reliable and cost-effective fabrication methods are essential to this technology’s applicability for mass production. Hybrid logic architectures that combine adiabatic and reversible logic may balance power efficiency and speed, reducing area overhead. To ensure performance under varied environmental circumstances, research should also improve temperature resilience. Integration of NCFET-based designs with legacy systems should also be a priority to ease the transition. Finally, customizing complete adder designs for low-power, high-speed embedded system applications can improve performance and energy efficiency. These future efforts aim to maximize NCFET-based designs’ practical uses.

REFERENCES

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