

Design and Analysis of CMOS and Adiabatic 1:16 Multiplexer and 16:1 Demultiplexer

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ABSTRACT

Conventional CMOS is compared with two adiabatic logic styles namely Efficient Charge Recovery Logic (ECRL) and Improved Efficient Charge Recovery Logic (IECRL). A 16:1 multiplexer and 1:16 demultiplexer using these design techniques are designed and results are compared based on their minimum/maximum power consumption and transistor count. The proposed schematics multiplexer and demultiplexer are simulated using Microwind2 and DSCH2 software.

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1. INTRODUCTION

During recent years the main and highly concerned issue in the low power VLSI design is energy/power dissipation. This is due to the increasing demand of portable systems and the need to limit the power consumption in VLSI chips. In conventional CMOS circuits, the basic approaches used for reducing power consumption are by reducing the supply voltages, on decreasing node capacitances and minimize the switching activities with efficient charge recovery logic. The adiabatic logic works on the principle of energy recovery logic and provides a way to reuse the energy stored in load capacitors rather than the conventional way of discharging the load capacitors to the ground and wasting this energy. The Power consumption is the major concern in low power VLSI design technology. The need for low power devices has been increasing rapidly due to the battery operated and portable devices. In this paper two circuits techniques ECRL, IECRL are analyzed using multiplexer and demultiplexer circuits.

2. MOTIVATION

2.1. Need for Low Power Design

The requirement for low power design has caused a large paradigm shift where energy dissipation has become as essential consideration as area and performance. Several factors have contributed to this trend. The need for low power devices has been increasing very quickly due to the portable devices such as laptops, mobile phones and battery operated devices such as calculator, wrist watches. These products always put a large attention on minimizing power in order to maximize their battery life. Another motive for low power is associated to the high end products. This is due to the packaging and cooling of such high performance, high

density and high power chips are prohibitively expensive.

Another consideration low power design is related to the environment. The Micro electronics products become tolerable usage in everyday's life, their need on energy will sharply increase. Therefore the reduction in power consumption reduces the heat generated and so reduces the cost required for extra cooling systems in homes and office.

2.1. Multiplexer

A multiplexer is a device which selects one of many input signals and forwards the selected input to the output. Multiplexer pin diagram is shown in figure 1. Multiplexers are mainly used connect many sources or devices with single destination or device. A Multiplexer is also known as data selector.

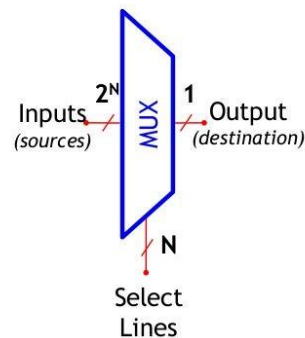


Figure 1. Block Diagram of Multiplexer

2.3. Demultiplexer

A demultiplexer is a device which has single input and many outputs. Demultiplexer is used to connect a single source to multiple destinations. Figure 2 shows the pin diagram of demultiplexer. The multiplexer and demultiplexer work together to perform the process of transmission and reception of data in communication system. It performs the reverse operation of multiplexer. Both play an important role in communication systems.

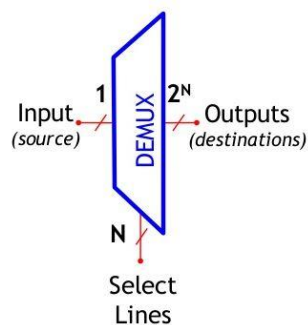


Figure 2. Block Diagram of Demultiplexer

2.4. Conventional CMOS

Conventional CMOS designs consume a lot of energy during switching process. Two major sources of power dissipation in digital CMOS circuits are dynamic power and static power. Dynamic power is related to the changing events of logic states or circuit switching activities including power dissipation due to capacitance charging and discharging.

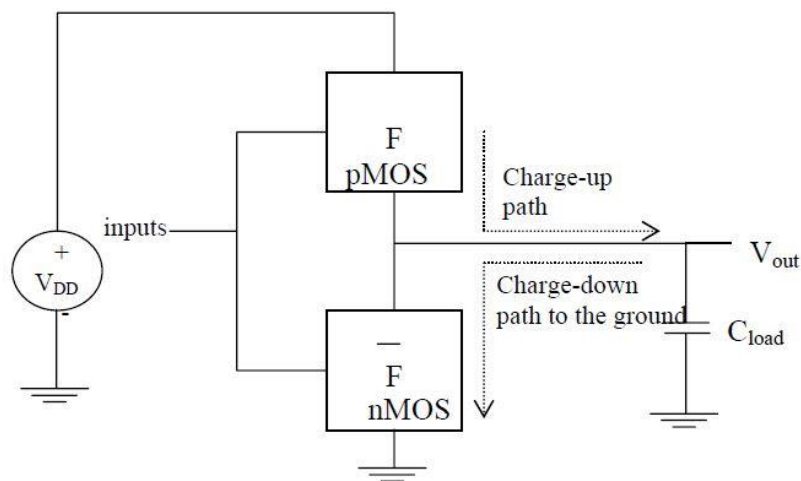


Figure 3. CMOS switching process

During device switching, power dissipation primarily occurs in conventional CMOS circuits. In CMOS logic design half of the power is dissipated in PMOS network and during the switching events, stored energy is dissipated during discharging process of output load capacitor. CMOS NAND gate is shown in the figure (5) which consists of 2 PMOS and 2NMOS devices.

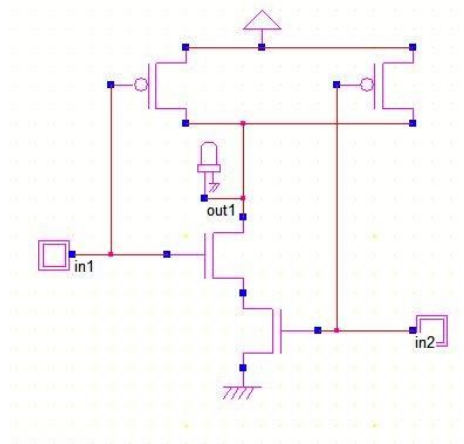


Figure 4. CMOS NAND gate

3. ADIABATIC LOGIC CIRCUITS

3.1. Operation of Adiabatic Logic

The term adiabatic indicates the thermodynamics process which is used to describe a process with no transfer of heat with the environment. Hence the adiabatic logic structure effectively reduces the power dissipated in a circuit. The adiabatic switching technique can realize very low power dissipation. Figure (6) shows the adiabatic switching process.

Adiabatic logic offers a method to use the energy stored in load capacitors compared to the traditional method of discharging load capacitor to the ground and this energy is wasted. Thus, the term adiabatic logic implements reversible logic and used in low-power VLSI circuits.

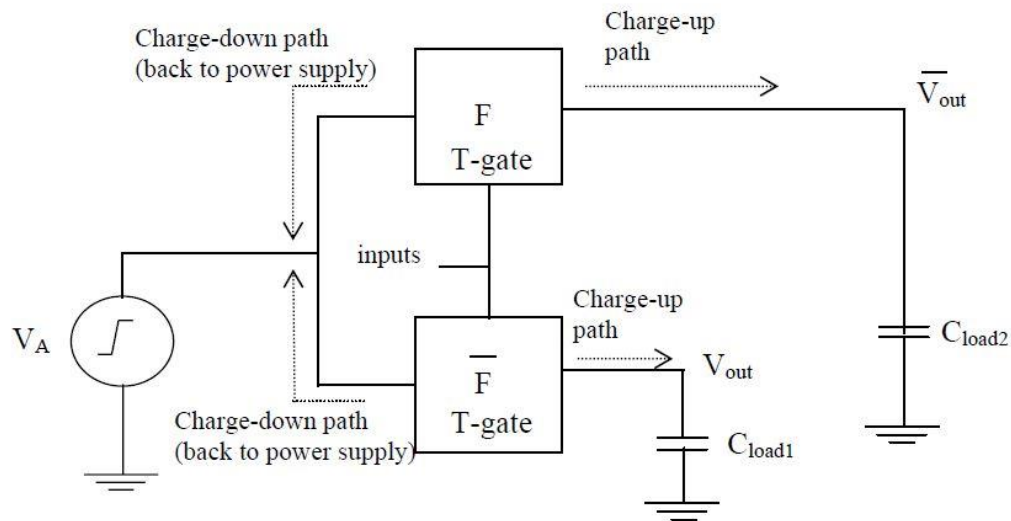


Figure 5. Adiabatic Switching Process

3.2. Efficient Charge Recovery Logic (ECRL)

ECRL consists of two cross coupled PMOS transistors and two N-functional blocks for ECRL adiabatic logic block. Both out and out bar are generated. Energy dissipation is reduced to a large extent in ECRL logic by performing the precharge and evaluation phase simultaneously.

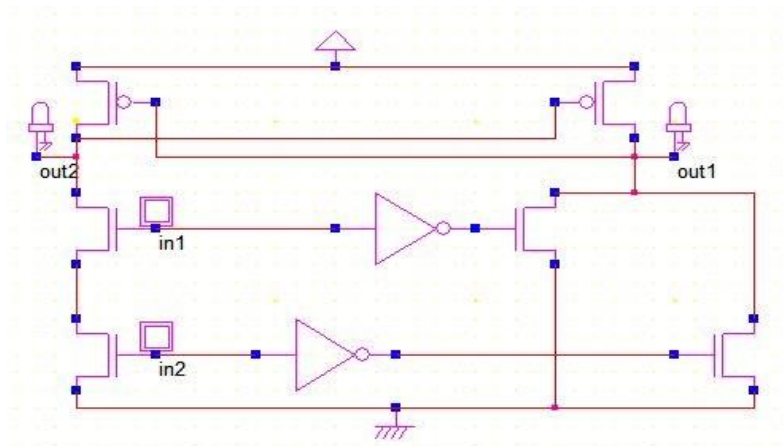


Figure 6. ECRL NAND gate

ECRL dissipates less energy than other adiabatic logics by eliminating the precharge diodes. It consists of only two PMOS switches. It provides full swing at the output. The basic structure of ECRL logic is similar to the Differential Cascode Voltage Switch Logic (DCVSL) with differential signaling. Figure (7) shows the ECRL NAND gate. A major disadvantage of ECRL circuit is that the coupling effects due to the two outputs are connected by the PMOS latch and the two complementary outputs can interfere with each other.

3.3. Improved Efficient Charge Recovery Logic (IECRL)

IECRL consists of a pair of cross coupled PMOS device and two N-functional blocks. In IECRL, delay has been improved by adding a pair of cross coupled NMOS devices in the ECRL design. The basic structure of IECRL is similar to the Modified Differential Cascode Voltage Switch Logic (MDCVSL) with differential signaling. Figure (8) shows the IECRL NAND gate.

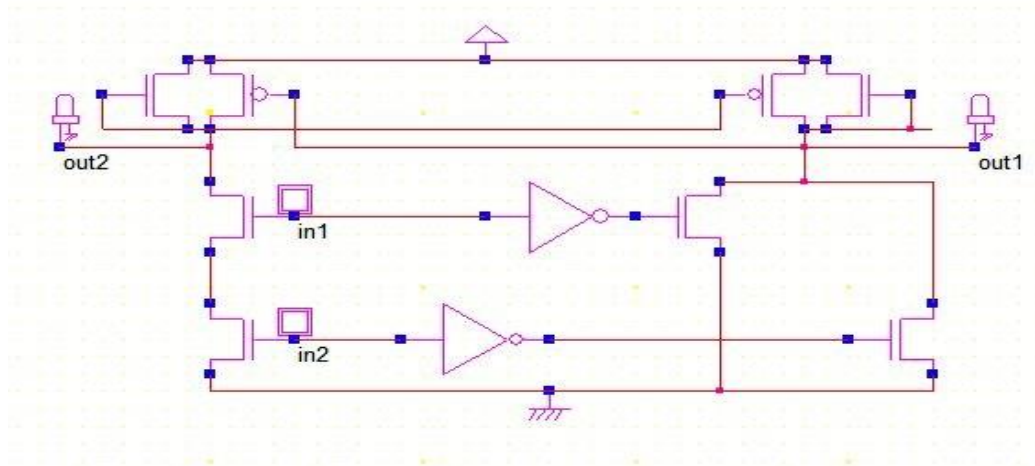


Figure 7. IECRL NAND gate

The IECRL logic is the improved ECRL logic. The performance of IECRL is better than the ECRL logic even though the number of transistors is higher than the ECRL logic. The main advantage of IECRL logic is that it consists of a pair of cross coupled NMOS devices to improve the performance of ECRL logic.

4. DESIGN AND IMPLEMENTATION OF PROPOSED CIRCUITS

A 16:1 multiplexer and 1:16 demultiplexer are designed using adiabatic techniques namely ECRL and IECRL which shows reduce in power dissipation compared to the conventional CMOS logic. The proposed circuit and layout for combinational circuits has been designed in microwind2 version tool and DSCH2 software. The DSCH2 and Microwind2 are user friendly PC tools for the design and simulation of CMOS integrated circuits. The schematic diagram of all proposed circuits is designed in DSCH software. Using DSCH2 verilog file is generated for schematic diagram of all logic operation. By compiling this verilog file in microwind2, the CMOS layout of the schematic diagram is generated. This layout is simulated in microwind2 to observe the power dissipation of the circuit.

4.1. 16:1 Multiplexer

A 16:1 multiplexer consists of 16 input lines, 4 select lines and 1 output line. Figure (9) and (11) shows the 16:1 multiplexer design using ECRL and IECRL respectively. The number of transistors used in 16:1 multiplexer design using ECRL and IECRL are 162 and 164 respectively. Figure (10) and (12) shows the simulation results 16:1 multiplexer using ECRL and IECRL respectively. The power dissipation of these circuits is 5.233 mw and 0.239 mw which are lower when compared to conventional CMOS design.

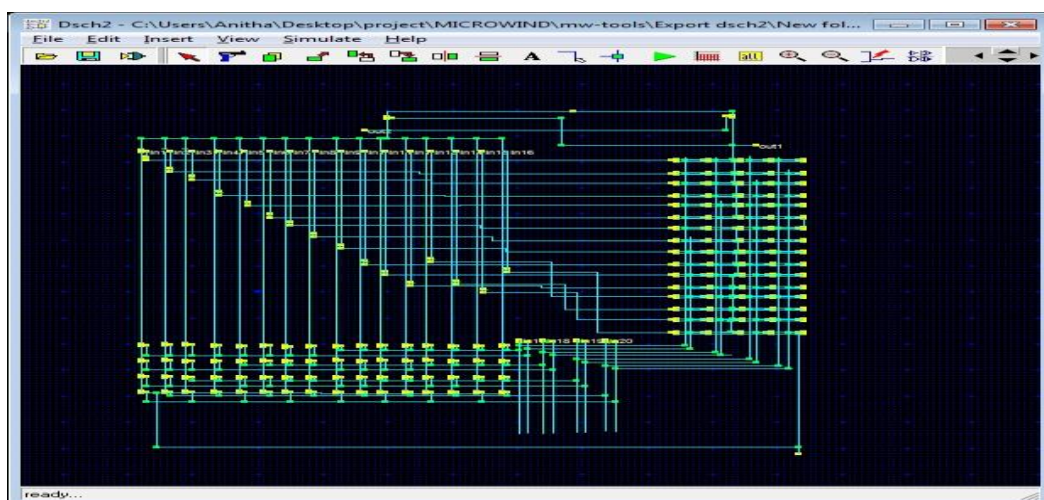


Figure 9. Design of 16:1 Multiplexer Using ECRL Logic



Figure 10. Simulation Output of 16:1 Multiplexer Using ECRL Logic



Figure 11. Design of 16:1 Multiplexer Using IECRL Logic

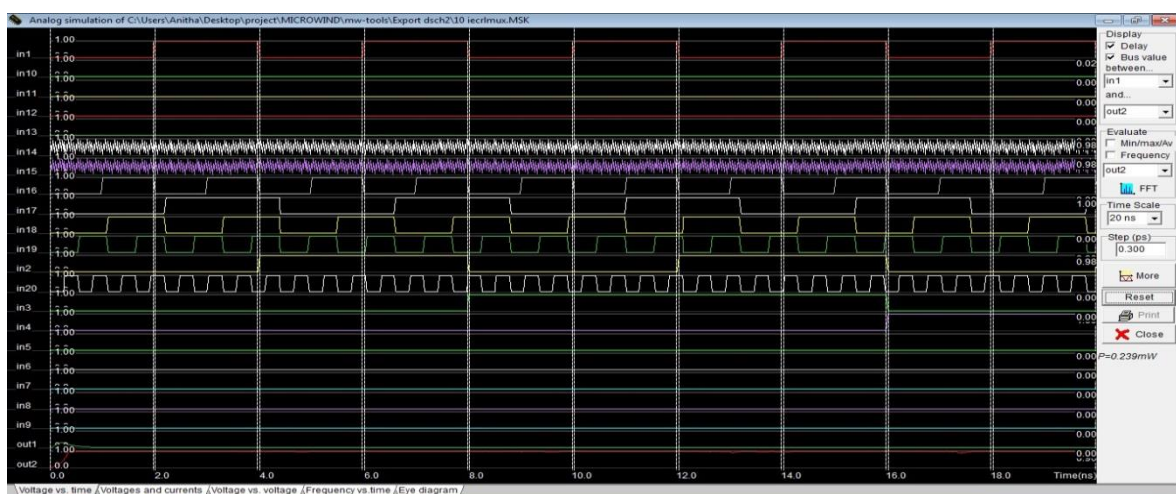


Figure 12. Simulation Output of 16:1 Multiplexer Using IECRL Logic

4.2. 1:16 Demultiplexer

A 1:16 demultiplexer consists of 1 input signal, 4 select signal and 16 output signals. Figure (13) and (15) shows the 1:16 demultiplexer design using ECRL and IECRL respectively. The number of transistors used in 1:16 demultiplexer design using ECRL and IECRL are 162 and 164 respectively. Figure (14) and (16) shows the simulation results 16:1 multiplexer using ECRL and IECRL respectively. The power dissipation of these circuits is 4.946 mw and 0.279 mw which are lower when compared to conventional CMOS design.

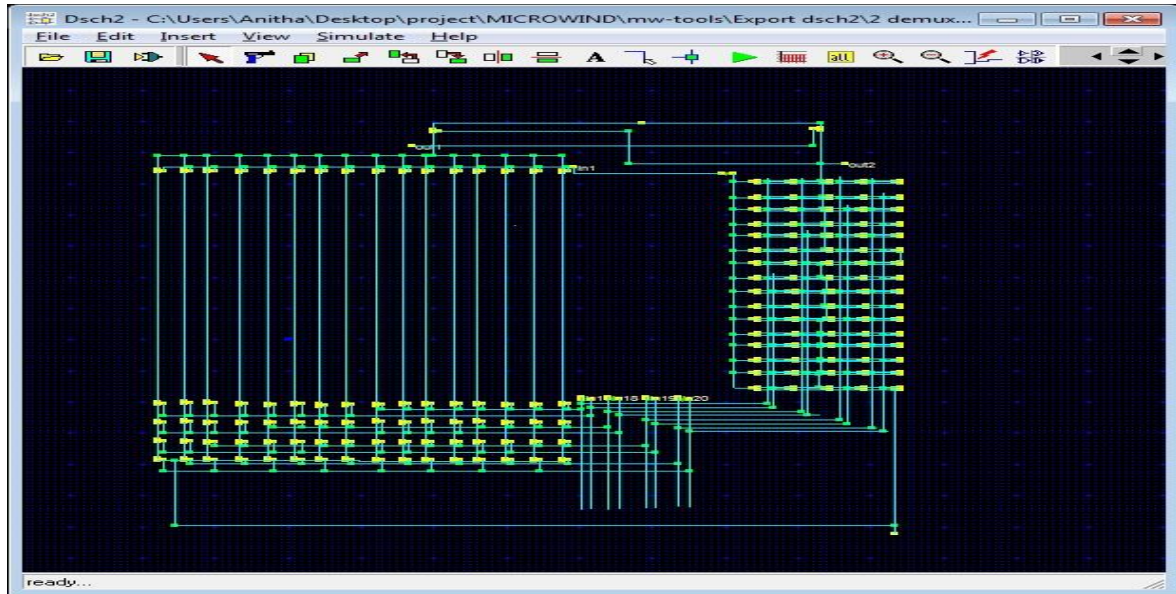


Figure 13. Design of 1:16 Demultiplexer Using ECRL Logic



Figure 14. Simulation Output of 1:16 Demultiplexer Using ECRL Logic

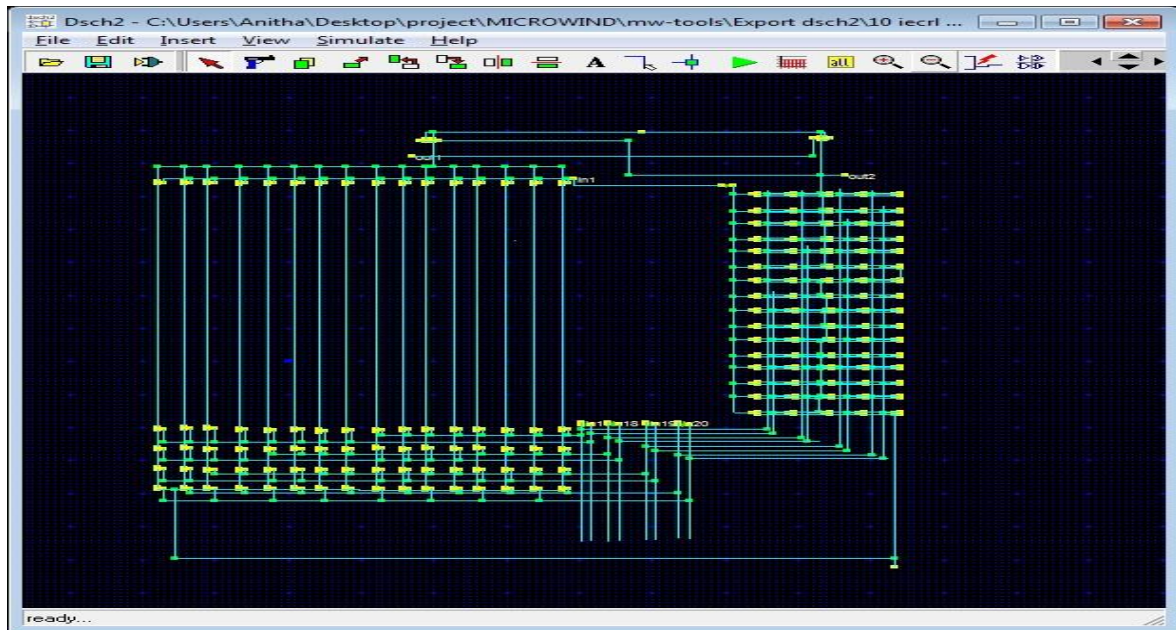


Figure 15. Design of 1:16 Demultiplexer Using IECRL Logic

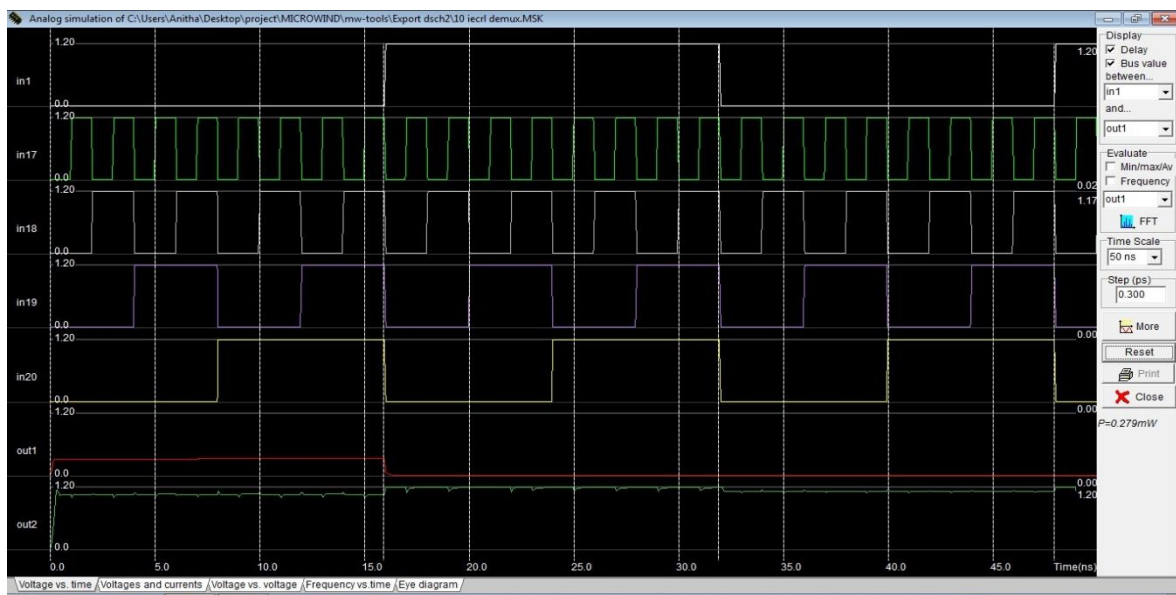


Figure 16. Simulation Result of 1:16 Demultiplexer Using IECRL Logic

5. COMPARATIVE ANALYSIS OF SIMULATION RESULTS

The simulation results are compared based on the power dissipation of the proposed circuits and their transistor count with conventional CMOS logic design. The comparison makes easier to analysis the adiabatic logic circuits based on the power dissipation. The analysis shows that the designs based on adiabatic technique offers significant power reduction which provides better power performance over conventional CMOS circuits.

Table 1. Comparison of 16:1 Multiplexer Using Different Logics

Technology	Power dissipation (mw)	Number of Transistors
Conventional CMOS	14.196	192
ECRL	5.233	162
IECRL	0.239	164

Table 2. Comparison of 16:1 Multiplexer Using Different Logics

Technology	Power dissipation (mw)	Number of Transistors
Conventional CMOS	13.105	160
ECRL	4.946	162
IECRL	0.279	164

6. CONCLUSION

The proposed combinational circuits primarily focus on lowering the power dissipation. Logics for 16:1 multiplexer and 1:16 demultiplexer are designed and the results indicate that they have lesser power dissipation than conventional CMOS circuits. The power dissipation in conventional CMOS circuits is minimized through adiabatic technique. Adiabatic logic works with the idea of switching activities which reduces the power by offering back the stored energy to the supply. The proposed circuits using ECRL and IECRL are compared with conventional CMOS logic for the 16:1 multiplexer and 1:16 demultiplexer. It is observed that the adiabatic technique is good choice for low power application. From the analysis IECRL logic shows significant energy saving compared with conventional CMOS logic and ECRL logic. The future scope of this work is that the proposed 16:1 multiplexers and 1:16 demultiplexers can be cascaded to construct multiplexers and demultiplexers along more number of inputs and output lines.

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