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A novel switch pattern algorithm for fault diagnosis in 27-level trinary switched ladder inverter

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ABSTRACT

This article proposes a novel switch pattern algorithm for diagnosing switch faults in the 27-level trinary switch ladder multi-level inverter (TSLMLI). The proposed novel switch pattern algorithm is a fusion of the improved counter-based neural network for identifying switch fault occurrence and the synthesizable K-nearest neighbor (SKNN) algorithm. The proposed algorithm identifies the switch fault occurrence by making use of the counter-based neural network logic, and the SKNN algorithm predicts the induced faults based on the inverter parameters, namely total harmonic distortions (THD), root mean square voltage (V_{RMS}), and peak voltage (V_{PEAK}). The trinary switched ladder inverter topology is considered for the fault analysis of the switches due to its merit of attaining high levels with less power switch usage. Though there are several fault diagnoses for power inverters based on signals and models, the proposed fault diagnosis algorithm is data-driven, which is fast and precise. This work involves developing switch patterns for the TSLMLI using an angle-based method and concurrently diagnosing the induced faults of the generated switched patterns in the Xilinx Artix-7 field programmable gate array (FPGA) device. The developed algorithm is validated with both electrical and very large scale integration (VLSI) evaluations. Also, the system-on-chip (SoC) design for the proposed algorithm proves the practical feasibility, demonstrating superior hardware acceleration and deterministic real-time execution over traditional microprocessor implementations.

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1. INTRODUCTION

Power inverters are driven by switch patterns irrespective of the topology and modulation scheme utilized. The AC output of the power inverter is used for many industrial applications in real-time, which demands the total harmonic distortion percentage (THD%) to be at the lowest, say less than 5% [1]. This can be ensured only with the error-free driving of the switches in the multi-level inverter (MLI). In practice, the switches are affected and generate a faulty switch pattern that has to be identified as it directly influences the cost and efficiency of the inverter. Conventionally, the drive for the switches involves pulse width modulation (PWM) signals for the generation of AC output. The PWM signals are generated with low frequency to compensate for the complexity of the switching patterns [2]. The control for the switches is produced by making of Hybrid PWM algorithm to lower the complex circuit setup [3]. The parameters of the inverter switches are manipulated mathematically to compare with the different topologies of the MLI [4].

With the advent of artificial intelligence algorithms both machine learning and deep learning, the faults in the power switches can be diagnosed easily and efficiently [5]. This is because the fault diagnosis of power switches of the MLI is accurate using the artificial intelligence algorithm. The artificial intelligence-based fault investigation for a 5-level cascaded MLI is effective and accurate in identifying common faults in insulated gate bipolar transistors [6]. The machine learning fault identification in switches and phases of the 3-phase NPC MLI are accurate under the renewable PV source [7]. The inverter under test is subjected to fault detection to identify the condition and if it is faulty, the scan for faulty phase in the inverter is performed [8], [9]. The inverter based on solar is utilized with the Bayesian network algorithms to detect the various fault occurrences that degrade the efficiency of the converter [10].

The fault diagnosis of inverters is attained with the Gramian Angular Summation Field to transform the 1D value to 2D images to extract the features with the modified AlexNet model. Though this fusion diagnosis algorithm exhibits high accuracy, fault recovery is not feasible [11]. The extreme learning machine is used to identify the open circuit faults in the MLI with noise immunity [12]. A fusion of a machine learning algorithm with fuzzy logic can be used to classify the fault occurrence in the power grid [13]. Harris Hawk's algorithm is used to optimize the extracted voltage and current features to locate faults with accuracy for the HVDC transmission line [14].

The fault diagnosis algorithm based on deep neural network and wavelet compression could detect the OC faults in switches of the power converters [15]. The AC outputs are transformed to the frequency domain to extract features using convolutional neural network (CNN) and analyzed for different level faults by multi-scale kernel CNN algorithm [16]. The switching faults of the AC-DC converter can be diagnosed with the use of artificial neural network (ANN) by extracting the pattern of the switches of the series hybrid electric vehicles (SHEV) [17]. The combination of deep neural network and discrete wavelet transform algorithm in comparison with the wavelet packet transform accurately classifies the faults in the hybrid energy-based microgrid [18].

The real-time hardware implementation of fault detection in a MLI is possible using the K-nearest neighbor (KNN) algorithm [19]. The ANN is utilized to monitor the open circuit switching faults at a given estimated time, as the semiconductor switching devices are vulnerable to frequent faults [20]. Though CNN based model is used to detect certain fault types in MLIs, the integration of deep learning architecture with machine learning algorithm could enhance the accuracy of diagnosing faults [21]. From the standard to the multiple open and short faults, the efficiency of the DWT-ANN-Labview technique is superior to the FFT-ANN-labview technique [22]. With the utilization of several topologies and modulation schemes in power inverters, the conventional power switch fault analysis depends heavily on microprocessor driven software based algorithm. The microprocessors demerits with high latencies and software overhead that are unprotective for high reliable applications. This work overcomes these limitations and presents a full hardware accelerated system-on-chip (SoC) optimized for low-latency embedded systems and industrial internet of thing (IIoT) applications. The proposed novel switch pattern algorithm is developed by a fusion of improved counter-based neural network and synthesizable K-nearest neighbor (SKNN) algorithm at the register-transfer level (RTL). The memory intensive floating point operators used in deep learning models are eliminated by this hybrid approach. The field programmable gate array (FPGA) implementation of the fault diagnosis makes it suitable for smart-grid infrastructures, automation industry and locomotives.

A major concern in the existing hardware artificial intelligence based fault algorithms is their dependency on spectral processing blocks or complex floating point arithmetic arrays. These could cause high delay in execution and increase the physical logics. This article addresses these issues by utilizing synthesizable integer only approach for transforming the 27-level switching patterns as 19 irregular integer sequences with no multipliers and this attaining ultra low-power and matching area constraints of reconfigurable embedded IC design.

2. THE PROPOSED METHOD: NOVEL SWITCH PATTERN ALGORITHM

This section will explain the novel algorithm as: i) improved counter based neural network for the indication of fault occurrence in the switching patterns and ii) real-time SKNN algorithm to predict the occurrence of the fault in power switches based on the AC output parameters say THD%, peak voltage (V_{PEAK}), and root mean square voltage (V_{RMS}). For the sake of validating the proposed algorithm, the 27-level trinary switch ladder multi-level inverter (TSLMLI) is selected. The practical advantage of the TSLMLI is the ability to achieve higher levels of AC output with the minimum number of switches in the inverter circuit.

2.1. Trinary switched ladder multi-level inverter topology

The switched ladder-based MLI topology consists of metal oxide semiconductor field-effect transistor (MOSFET) switches in the pattern of ladder form as given in Figure 1. The ladder structure of the

MLI consists of a ground at the center of its topology to represent the partition of the positive voltage sources right side to the ground node and negative voltage sources left side to the ground node. Also, on the positive side, the voltages are in the forward direction, and on the negative side, the voltages are in the reverse direction.

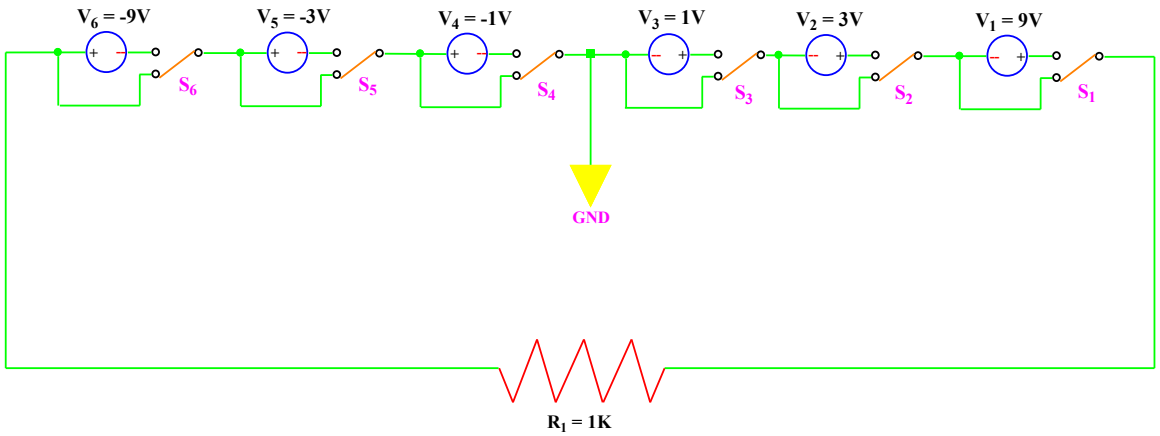


Figure 1. TSLMLI circuit topology

There are several types of inverter topologies based on DC source voltage values. The asymmetrical inverter topology driven by the progression formula in the voltage sources is advantageous compared to the symmetrical inverter topology. Based on the progression type utilized in the DC source values, the asymmetrical switched ladder MLI can be further divided into several types such as binary switched ladder MLI, modified binary switched ladder MLI, luo progression switched ladder MLI, ye progression switched ladder MLI, and TSLMLI. Among these types of switched ladder MLI, the TSLMLI is superior in terms of the number of switches employed, the number of stages in the design, the number of DC sources, and the number of levels attained in the inverter as given in Table 1. The merit of the TSLMLI circuit is that it can attain 243 levels of MLI with 10 power switches in its topology which is maximum compared to the other progression-based topologies.

Table 1. Comparison of inverter characteristics for different switched ladder topologies

Inverter properties	Binary ladder	Luo ladder	Ye ladder	Trinary ladder
Number of switches	10	10	10	10
Number of stages	10	10	10	10
Number of DC sources	10	10	10	10
Total number of levels	63	189	225	243

The 27-level TSLMLI is considered with the trinary progression in the DC voltage sources for the proposed method. The trinary progression utilized for the 27-level TSLMLI consists of 6 switches in which 3 switches control the DC voltage sources of +1V, +3V, and +9V and 3 switches control the DC voltage sources of -1V, -3V, and -9V. The negative DC voltage is achieved by the reverse bias of the DC source in the ladder structure. The DC source in the ladder structure of the TSLMLI is powered by the trinary progression. Trinary progression values, such as V0=1V, V1=3V, V2=9V, and V3=27V, are assigned to the voltage sources. The TSLMLI circuit's DC voltage sources are expressed using (1):

$$V_{DCN} = 3_N E \quad (1)$$

where N=number of levels.

$$E = DC\ voltage$$

The 27-level TSLMLI circuit consists of 13 levels in the positive cycle, 13 levels in the negative levels, and 1 level at "Zero". To drive the switch pattern of the 27-level TSLMLI, the half height switch angle method is utilized as given in (2).

$$\alpha_i = \sin^{-1}\left(\frac{2i-1}{m-1}\right) \quad (2)$$

where i=1, 2, …., $\frac{m-1}{2}$.

This algorithm is utilized as it inherently generates an AC output with optimized THD profiles. The angle of changing events is calculated as per the formulation given in (2) and converted to digital values with a resolution of 2^8 bits. The x-axis angles from 0° to 360° of an AC cycle are converted as 0 to 255 bits in digital format. Table 2 presents the digital equivalent for the quadrants of the AC output.

Table 2. Bit equivalence for the quadrant angles of the MLI

Quadrant	Angles	28 bits equivalence
First	0–90	0–63
Second	90–180	64–127
Third	180–270	128–191
Fourth	270–360	192–256

For coding purposes, the resulting number is also rounded up to the closest integer value. The angles are used to generate 26 DPWM signals with a resolution of 2^8 bits. The intended switch patterns for the 27-level TSLMLI are obtained by logically combining the 26 DPWM signals that were generated. Six different switch patterns are needed for generating the 27-level AC output of the TSLMLI. The notations of the 6 switches are represented as S_1, S_3, and S_9 for the positive cycle and S_{B1}, S_{B3}, and S_{B9} for the negative cycle.

2.2. Improved counter-based neural network for fault identification

This section indicates the occurrence of switch faults by using the proposed method to monitor the faults in switch patterns of the 27-level TSLMLI circuit. The errors in the generated 6 switching patterns of the 27-level TSLMLI will have an impact on the levels, damaging the switches, and thus increasing the cost. The switch patterns of the power inverter depend on the topology utilized in the circuitry. As discussed earlier, in this work, the switch patterns are generated using the non-carrier angle-based manipulation for the 27-level TSLMLI. The switch patterns are considered in two formats namely direct bits as $S_1S_3S_9S_{B1}S_{B3}S_{B9}$ and reversed bits as $S_{B1}S_{B3}S_{B9}S_1S_3S_9$ along with their decimal equivalence. The positive levels of the 27-level TSLMLI and negative levels of the 27-level TSLMLI are considered in decimal equivalence. In the comparison of the decimal equivalent values of both tables, the minimum values are considered for the evaluation of the proposed algorithm, thus the reversed bit format is taken for the positive levels and the direct bit format is considered for the negative. The redundancy of decimal equivalent values of the switch patterns is removed and normalized as depicted in Table 3. These 19 decimal values are oriented to form an irregular counter sequence and fed as the input nodes for the proposed improved counter-based neural network algorithm. These 19 values of the irregular counter (0, 1, 2, 3, 4, 5, 6, 7, 10, 12, 14, 17, 20, 21, 28, 33, 34, 35, 49) should occur in one cycle of AC output for error-free switching patterns in the 27-level TSLMLI. If any deviation from this counting, then the proposed algorithm indicates the error in the any of the 6 switch patterns of the 27-level TSLMLI. The proposed method indicates precisely the faulty switch of the 27-level TSLMLI.

The 19 irregular counter values are subjected to a multi-layer neural network structure that consists of 2 hidden layers with 21 nodes each and output layer of 19 target values ranging from 0.05 to 0.95. The number of nodes for the hidden layer is restricted to 21 based on two criteria: i) the total number of nodes of the hidden layer (21 nodes) is greater than the number of nodes assigned in input layer (19 nodes) and output layer (19 nodes) individually and ii) the number of node in the hidden layer (21 nodes) is less than the total nodes of both input and output layers (38 nodes). Also, the hidden layer nodes count is fixed at 21 nodes to minimum the complexity of synthesizable HDL code in real-time. The proposed counter based neural network consists of 800 synaptic weights to be optimized for the precise development of HDL code.

2.3. Synthesizable K-nearest neighbour algorithm for fault prediction

This section explains the SKNN algorithm that is developed based on the performance parameters evaluated from the AC output of the 27-level TSLMLI. The parameters namely THD%, V_{PEAK}, and V_{RMS} values are considered under all possible circumstances of error occurrence in the switching pattern of the 27-level TSLMLI. The designation of N and E are used to indicate the "No error" and "Error", respectively. Table 4 presents the possible error incorporation in binary format as it starts with the least significant bit (S_1)

and to the most significant bit (S_{B9}). The 6 switch patterns are induced with the possible error in the switching pattern and their corresponding parameters are derived.

Table 3. Normalization of the positive and negative levels for the 27-level TSLMLI

Levels	Decimal value	Levels	Decimal value	After normalization
-13	7	13	7	0
-12	3	12	3	1
-11	35	11	14	2
-10	5	10	5	3
-9	1	9	4	4
-8	33	8	12	5
-7	21	7	21	6
-6	17	6	20	7
-5	49	5	28	10
-4	6	4	3	12
-3	2	3	2	14
-2	34	2	10	17
-1	4	1	1	20
0	0	0	0	21
				28
The decimal equivalence of the levels is taken in increasing order.				33
The repeated values are considered only once.				34
				35
				49

Table 4. Possible errors induced in the switches to evaluate parameters of THD%, V_{PEAK}, and V_{RMS}

SWITCHES						THD%	V_{PEAK}	V_{RMS}	SWITCHES						THD%	V_{PEAK}	V_{RMS}
S_{B9}	S_9	S_{B3}	S_3	S_{B1}	S_1				S_{B9}	S_9	S_{B3}	S_3	S_{B1}	S_1			
N	N	N	N	N	N	3.28	128.1	90.6	E	N	N	N	N	N	42.73	74.55	52.71
N	N	N	N	N	E	5.52	127	89.83	E	N	N	N	N	E	42.38	73.43	51.92
N	N	N	N	E	N	5.53	127	89.8	E	N	N	N	E	N	43.64	73.43	51.92
N	N	N	N	E	E	7.78	125.9	89.01	E	N	N	N	E	E	43.96	72.31	51.13
N	N	N	E	N	N	14.05	118.7	83.96	E	N	N	E	N	N	43.15	65.16	46.07
N	N	N	E	N	E	14.82	117.6	83.18	E	N	N	E	N	E	42.68	64.04	45.28
N	N	N	E	E	N	14.58	117.6	83.17	E	N	N	E	E	N	43.97	64.04	45.28
N	N	N	E	E	E	16.04	116.5	82.38	E	N	N	E	E	E	44.36	62.92	44.49
N	N	E	N	N	N	14.27	118.7	83.94	E	N	E	N	N	N	46.19	65.15	46.07
N	N	E	N	N	E	14.71	117.6	83.15	E	N	E	N	N	E	45.51	64.03	45.28
N	N	E	N	E	N	15.08	117.6	83.14	E	N	E	N	E	N	47.36	64.04	45.28
N	N	E	N	E	E	16.21	116.5	82.36	E	N	E	N	E	E	47.50	62.92	44.49
N	N	E	E	N	N	26.42	109.3	77.31	E	N	E	E	N	N	55.81	55.76	39.43
N	N	E	E	N	E	26.93	108.2	76.52	E	N	E	E	N	E	55.35	54.64	38.64
N	N	E	E	E	N	26.98	108.2	76.51	E	N	E	E	E	N	57.07	54.64	38.64
N	N	E	E	E	E	27.96	107.1	75.72	E	N	E	E	E	E	57.53	53.52	37.84
N	E	N	N	N	N	42.17	74.65	52.79	E	E	N	N	N	N	149.46	21.04	14.88
N	E	N	N	N	E	43.09	73.54	52.0	E	E	N	N	N	E	153.32	19.92	14.09
N	E	N	N	E	N	41.91	73.52	51.99	E	E	N	N	E	N	153.44	19.91	14.08
N	E	N	N	E	E	43.50	72.41	51.2	E	E	N	N	E	E	160.25	18.8	13.29
N	E	N	E	N	N	45.60	65.29	46.17	E	E	N	E	N	N	171.22	11.67	8.251
N	E	N	E	N	E	46.80	64.18	45.38	E	E	N	E	N	E	176.09	10.57	7.472
N	E	N	E	E	N	45.02	64.16	45.37	E	E	N	E	E	N	173.41	10.54	7.45
N	E	N	E	E	E	47.05	63.05	44.58	E	E	N	E	E	E	186.79	9.432	6.669
N	E	E	N	N	N	42.84	65.22	46.12	E	E	E	N	N	N	171.95	11.64	8.227
N	E	E	N	N	E	43.66	64.11	45.34	E	E	E	N	N	E	173.87	10.51	7.435
N	E	E	N	E	N	42.46	64.1	45.32	E	E	E	N	E	N	176.99	10.52	7.44
N	E	E	N	E	E	44.14	62.98	44.54	E	E	E	N	E	E	187.41	9.398	6.645
N	E	E	E	N	N	55.55	55.86	39.5	E	E	E	E	N	N	440.99	2.24	1.584
N	E	E	E	N	E	56.83	54.75	38.72	E	E	E	E	N	E	512.19	1.14	0.8062
N	E	E	E	E	N	55.20	54.73	38.7	E	E	E	E	E	N	516.36	1.129	0.7984
N	E	E	E	E	E	57.41	53.62	37.92	E	E	E	E	E	E	0	0	0

The SKNN algorithm is developed using the VHDL code by considering the Euclidean calculation for THD%, V_{PEAK}, and V_{RMS} parameters to predict the faults in the switches. The VHDL code is trained with these table values to give prediction according to any test value of the parameters. Figure 2 depicts the block diagram of the proposed algorithm. Practically, the possibility of error occurrence in the switches is limited to two switches; however, the proposed methods have been able to consider all possible combinations of the faults in the 6 switch patterns of the 27-level TSLMLI. The proposed method is the fusion of VHDL codes

consisting of VHDL code developed for the 6 switch pattern generation, VHDL code for fault occurrence using the improved counter-based neural network, and VHDL code for the fault prediction using the SKNN algorithm.

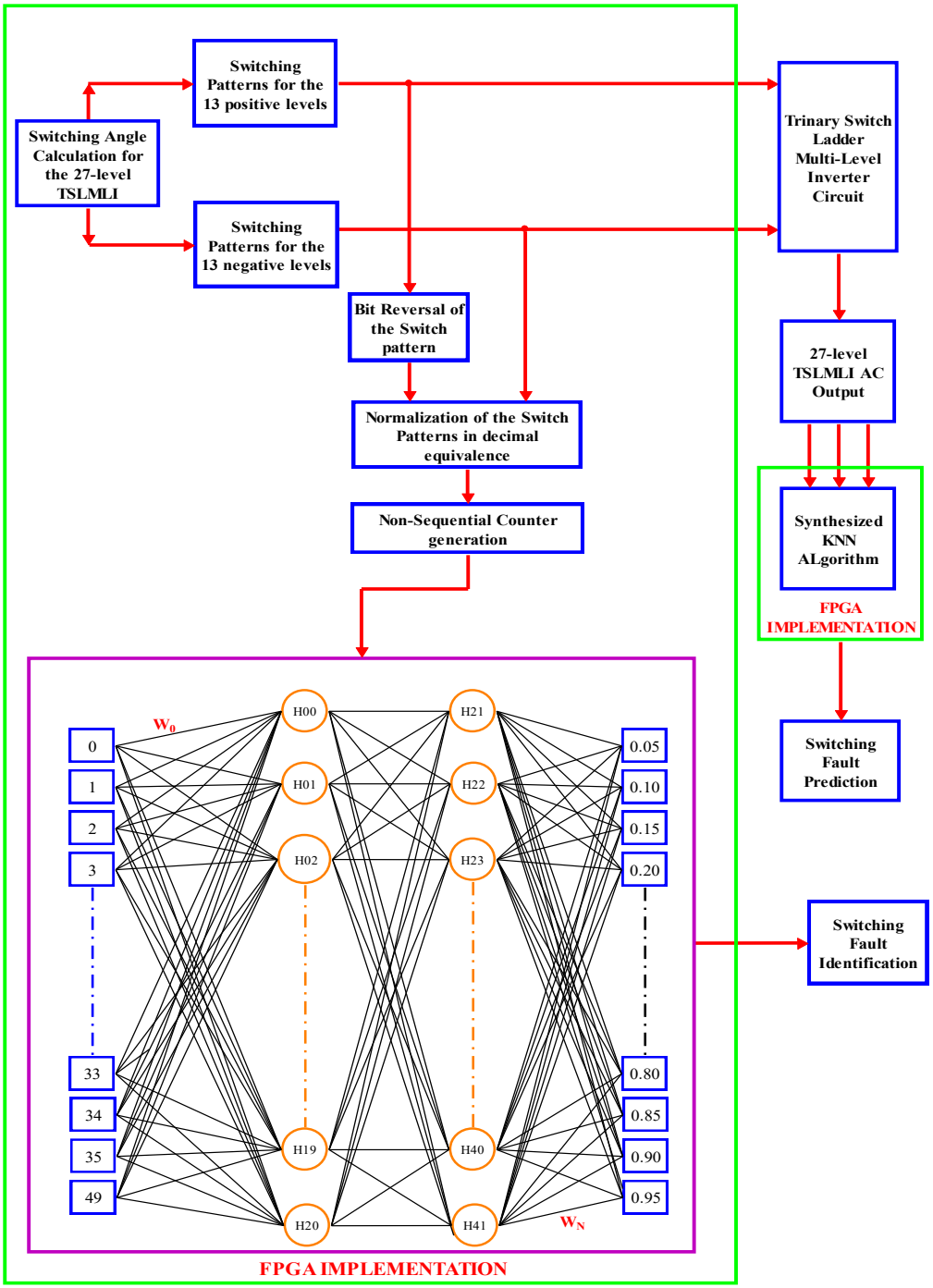


Figure 2. Block diagram of the proposed switch pattern algorithm to fault occurrence in the 27-level TSLMLI

3. RESULTS AND DISCUSSION

The experimental verification for the proposed method is validated by inducing two single switch errors in real time. As indicated in Table 3, the error induction in the switches S_1, S_{B1}, and S_3 gives a reduced THD% error compared to the other switches S_{B3}, S_9, and S_{B9} in the 27-level TSLMLI. In this work, the

minimum THD% switch combinations are considered by inducing the real time error at two instances namely: i) S_1 & S_{B1} and ii) S_3 & S_{B1}. The real-time validated output for the 27-level TSLMLI using the FPGA device is implemented and verified using DSO output and its CSV file is imported into the MATLAB/Simulink environment to calculate the THD% of the AC output at 4.96% as given in Figure 3 for no error.

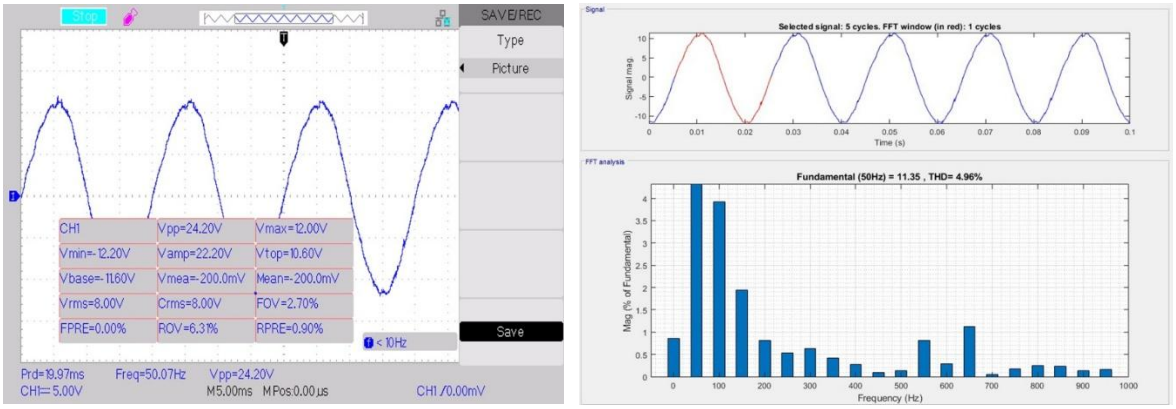


Figure 3. Experimental AC output for the 27-level TSLMLI without any error induction with THD% as 4.96%

3.1. Case I: induction of errors at S_1 and S_{b1}

The induction of errors at S_1 and S_{B1} degraded the THD% of the real-time AC output for the 27-level TSLMLI. The THD% calculated for the induced error combinations produces a value of 7.26%. The target values of the counter-based neural network are affected when the switch errors (S_1 and S_{B1}) are induced and trigger the fault signal to be high indicating the erroneous status of the output. Simultaneously, the THD% of 7.26% as given in Figure 4 is fed as input for the secondary SKNN algorithm to predict the exact faulty switch for the 27-level TSLMLI.

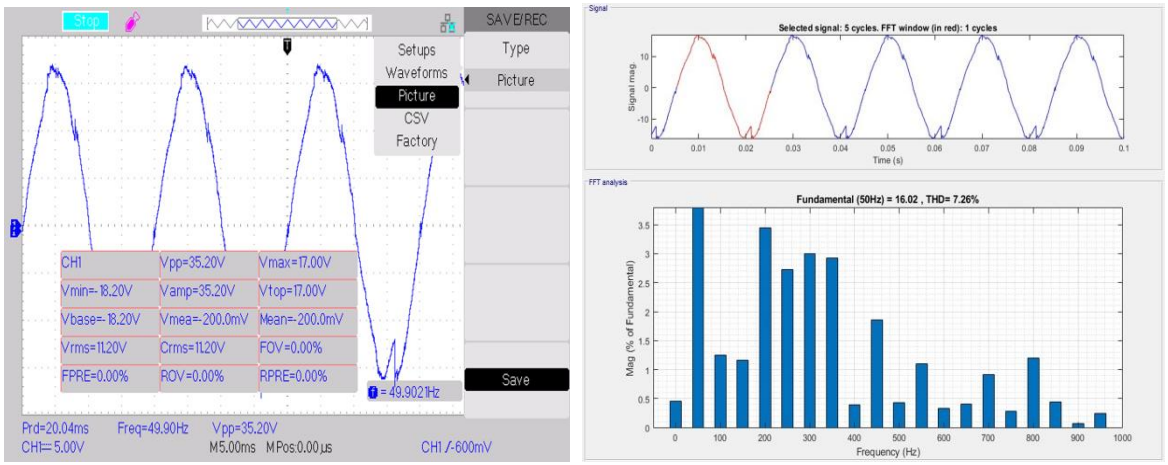


Figure 4. Experimental AC output for the 27-level TSLMLI with 2 errors induced at S1 and B1 and its THD% as 7.26%

3.2. Case II: induction of errors at S_3 and S_{b1}

In this case, the errors are induced at switches S_3 and S_{B1} and checked for the THD% parameter of the 27-level TSLMLI AC output. In this case, the fault signal is ascertained due to the difference in the actual and target values of the counter-based neural network. After inducing the errors at S_3 and S_{B1}, the THD% of the AC output is 14.53% as depicted in Figure 5. Concurrently, the prediction for the observed THD% is

verified as it presents a closer prediction of the faulty switches of the S_3 and S_{B1} by utilizing the SKNN algorithm. Figure 6 depicts the output waveform that concurrently predicts the faulty switches based on the THD% values using the SKNN. The output for the prediction is evaluated using the Xilinx Vivado tool.

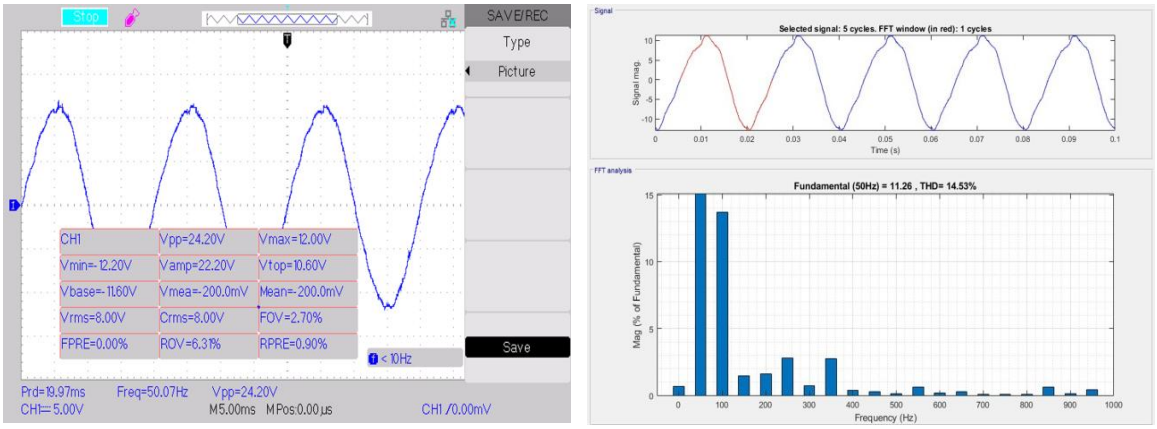


Figure 5. Experimental AC output for the 27-level TSLMLI with 2 errors induced at S3 and B1 and its THD% as 14.53%



Figure 6. Output for the prediction of the KNN algorithm using inverter parameters of THD%, V_{RMS}, and V_{PEAK}

3.3. Hardware synthesis, power, and benchmarking

The proposed HDL architecture is developed to evaluate area occupancy and physical feasibility when implemented. The IC layout is developed using the Cadence Innovus tool that transforms RTL code into a GDSII-ready SoC design as shown in Figure 7. The 186 real time signals have be accommodated in the Artix-7 FPGA device and the need for this fusion approach is validated in this study. While the counter-NN core handles rapid fault detection (45.200 ns), the fused KNN pipeline is required to achieve complete localization within a fully deterministic 274.384 ns window. Tables 5 and 6 details the profile of clock tree synthesis (CTS) and direct comparison against state-of-the-art FPGA devices.

As depicted in the comparison table, the proposed method achieves significant low logic utilization in both LUT and FF blocks compared to the standard deep networks. Crucially, the system locks in a fully deterministic diagnostic latency of just 274.384 ns while maintaining an ultra-low leakage power footprint of 1.97% (0.00256 W). This structural efficiency validates the hybrid architecture for highly constrained reconfigurable edge monitors and IoT-enabled smart grids where software-induced delays are unacceptable.

The open circuit failure in the power switches triggers an omission in the voltage step of the AC output. This induces energy into lower-order harmonics, and causes a drop in the fundamental peak voltage and a correlated expansion of the harmonic distortion profile. The SKNN framework tracks these parametric

shifts via parallel on-chip Euclidean distance pipelines, rendering high sensitivity during complex multi-fault events (including total concurrent system shutdowns). Operating as a reconfigurable hardware companion core integrated directly alongside primary gate drivers, this framework enables microsecond-level fault isolation, protecting high-voltage converters from cascading physical destruction.

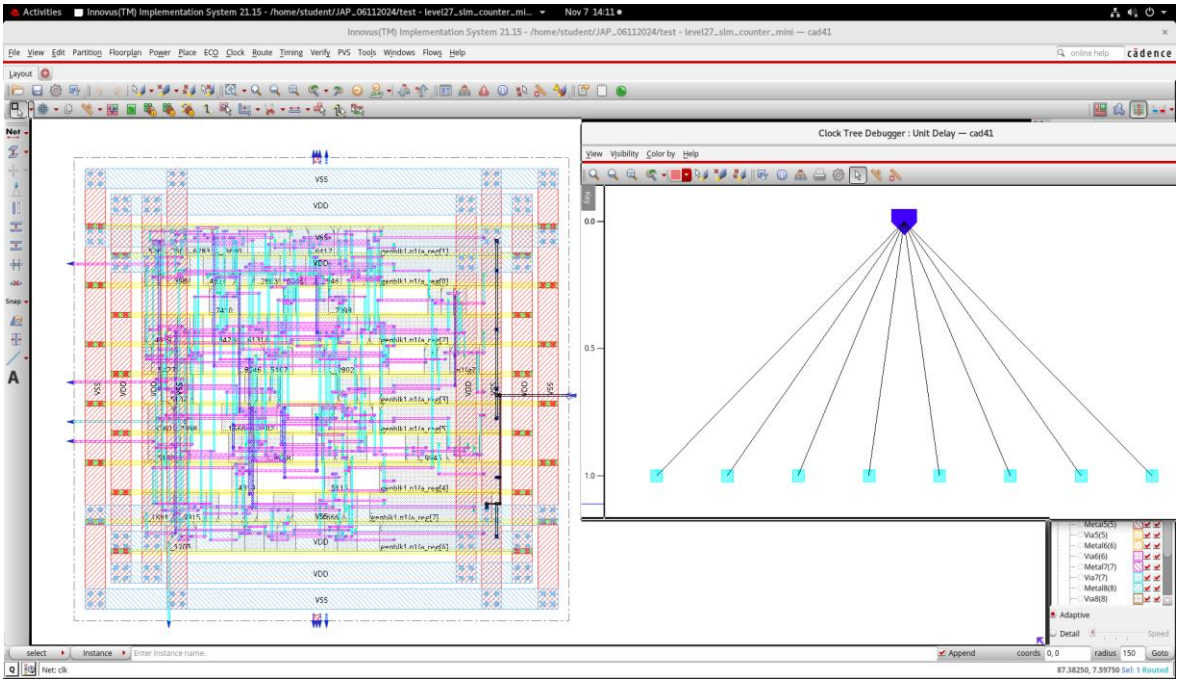


Figure 7. IC layout design for the proposed algorithm using cadence innovus tool

Table 5. Post-CTS power consumption profiling (cadence innovus at 0.9 V)

Power type/group	Internal power (W)	Switching power (W)	Leakage power (W)	Total power (W)	Percentage (%)
Sequential logic	0.07691	0.008053	0.001134	0.08610	66.24
Combinational logic	0.02546	0.016980	0.001432	0.04387	33.76
Total net summary	0.10237	0.025034	0.002566	0.12997	100.0

Table 6. FPGA device utilization and performance benchmarking for the proposed method

Parameters	RNN algorithm (Xilinx XCVU9P) [23]	Euler method (Virtex-7 VC709) [24]	Deep neural network model (ZU3EG) [25]	Proposed SP algorithm (Artix 7xc7a200tfbg484-1)
LUT overhead	316727(26%)	32548	52317 (74.1%)	28552(21.34%)
FF overhead	320651 (13%)	17407	33631 (23%)	7049 (2.63%)
DSP block	1626 (13%)	--	172 (47.8%)	406 (54.86%)
Latency/delay	--	--	--	274.384 ns

4. CONCLUSION

The proposed work enables the identification of errors induced at the switches in real time, while simultaneously predicting fault occurrence using the SKNN algorithm. Overall, the work is satisfactory and proves to be feasible for the real-time fault identification of the power inverter switches using an FPGA. The implementation of the proposed novel algorithm on an Artix-7 FPGA demonstrates efficient hardware-software co-design for 27-level trinary switched ladder inverters, characterized by minimal logic resource usage. The system achieves high-performance, real-time control with 274.384 ns latency, reducing switching losses and lowering THD in high-voltage applications. The SoC design for the proposed algorithm proves the blueprint for IC fabrication in real time. Further work could be encouraged toward the utilization of the fusion of switch pattern with deep learning algorithms for higher levels of the power inverter.

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AUTHOR CONTRIBUTIONS STATEMENT

This journal uses the Contributor Roles Taxonomy (CRediT) to recognize individual author contributions, reduce authorship disputes, and facilitate collaboration.

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C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

Authors state no conflict of interest.

INFORMED CONSENT

We have obtained informed consent from all individuals included in this study.

ETHICAL APPROVAL

No animal or human were used in this research work.

DATA AVAILABILITY

The authors confirm that the data supporting the findings of this study are available within the article

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