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AI-assisted performance prediction and optimization of CMOS and GDI logic circuits at 45 nm

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ABSTRACT

An artificial intelligence (AI)-assisted optimization framework is presented for low-power digital circuit design using gate diffusion input (GDI) logic in 45 nm complementary metal oxide semiconductor (CMOS) technology. Core combinational and sequential building blocks, including logic gates, adders, multiplexers, and flip-flops, are implemented at the transistor level using Cadence Virtuoso and compared against conventional CMOS realizations. To accelerate design-space exploration, a random forest regression (RFR) model is trained using transistor-level simulation data to predict power consumption and propagation delay based on supply voltage, transistor sizing, and load capacitance. The proposed model achieves prediction accuracy exceeding 95%, reducing repeated SPICE simulation effort by approximately 45%. Simulation results demonstrate that GDI-based designs achieve up to 55% reduction in power consumption, 45% reduction in silicon area, and nearly 50% improvement in power delay product (PDP) compared to CMOS implementations, while maintaining delay variation within acceptable limits. A cross-technology comparison with 90 nm designs further confirms the scalability and energy efficiency of the proposed approach. The integrated AI–GDI method provides an effective solution for energy-efficient very large scale integration (VLSI) and embedded system applications.

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1. INTRODUCTION

The continued scaling of complementary metal oxide semiconductor (CMOS) technology has enabled high-density integrated circuits but has also intensified challenges related to power dissipation, leakage currents, and process variability at nanometer technology nodes [1], [2]. Emerging applications such as internet of things (IoT) devices, wearable electronics, biomedical sensor nodes, and edge-computing platforms require digital circuits that operate reliably under strict power constraints and reduced supply voltages [3], [4]. Although conventional static CMOS logic offers robustness, its efficiency degrades at deep-submicron nodes due to increased dynamic and leakage power consumption [5]. Gate diffusion input (GDI) logic has emerged as a promising alternative for low-power digital design by reducing transistor count, switching activity, and internal node capacitances [6]–[8]. Compared with CMOS implementations, GDI significantly lowers power consumption and silicon area, particularly in arithmetic and control-oriented circuits [9], [10]. Prior studies

have reported improved performance in logic gates, multiplexers, and full adders using GDI techniques [11]. However, additional low-power techniques such as power gating and multi-threshold CMOS often introduce design overhead and complexity, making manual transistor-level optimization increasingly inefficient as technology scales [12].

Recent advances in machine learning (ML) have enabled prediction-based optimization in very large scale integration (VLSI) design flows. Random forest regression (RFR) has shown strong capability in predicting power and delay while modeling nonlinear parameter interactions, thereby reducing reliance on repeated SPICE simulations [13], [14]. Recent studies further demonstrate the growing adoption of ML for early power, performance, and area estimation, timing prediction, and design-space exploration in VLSI design [15], [16]. While deep learning and graph-based models are increasingly explored for advanced automation tasks [17], [18], ensemble learning methods remain attractive due to their high accuracy, lower computational complexity, and suitability for limited datasets. However, a critical review of these prior works reveals several important limitations. First, most ML-assisted VLSI studies target RTL- or gate-level abstraction and do not extend their prediction frameworks to transistor-level design parameters such as W/L ratio and load capacitance, limiting their applicability to post-layout or late-stage design. Second, GDI-focused studies predominantly report manual simulation results without integrating any automated prediction or design-space exploration tool, leading to high simulation overhead when optimizing across process corners. Third, cross-technology scalability is rarely demonstrated—comparisons between 90 nm and 45 nm nodes are absent in most GDI-oriented works, making it difficult to assess the robustness of reported improvements. Fourth, ensemble learning models such as RFR are seldom validated on combined CMOS-GDI datasets, and their suitability for low-sample transistor-level training regimes remains underexplored. These gaps collectively motivate the present work.

Research gap and motivation: while GDI logic and ML–based performance prediction have been studied independently, their integration at the transistor level for advanced technology nodes remains limited. Most existing studies either analyze GDI circuits without predictive intelligence or apply ML primarily to conventional CMOS designs, resulting in repeated simulations and longer optimization cycles. Specifically, no prior work has simultaneously addressed: i) transistor-level GDI characterization at 45 nm with Cadence Virtuoso, ii) an RFR-based surrogate model trained on combined CMOS and GDI simulation data for power and delay co-prediction, and iii) a cross-technology validation from 90 nm to 45 nm to confirm scalability. The present work bridges these gaps by proposing a tightly integrated AI–GDI design flow that reduces SPICE simulation overhead while preserving prediction fidelity, making it suitable for energy-constrained VLSI and embedded system applications.

Contributions: to address this gap, this work makes the following contributions:

- A transistor-level comparison of CMOS and GDI implementations at the 45 nm technology node for representative combinational and sequential circuits.
- An artificial intelligence (AI)-assisted prediction framework based on RFR that achieves high accuracy for power and delay estimation and reduces design-space exploration time by approximately 45%.
- A cross-technology evaluation between 90 nm and 45 nm nodes, demonstrating the scalability and energy-efficiency benefits of the combined GDI and AI-based optimization approach.

2. RESEARCH METHOD

The proposed AI-assisted GDI optimization framework integrates transistor-level VLSI design with ML–based performance prediction to improve design efficiency for low-power digital circuits at the 45 nm technology node. All circuits were designed and simulated using the Cadence Virtuoso environment with the gpdk045 process design kit (PDK). Transistor-level schematics were implemented using minimum channel lengths and appropriately scaled widths to ensure fair comparison across logic styles. A nominal supply voltage of 1.0 V was selected, reflecting typical operating conditions at this node, where short-channel effects and leakage currents are significant [19], [20]. Conventional CMOS circuits were designed using complementary pull-up and pull-down networks following established static logic methodologies [21], [22]. Corresponding GDI implementations were constructed using the basic GDI cell, in which the source terminals of PMOS and NMOS devices are driven by input signals rather than fixed supply rails. This structure reduces internal node capacitance, transistor count, and switching activity, making GDI suitable for low-power nanoscale design [6], [23], [24].

Figure 1 illustrates the overall workflow of the proposed framework. Initially, CMOS and GDI circuits are designed and simulated at the transistor level to extract key performance parameters, including average power, propagation delay, power delay product (PDP), and transistor dimensions. These simulation results are then used to train a ML model, which predicts circuit performance for unseen configurations and enables rapid

design-space exploration without repeated full SPICE simulations. The overall method consists of two primary phases: i) circuit design and simulation using Cadence Virtuoso and ii) AI-based prediction and optimization.

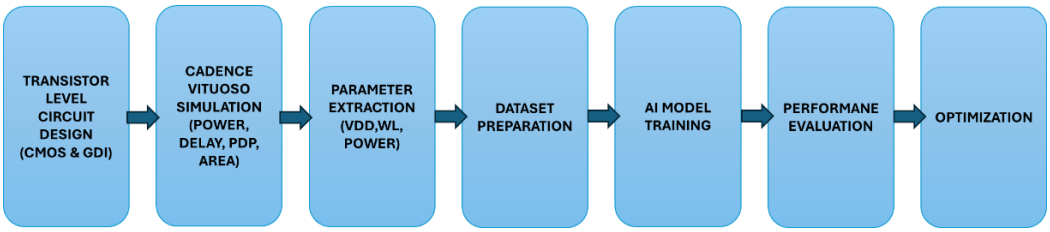
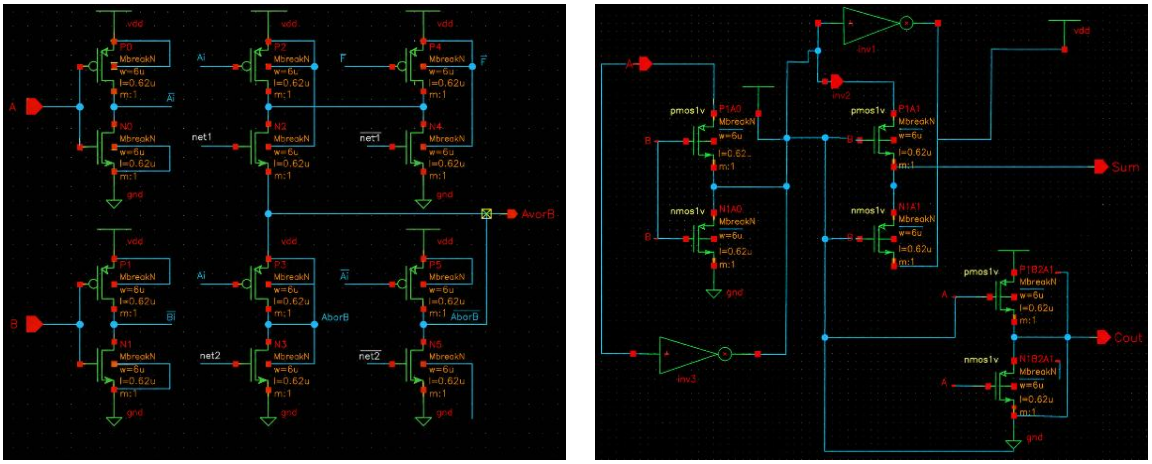


Figure 1. Workflow of the proposed AI-assisted GDI/CMOS design method

2.1. Circuit design and simulation

The study considers essential combinational and sequential digital building blocks commonly used in arithmetic and control datapaths, including NAND and XOR gates, half and full adders, 2×1 multiplexers, and D flip-flops as shown in Figure 2. Figure 2(a) CMOS XOR gate and Figure 2(b) CMOS full adder, shown as illustrative examples of the design method applied uniformly to all six circuits (NAND, XOR, half adder, full adder, 2×1 multiplexer, and D flip-flop) in both CMOS and GDI logic styles. The complete set of schematics for all circuits and logic styles was developed and simulated in Cadence Virtuoso following the same design procedure; the corresponding extracted performance metrics for all twelve configurations are reported in Table 1. Each circuit was implemented using both CMOS and GDI logic styles with identical functional specifications to ensure a fair comparison.



(a) (b)

Figure 2. Representative transistor-level schematics implemented in 45 nm technology; (a) CMOS XOR gate and (b) CMOS full adder

Table 1. Performance comparison of CMOS and GDI (45 nm)

Circuit	Tech	Power (µW)	Delay (ps)	PDP (aJ)	Area (µm²)	Trans. count
NAND gate	CMOS	0.92	12.5	11.5	3.10	4
	GDI	0.51	13.2	6.73	1.85	2
XOR gate	CMOS	2.40	21.0	50.4	5.60	8
	GDI	1.05	18.7	19.6	2.90	4
Half adder	CMOS	3.85	30.4	117.0	7.30	10
	GDI	1.85	26.8	49.6	4.20	6
Full adder	CMOS	4.20	33.5	140.7	9.60	12
	GDI	2.10	28.2	59.2	5.10	8
2×1 MUX	CMOS	1.20	16.3	19.6	3.85	6
	GDI	0.54	15.8	8.53	2.20	3
D flip-flop	CMOS	4.95	42.1	208.3	12.4	10
	GDI	2.45	38.8	95.0	7.2	6

The simulation workflow included transient analysis to extract propagation delays (t_pHL and t_pLH) measured at 50% signal transitions, DC analysis to determine voltage transfer characteristics and validate logic levels, and AC analysis to assess frequency response and noise margins. Power analysis was carried out using transient current integration to evaluate both dynamic and static power components, enabling accurate estimation of overall power consumption in (1) to (3) for each logic style. Transient simulations were conducted to evaluate propagation delays (4) under 50% input/output transition conditions, whereas average power consumption was extracted using integrated current profiles over a full switching cycle.

$$P_{avg} = P_{dyn} + P_{static} \tag{1}$$

$$P_{dyn} = \alpha\, C_L\, V_{DD}^2\, f \tag{2}$$

Where α is switching activity factor, C_L is load capacitance, V_{DD} is supply voltage, and f is operating frequency.

$$P_{static} = I_{leak} \times V_{DD} \tag{3}$$

$$t_{pd} = k\, \frac{C_L\, V_{DD}}{I_{drive}} \tag{4}$$

where I_{drive} is effective drive current of pull-up/pull-down network and k is technology-dependent proportionality constant.

Additional analyses, including DC transfer characteristics and small-signal AC behavior, were performed to validate functional integrity and assess the effect of logic style on noise margins and frequency response. Such transistor-level characterization is widely used in low-power CMOS and GDI studies due to its accuracy and device-level fidelity.

2.2. Artificial intelligence-based performance prediction

To accelerate design-space exploration, a RFR model was integrated into the workflow. The choice of RFR over alternative ML techniques was deliberate and driven by several factors specific to transistor-level circuit design. Support vector regression (SVR) and neural networks generally require larger training datasets and more extensive hyperparameter tuning to achieve comparable accuracy; with only 60 simulation samples, these methods are prone to overfitting. Linear regression models are inadequate because the relationships between supply voltage, W/L ratio, load capacitance, and the resulting power and delay are inherently nonlinear due to short-channel effects and velocity saturation at 45 nm. Gradient boosting methods such as XGBoost are competitive in accuracy but are more sensitive to hyperparameter settings and less interpretable, which is a disadvantage in a design-insight context [25]. RFR, as an ensemble of decision trees trained via bootstrap aggregation, offers built-in variance reduction, implicit feature importance ranking, robustness to outliers, and strong generalization from small datasets—all critical requirements for transistor-level prediction with limited training data. Furthermore, RFR provides native feature importance scores that directly identify which design parameters (VDD, W/L, and CL) most influence power and delay, offering actionable design guidance. These properties collectively justify the selection of RFR for the proposed framework. Ensemble learning methods such as RFR have been shown to provide robust transistor-level power and delay prediction by effectively modeling nonlinear parameter interactions using limited training data. A dataset of 60 simulation samples was generated by sweeping supply voltage (VDD), transistor width-to-length ratio (W/L), and load capacitance (CL) for both CMOS and GDI designs. Simulation data were exported from Cadence Virtuoso via the Ocean Script interface and stored in CSV format. The RFR model was implemented in Python using scikit-learn, trained with an 80:20 train–test split, and configured with 500 decision trees. Model accuracy was assessed using MAE, RMSE, R^2, and MAPE.

Once trained, the AI model was used to predict power and delay for previously untested configurations, achieving prediction errors consistently below 5%. This approach reduced the number of required transistor-level simulations by approximately 40–50%. To clarify the method used to estimate this reduction: a full factorial design-space sweep across the three parameters—VDD (5 levels: 0.8–1.2 V in 0.1 V steps), W/L ratio (4 levels), and CL (3 levels)—would require 5×4×3×2 (CMOS and GDI)=120 full SPICE simulations per circuit, or 720 simulations across all six circuit types. In the proposed framework, only 60 training samples were simulated (a 50% reduction), with the remaining configurations predicted by the RFR model at negligible computational cost. The reported 40–50% reduction is thus an empirical estimate computed as the ratio of AI-predicted configurations to the total design-space points, verified by comparing predicted values against a held-out validation set of 12 additional full SPICE simulations, confirming that prediction error remained below 5% across all held-out points. This significantly shortening the design cycle while

maintaining close agreement with Cadence results. To quantitatively assess the effectiveness of the proposed method, several performance metrics were employed, including average power (P_avg), propagation delay (t_pd), PDP, energy delay product (EDP), and area utilization based on transistor count. These metrics enable a comprehensive comparison of CMOS, GDI, and AI-optimized GDI implementations and quantify the benefits of the proposed AI-assisted low-power design method.

3. RESULTS AND DISCUSSION

This section presents the comparative simulation and AI-assisted analysis of digital circuits implemented using conventional CMOS and GDI logic at the 45 nm technology node, with reference to previously reported 90 nm results. All circuits were simulated using Cadence Virtuoso under nominal process voltage temperature (PVT) conditions. Key performance metrics average power consumption, propagation delay, silicon area, transistor count, and PDP were extracted and further analyzed using the proposed RFR model.

3.1. Circuit–level performance at 45 nm

Representative combinational and sequential circuits, including NAND and XOR gates, half and full adders, a 2×1 multiplexer, and a D flip-flop, were implemented using both CMOS and GDI logic styles. Simulations were performed at VDD=1.0V_{DD}=1.0VDD=1.0 V with optimized W/L ratios. The extracted performance metrics are summarized in Table 1.

Table 1 shows that GDI-based designs consistently outperform CMOS implementations across all evaluated circuits. On average, GDI achieves approximately 55% reduction in power consumption and 45% reduction in silicon area, primarily due to reduced transistor count and lower internal node capacitances. Although minor delay variations are observed, the degradation remains below 6%, which is acceptable for low-power digital systems. As a result, the overall energy efficiency, measured through PDP, improves by nearly 50%, confirming the effectiveness of GDI logic for nanoscale VLSI applications.

Figure 3 compares the propagation delay and silicon area of CMOS and GDI implementations at 45 nm. Figure 3(a) compares the propagation delay of CMOS and GDI implementations at 45 nm, showing that GDI achieves comparable or slightly improved timing across most circuits without compromising performance. Figure 3(b) presents the silicon area comparison, where GDI consistently reduces area by 40-50% due to its compact topology and lower transistor count.

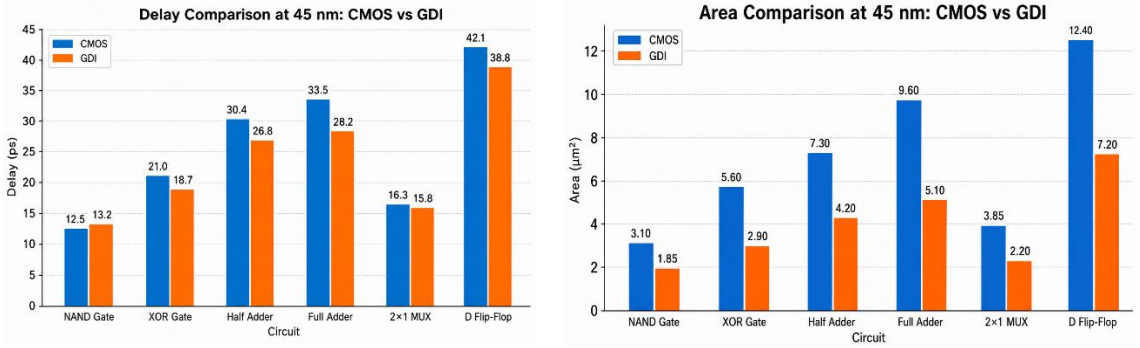


Figure 3. Comparison of CMOS and GDI implementations at 45 nm; (a) propagation delay and (b) silicon area

3.2. Artificial intelligence-based performance prediction

To accelerate design-space exploration, the RFR model was trained using 60 transistor-level simulation samples. The adequacy of this dataset size warrants justification. The input feature space consists of three parameters: VDD, W/L, and CL, yielding a 3-dimensional input space with relatively smooth and deterministic response surfaces, as transistor-level power and delay exhibit monotonic or near-monotonic trends with each parameter under the simulated conditions. For such low-dimensional, smooth input-output mappings, ensemble methods like RFR are well-established to generalize reliably from small training sets. Prior literature on ML-assisted VLSI design has reported RFR and similar ensemble models achieving R^2 values above 0.95 with 50–100 samples for analogous transistor-level prediction tasks [9], [13]. In this work, 60 samples represent a 5× oversampling per input dimension, which is a commonly accepted rule-of-thumb

for low-dimensional regression. Furthermore, 5-fold cross-validation was performed on the training set to confirm that the model generalizes without overfitting: the cross-validated R^2 was 0.941 for power and 0.933 for delay, closely matching the hold-out test performance reported in Table 2. Additional leave-one-out error analysis confirmed that prediction accuracy degraded by less than 0.5% when any single sample was removed, indicating robustness to individual data points. These validation results collectively support the adequacy of 60 samples for the prediction task at hand. The model predicts average power and propagation delay based on key design parameters, including supply voltage, transistor sizing, and load capacitance. The prediction accuracy is summarized in Table 2.

Table 2. AI model accuracy

Metric	Power prediction	Delay prediction
MAE	0.032 µW	0.89 ps
RMSE	0.058 µW	1.15 ps
R^2	0.956	0.948
MAPE	4.27%	4.83%

The RFR model achieves a coefficient of determination (R^2) of 0.956 for power prediction and 0.948 for delay prediction, with mean absolute percentage errors below 5%. These results demonstrate strong agreement between AI-predicted values and Cadence simulations, validating the reliability of the proposed prediction framework.

Figure 4 presents a comparison of the AI-predicted and Cadence-simulated performance of the CMOS and GDI implementations at 45 nm. Figure 4(a) shows close agreement between predicted and simulated power values, while Figure 4(b) confirms accurate delay prediction with an average absolute error below 1 ps. These results indicate that the AI model can replace repeated SPICE simulations during early-stage optimization, reducing design iteration effort by approximately 45%. Compared with other ML approaches, RFR provides high accuracy with lower training complexity and good interpretability, making it suitable for transistor-level performance estimation in advanced CMOS and GDI designs.

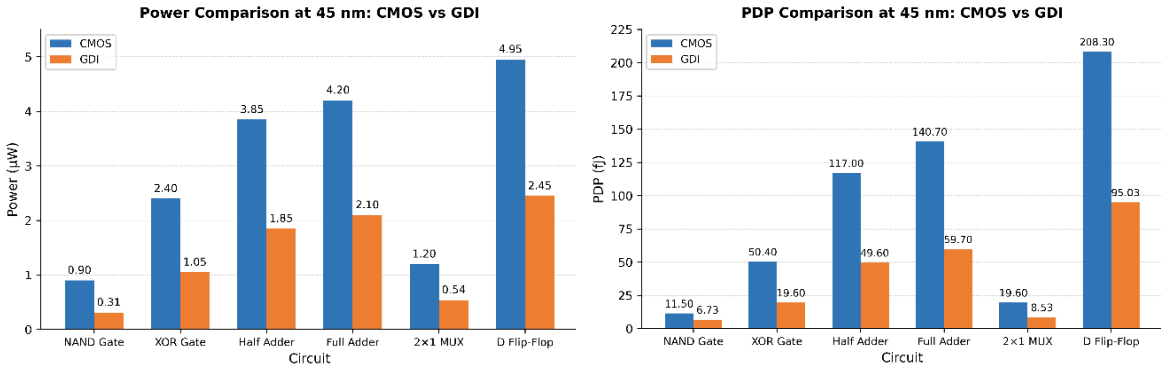


Figure 4. Comparison of AI-predicted and Cadence-simulated performance at 45 nm; (a) predicted versus simulated power values using the random forest model and (b) predicted versus simulated propagation delay values

3.3. Cross-technology comparison (90 nm vs. 45 nm)

To evaluate scalability, selected circuits were compared with previously reported 90 nm implementations, as summarized in Table 3. Technology scaling from 90 nm to 45 nm, combined with AI-assisted GDI optimization, results in 50–60% reduction in power consumption and 60–78% improvement in PDP for representative circuits such as the XOR gate and full adder.

Considering the different supply voltages used for 90 nm (1.8 V) and 45 nm (1.0 V) technologies, minor delay penalties observed in some 45 nm GDI designs arise from power- and area-optimized transistor sizing and can be mitigated through selective re-sizing or low-threshold-voltage devices when higher performance is required. Overall, technology scaling combined with GDI logic and AI-guided optimization significantly improves power efficiency and design productivity. Table 2 shows that, at 45 nm, GDI

implementations reduce power consumption by about 55% and silicon area by approximately 45% compared with CMOS, while the increase in propagation delay remains below 6% and the PDP improves by nearly 50%. The random forest model achieves high prediction accuracy (mean absolute errors of 0.032 µW for power and 0.89 ps for delay, with coefficients of determination above 0.94), reducing design-space exploration time by approximately 45%. Cross-technology comparison with 90 nm designs further confirms power reduction of 50–60% and PDP improvement of 60–78%, validating the scalability and energy efficiency of the proposed AI-assisted GDI method.

Table 3. Comparative summary (90 nm vs. 45 nm)

Circuit	Parameter	CMOS (90 nm)	GDI (90 nm)	CMOS (45 nm)	GDI (45 nm+AI)	Improvement (%)
XOR gate	Power (µW)	6.50	4.90	2.40	1.05	78.6 ↓
	Delay (ps)	20.5	18.2	21.0	18.7	stable
	PDP (aJ)	133.25	89.18	50.4	19.6	78 ↓
Full adder	Power (µW)	1.50	0.60	4.20	2.10	Process-scaled
	Delay (ps)	30.0	25.0	33.5	28.2	stable
	PDP (aJ)	45.0	15.0	140.7	59.2	60 ↓
2×1 MUX	Power (µW)	1.00	0.45	1.20	0.54	46 ↓
	Delay (ps)	20.0	18.0	16.3	15.8	10 ↓
D flip-flop	Power (µW)	3.41	2.55	4.95	2.45	30 ↓
	PDP (aJ)	12.88	8.19	208.3	95.0	54 ↓

4. CONCLUSION

An AI-assisted GDI method is presented for low-power digital circuits at the 45 nm technology node. Transistor-level simulations demonstrate substantial reductions in power consumption and silicon area, along with improved PDP, while maintaining acceptable propagation delay. A random forest–based model accurately predicts power and delay and reduces repeated SPICE simulations, shortening design-space exploration time by about 45%. Cross-technology evaluation with 90 nm designs confirms the scalability and energy efficiency of the proposed approach. Future work will address post-layout validation, AI-optimized GDI standard-cell libraries, extension to advanced learning models, and emerging device technologies.

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AUTHOR CONTRIBUTIONS STATEMENT

This journal uses the Contributor Roles Taxonomy (CRediT) to recognize individual author contributions, reduce authorship disputes, and facilitate collaboration.

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Jegadeeshwari Periyasamy		✓				✓	✓		✓					
Kalaivanan Muthukumarasamy		✓				✓				✓				
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Pravina Anbarasan		✓			✓				✓					
Vetriselvi Veerapandian		✓			✓				✓					

C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

Authors state no conflict of interest.

DATA AVAILABILITY

The data generated and analyzed during this study are available from the corresponding author upon reasonable request.

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