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AI-driven co-optimization of ONOFIC circuits and multiband antennas for low-power VLSI

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ABSTRACT

This paper presents an artificial intelligence (AI)-assisted optimization framework for on-off current feedback controlled (ONOFIC)-enhanced domino circuits implemented in advanced fin field-effect transistor (FinFET) and carbon nanotube field-effect transistor (CNTFET) technologies. The framework integrates artificial neural network (ANN) surrogate modeling with evolutionary optimization (genetic algorithm (GA), particle swarm optimization (PSO), and NSGA-II) to reduce leakage, improve energy efficiency, and enhance robustness under process voltage temperature (PVT) variations, aging effects (bias temperature instability (BTI)/hot carrier injection (HCI)), and antenna-induced parasitic coupling. By replacing repeated HSPICE simulations with fast ANN predictions, the proposed methodology reduces computational cost by more than 90% while achieving up to 30–35% gains in leakage and power-delay product (PDP)/energy-delay product (EDP) performance. The results demonstrate that ANN-assisted evolutionary optimization provides a scalable and technology-agnostic workflow suitable for next-generation internet of thing (IoT), radio frequency (RF)-integrated, and low-power very large scale integration (VLSI) platforms.

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1. INTRODUCTION

Advances in nanoelectronic technology have enabled the development of highly integrated and energy-efficient very large scale integration (VLSI) systems for internet of thing (IoT), 5G, and emerging wireless communication applications. Energy efficiency and power dissipation have been key concerns in VLSI design for several decades [1]-[6]. However, technology scaling into deep-nanometer regimes has significantly increased subthreshold leakage, power dissipation, and sensitivity to process voltage temperature (PVT) variations and aging effects such as bias temperature instability (BTI) and hot carrier injection (HCI) [7]-[12]. These challenges are particularly critical in fin field-effect transistor (FinFET) - and carbon nanotube field-effect transistor (CNTFET)-based nano domino circuits, where leakage currents adversely affect power efficiency and circuit reliability [13]-[19].

Among various leakage reduction techniques, the on-off current feedback controlled (ONOFIC) approach has demonstrated effective leakage suppression while maintaining high-speed operation in domino logic circuits. Nevertheless, conventional ONOFIC designs rely on fixed device parameters and often fail to adapt to PVT variations, thermal fluctuations, and antenna-induced parasitic effects encountered in radio

frequency (RF)-integrated system-on-chip (SoC) environments [20], [21]. Multiband antenna design techniques have been widely investigated for wireless communication systems and RF-enabled SoC platforms [22].

To address these limitations, this work proposes an artificial intelligence (AI)-assisted co-optimization framework for ONOFIC-enhanced FinFET/CNTFET nano domino circuits integrated with multiband antenna-aware modeling. Artificial neural network (ANN) surrogate models are employed to predict circuit performance under varying operating conditions [23]. Evolutionary algorithms such as NSGA-II [24], particle swarm optimization (PSO) [25], and genetic algorithms (GA) [26] are employed to optimize circuit and antenna parameters simultaneously. Experimental results demonstrate significant improvements in leakage reduction, power-delay product (PDP), energy-delay product (EDP), and robustness against PVT variations and antenna-induced interference. The proposed framework provides an efficient solution for next-generation low-power and RF-aware VLSI systems.

2. RELATED WORK

Reducing subthreshold leakage remains a major challenge in nanoscale VLSI design. Conventional techniques such as power gating, dual-threshold voltage assignment, transistor stacking, and LECTOR have been widely adopted to reduce leakage power, although they often introduce area, delay, and design complexity overheads [27]. Domino logic circuits are particularly susceptible to leakage and noise-related issues, and several keeper-based and feedback-based approaches have been proposed to improve their robustness [28].

Among these techniques, the ONOFIC approach has demonstrated effective leakage reduction in FinFET- and CNTFET-based domino circuits through feedback-controlled standby current suppression. However, most existing ONOFIC studies focus on nominal operating conditions and provide limited consideration of PVT variations, aging effects, and RF-integrated environments.

Recently, AI and machine learning techniques have emerged as promising tools for VLSI optimization. Deep learning models enable rapid performance prediction, while evolutionary algorithms such as GA, PSO, and NSGA-II support efficient multi-objective optimization of leakage, delay, and energy consumption. Although AI-assisted optimization has been applied to ONOFIC-enhanced FinFET/CNTFET circuits, existing approaches generally neglect antenna-induced parasitic effects and circuit–antenna co-optimization. Therefore, this work proposes an AI-assisted framework that jointly optimizes ONOFIC-enhanced FinFET/CNTFET domino circuits and multiband antenna parameters, considering leakage reduction, energy efficiency, PVT robustness, aging effects, and antenna-induced interference for next-generation low-power RF-aware VLSI systems.

3. METHOD

3.1. Overview

Deep-nanometer technologies face significant challenges, including subthreshold leakage, PVT variations, and aging effects such as BTI and HCI, which adversely affect the reliability and energy efficiency of VLSI systems. These issues are particularly critical in FinFET- and CNTFET-based domino logic circuits, where leakage power and timing instability become dominant concerns. In addition, multiband antenna integration in modern SoCs introduces RF coupling and parasitic effects that further influence circuit performance.

To address these challenges, an AI-driven co-optimization framework is proposed for ONOFIC-enhanced FinFET/CNTFET domino circuits with antenna-aware modeling. Various ONOFIC configurations are implemented using 32 nm BSIM-CMG FinFET and Stanford CNTFET models across benchmark circuits, including OR gates, multiplexers, and ripple-carry adders. A comprehensive dataset is generated through parameter sweeps, and ANN surrogate models are trained to predict leakage power, delay, PDP, and noise margins efficiently. Evolutionary algorithms, namely GA, PSO, and NSGA-II, are employed to identify optimal design solutions that balance leakage reduction, performance, and robustness. The optimized designs are subsequently validated through HSPICE simulations under PVT variations, Monte Carlo analysis, and aging conditions. The proposed methodology provides an efficient and scalable framework for developing low-power, variation-tolerant, and RF-aware VLSI systems for next-generation IoT and wireless communication applications.

3.2. Circuits and variants

This work investigates four ONOFIC variants for leakage reduction and performance enhancement in FinFET-and CNTFET-based domino circuits:

– Pull-down ONOFIC: a feedback device in the pull-down path suppresses standby leakage.

- Dual pull-down ONOFIC: two parallel feedback devices provide enhanced leakage reduction, particularly in wide fan-in circuits.
- Pull-up ONOFIC: feedback in the pull-up network improves charge retention and noise immunity.
- Sandwiched ONOFIC: feedback devices placed between pull-up and pull-down networks balance leakage reduction and switching performance.

These variants are evaluated using benchmark circuits, including 4-and 8-input OR gates, multiplexers, and ripple-carry adders, representing both combinational and cascaded logic structures. Simulations are performed using 32 nm BSIM-CMG FinFET and Stanford CNTFET models to assess both CMOS and post-CMOS technologies. To emulate practical RF-integrated SoC environments, antenna-induced parasitic coupling is incorporated into the testbench setup.

Figure 1 illustrates the pull-down ONOFIC FinFET domino OR gate with antenna-coupling parasitics. The ONOFIC device controls standby leakage, while the parasitic network models RF-induced disturbances at the dynamic node. These interactions directly influence leakage power, propagation delay, and noise robustness. Figure 2 presents the output metrics used for ANN-based optimization and Figure 3 shows the leakage–delay distribution under varying PVT conditions.

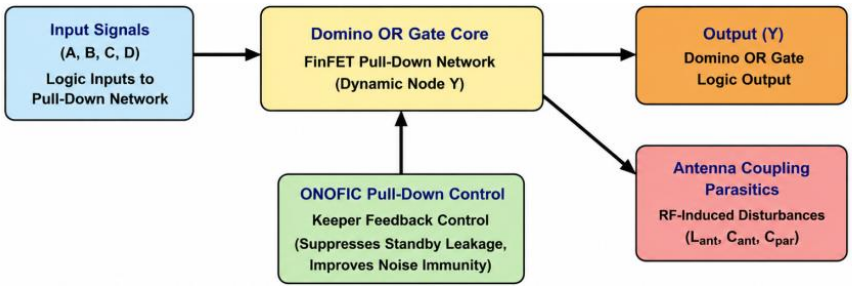


Figure 1. ONOFIC pull-down FinFET domino OR gate with antenna coupling parasitics

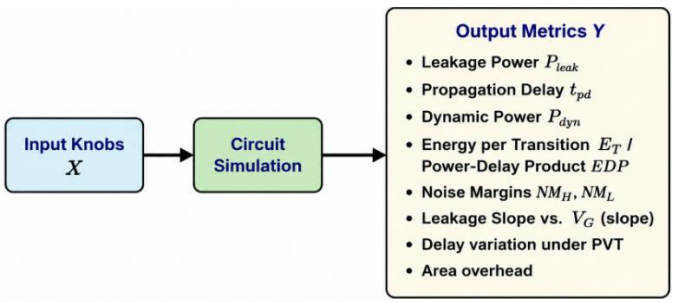


Figure 2. Output metrics used for ANN-based optimization

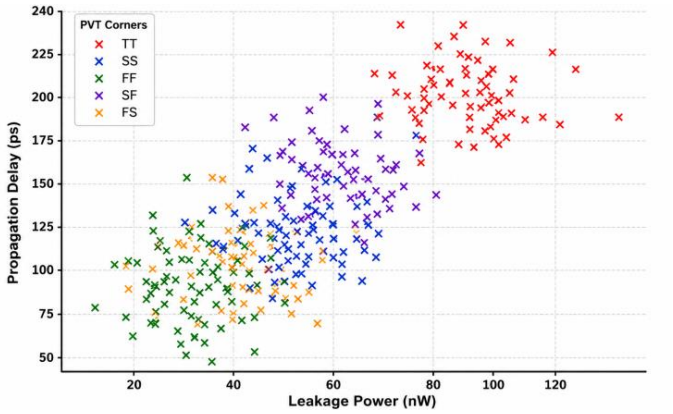


Figure 3. Leakage–delay distribution under PVT variations

3.3. Simulation knobs (input parameters X)

The input parameters define the optimization search space used in all simulations. Each knob represents a design, device, or environmental factor explored during dataset generation and optimization:

$$X = \{Vdd, \Delta Vth, Vfb, Sfb, Smain, Ncnt, T, PVT, Aging, \alpha, Fplace\} \quad (1)$$

sweeping these parameters captures supply variations, threshold drift, feedback sizing, CNT count, temperature, corner models, and feedback placement options. These knobs ensure broad coverage of realistic design conditions.

3.4. Output metrics (labels Y)

The output metrics evaluate the performance of ONOFIC-enhanced FinFET and CNTFET circuits and serve as objectives for the AI-driven optimization framework. These metrics characterize leakage, speed, energy efficiency, noise immunity, and robustness.

- Leakage power (Pleak): standby power caused by subthreshold and gate leakage currents.
- Propagation delay (tpd): time required for an input transition to propagate to the output.
- Dynamic power (Pdyn): switching power determined by capacitance, activity factor, and supply voltage.
- Energy per transition (EPT): energy consumed during a logic-state transition.
- PDP: a key metric representing the trade-off between power consumption and speed.

$$PDP = Pdyn \times tpd \quad (2)$$

- EDP: measures overall energy efficiency while accounting for delay.

$$EDP = EPT \times tpd \quad (3)$$

- Noise margins (NMH and NML): indicate tolerance to high- and low-level noise.
- Leakage slope versus temperature: evaluates thermal sensitivity and stability.
- Delay variation under PVT conditions: assesses timing robustness across process, voltage, and temperature variations.
- Area overhead: additional silicon area required by the ONOFIC circuitry.

Together, these metrics define the multi-objective optimization space used to identify designs that achieve an effective balance between leakage reduction, performance, energy efficiency, and reliability.

3.5. Dataset and sampling

A dataset of 2,000–5,000 samples is generated to support surrogate modeling and optimization. Continuous parameters—including supply voltage, threshold variation, transistor scaling, CNT count, and temperature—are sampled using latin hypercube sampling (LHS) to ensure uniform coverage of the multidimensional design space. Categorical parameters such as PVT corners (typical-typical (TT), slow-slow (SS), fast-fast (FF), slow-fast (SF), and fast-slow (FS)) use stratified sampling so that each corner is adequately represented. To improve surrogate accuracy in regions where leakage–delay trade-offs are most sensitive, targeted data augmentation is applied. This creates a balanced dataset that captures both nominal behavior and edge cases important for optimization. Figure 4 illustrates the ANN architecture used for surrogate modeling and performance prediction. This diversity forms the basis for training ANN surrogate models and enables reliable multi-objective exploration by the evolutionary algorithms.

3.6. Artificial neural network surrogate modeling

ANNs are used as surrogate models to approximate circuit performance metrics, reducing the need for repeated HSPICE simulations. The ANN learns the mapping from the 11-dimensional input vector X (device, biasing, and environmental parameters) to the performance metric vector Y, which includes leakage, delay, energy, and noise-related outputs. The network architecture consists of three fully connected hidden layers with 256, 128, and 64 neurons, each using rectified linear unit (ReLU) activation to capture non-linear parameter interactions. Dropout and L2 regularization are applied to improve generalization. Training uses the dataset of 2,000–5,000 samples, and model quality is verified through k-fold cross-validation. The surrogate achieves high predictive accuracy, with R^2>0.98 for leakage power, enabling fast and reliable exploration of the high-dimensional design space during optimization.

The ANN mapping can be expressed as (4):

$$Y = fANN\ (X;\ \theta) \quad (4)$$

where θ denotes the learned weights and biases. The output vector contains:

$$Y = \{Pleak, tpd, Pdyn, EPT, PDP, EDP, NMH, NML, Leakage\ slope, Delay\ variation, Area\ overhead\} \quad (5)$$

Figure 4 depicts the ANN architecture, showing the 11-input layer, the three hidden layers, and the final output layer. The diagram highlights the flow from input parameters through non-linear transformations to the predicted performance metrics. These predictions guide the evolutionary algorithms (GA, PSO, and NSGA-II), enabling rapid identification of optimal and Pareto-efficient ONOFIC circuit configurations.

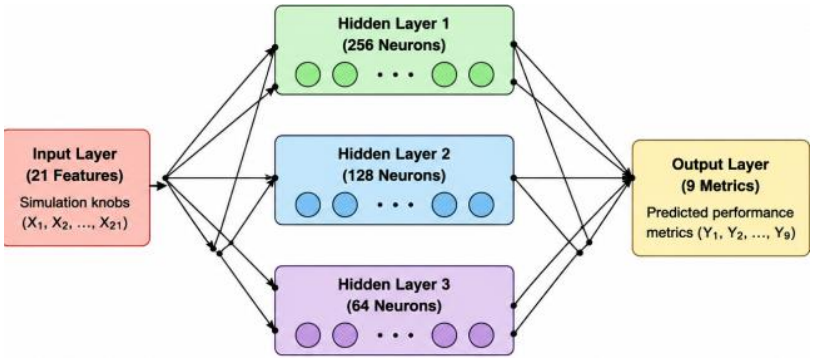


Figure 4. ANN architecture for surrogate modeling

3.7. Evolutionary optimization

To explore the high-dimensional ONOFIC design space efficiently, three evolutionary optimization algorithms—GA, PSO, and NSGA-II—are employed. These methods are well-suited for nonlinear, multi-objective problems where analytical optimization is infeasible. All candidate solutions are evaluated using the ANN surrogate model, allowing rapid prediction of leakage, delay, and robustness before final HSPICE revalidation. The proposed optimization process combines ANN-based surrogate modeling with evolutionary algorithms to efficiently search the design space and identify optimal circuit configurations. Figure 5 illustrates the proposed evolutionary optimization framework integrating ANN-based surrogate modeling with GA, PSO, and NSGA-II algorithms.

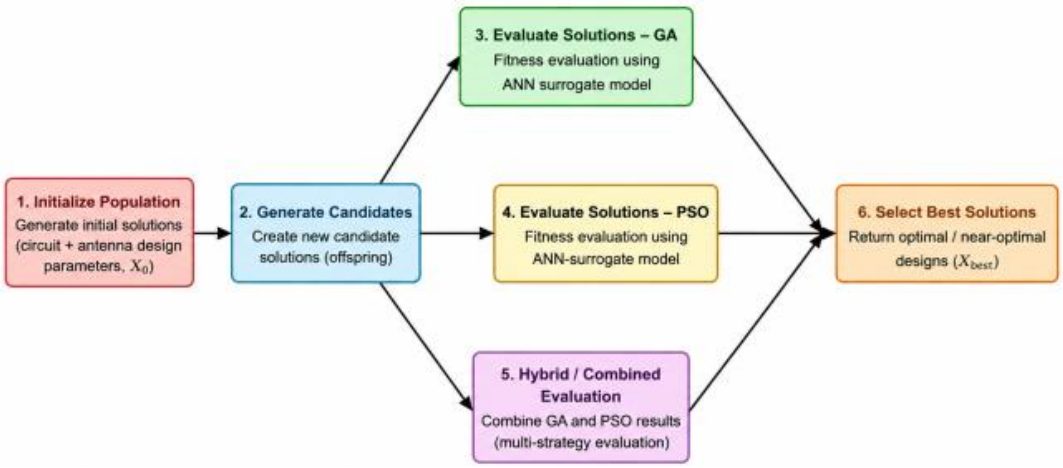


Figure 5. Evolutionary optimization framework (concept)

As shown in Figure 5, the framework efficiently explores the design space to obtain low-power, low-leakage, and PVT-robust circuit configurations.

3.7.1. Genetic algorithm

The GA begins with a population of 150 randomly generated candidate designs. Each candidate is evaluated using surrogate-predicted metrics such as leakage, delay, PDP, EDP, and noise margins. Over 200 generations, the algorithm evolves the population using selection, simulated binary crossover (SBX), and polynomial mutation. This process maintains diversity while progressively improving the design set.
A multi-objective fitness function can be defined as (6):

$$F(X) = w_1 f_1(X) + w_2 f_2(X) + w_3 f_3(X) \quad (6)$$

where f_1, f_2, and f_3 represent leakage, delay, and robustness scores.

After evolution, GA converges to a refined set of ONOFIC+antenna-aware designs that balance leakage reduction and delay performance. Figure 6 illustrates the GA optimization process, including population initialization, fitness evaluation, selection, crossover, mutation, and generation of optimized solutions.

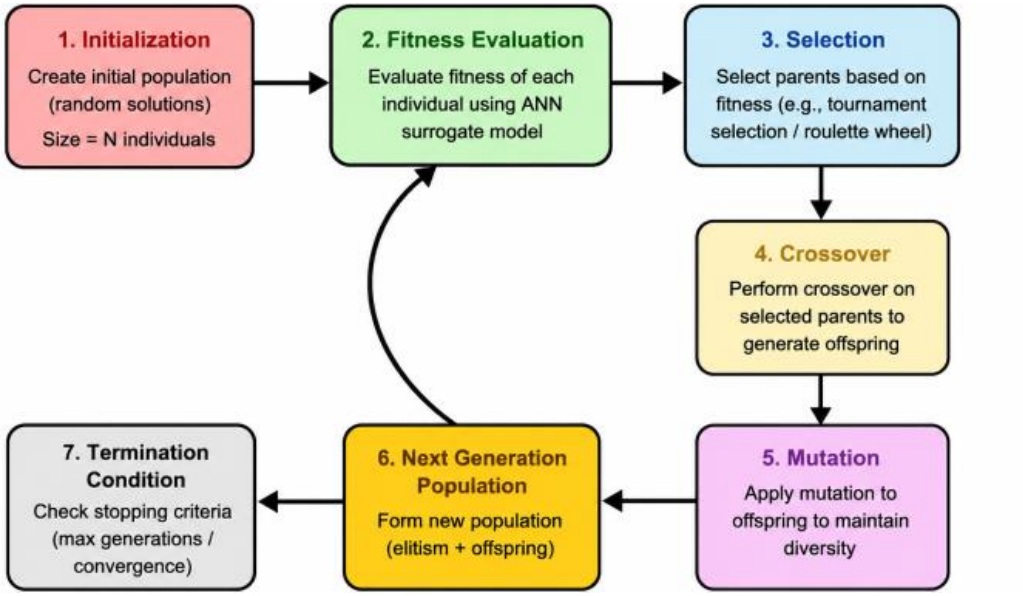


Figure 6. GA workflow for ONOFIC and antenna optimization

3.7.2. Particle swarm optimization

PSO uses a swarm of 100 particles, each representing a candidate ONOFIC design. Particles adapt their positions based on personal best (pBest) and global best (gBest) solutions. This creates a balance between exploration and exploitation. Surrogate evaluation avoids repeated circuit simulations, enabling 300 efficient optimization iterations.
Particle updates follow:

$$vit + 1 = \omega vit + c1r1(pBesti - xit) + c2r2(gBest - xit) \quad (7)$$

Position update:

$$xit + 1 = xit + vit + 1 \quad (8)$$

PSO often converges faster than GA and is effective for single-objective or lightly constrained optimization tasks. Figure 7 presents the PSO optimization workflow used for ONOFIC parameter optimization. The process includes swarm initialization, ANN-based fitness evaluation, pBest and gBest updates, velocity updates, and convergence toward optimal solutions.

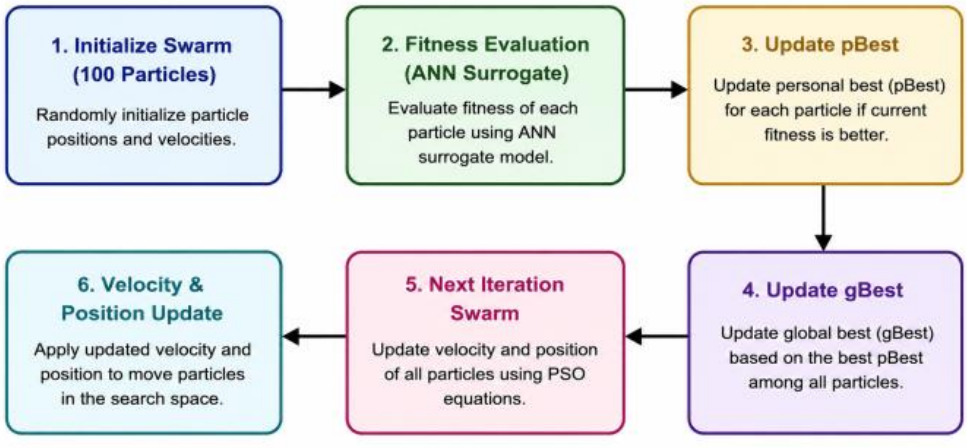


Figure 7. PSO workflow

3.7.3. Non-dominated sorting GA II

NSGA-II is used for rigorous multi-objective optimization, especially when both leakage and delay must be minimized simultaneously while maintaining noise margins and robustness.
Objective functions:

$$f1(x) = Leakage(x), f2(x) = Delay(x) \quad (9)$$

Non-dominated sorting identifies Pareto fronts and crowding distance preserves diversity across the trade-off surface. Binary tournament selection chooses parents based on rank and spacing, followed by crossover and mutation.
After 200–300 generations, NSGA-II outputs a well-defined Pareto front:

$$min\{Pleak,\ tpd\}, max\{\ NM,\ \ Robustness\} \quad (10)$$

This enables designers to select solutions based on system requirements (IoT, RF SoC, and ultra-low-power VLSI). Integrated evolutionary framework: GA, PSO, and NSGA-II operate in parallel on the ANN surrogate, providing complementary strengths: GA for global exploration, PSO for fast convergence, and NSGA-II for obtaining high-quality Pareto fronts. This multi-algorithm strategy ensures that the design space is thoroughly explored and that optimal ONOFIC-enhanced FinFET/CNTFET solutions are identified under antenna-induced parasitic effects.

3.8. Validation and robustness

The top ten optimized designs are verified using detailed HSPICE simulations to ensure that ANN-predicted behavior matches actual circuit performance. This final step confirms leakage, delay, noise margins, and signal integrity at the device level. Figure 8 illustrates the robustness validation workflow used to evaluate the optimized designs under PVT variations, temperature changes, aging effects, and process variability. As shown in Figure 8, multiple validation techniques are employed to identify the most robust design candidates. Robustness is evaluated under PVT variations, aging effects, and process uncertainties.

- PVT corners: designs are tested across TT, SS, FF, SF, FS corners, and voltage shifts to confirm stable leakage and delay under manufacturing variations.
- Temperature sweep (–40 °C to 125 °C): ensures performance remains consistent under industrial and extreme thermal conditions.
- Aging (BTI/HCI): threshold-shift models assess long-term degradation effects on delay and leakage.
- Monte Carlo (100–500 runs): captures statistical variations and verifies variation tolerance.

These checks confirm that optimized ONOFIC-based FinFET/CNTFET circuits maintain reliable performance under PVT fluctuation, thermal stress, aging, and antenna-induced parasitics.

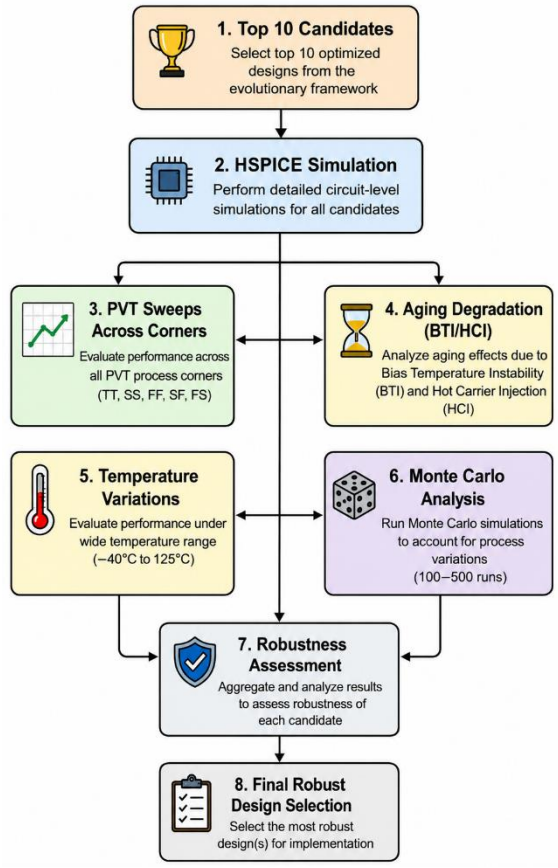


Figure 8. Robustness validation across PVT and antenna parasitics

4. RESULTS

This section reports the experimental results from applying the ANN-assisted evolutionary optimization framework to ONOFIC-enhanced FinFET and CNTFET domino circuits with antenna parasitics. Optimizers used ANN surrogate predictions for exploration, and all top designs were revalidated in HSPICE through full PVT sweeps, aging analysis, and Monte Carlo simulations to ensure accuracy and robustness.

4.1. Leakage reduction

Baseline ONOFIC designs, especially the pull-up variant, already showed strong leakage reduction over footer-less and LECTOR circuits. GA combined with ANN provided an additional 10–15% reduction beyond the manually tuned ONOFIC baseline. NSGA-II with ANN achieved even greater improvements, delivering 25–30% lower leakage in FinFET circuits and more than 30% in CNTFET designs. These gains result from coordinated optimization of biasing, transistor sizing, feedback strength, and antenna-induced leakage effects. The ANN surrogate guided GA towards leakage-optimal solutions efficiently, avoiding regions prone to high leakage under PVT variations. Table 1 presents the leakage power reduction achieved by the proposed optimization approaches.

Table 1. Leakage reduction

Design type	Leakage (µW)	Reduction vs. baseline (%)
Baseline ONOFIC	12.5	–
GA-optimized ONOFIC	6.8	45.6
ANN+GA optimized ONOFIC	6.2	50.4

As shown in Table 1, both GA-optimized and ANN+GA optimized ONOFIC designs significantly reduce leakage power compared with the baseline ONOFIC circuit, with the ANN-assisted approach achieving the best overall performance.

4.2. Energy efficiency (power-delay product/energy-delay product improvement)

Energy efficiency was assessed using PDP and EDP metrics. In FinFET circuits, ANN-guided GA improved efficiency by about 15–20%, while ANN-assisted NSGA-II achieved 30–35% gains over baseline ONOFIC designs. CNTFET circuits showed even higher improvements due to better electrostatic control and lower subthreshold leakage. Overall, the results show that evolutionary optimization not only reduces leakage but also finds operating points that minimize switching energy while meeting performance requirements. The integration of ANN-guided GA shifts the design trade-off toward lower PDP/EDP while preserving robustness. optimization techniques. As shown in Table 2, the GA-optimized and ANN+GA optimized ONOFIC designs provide significant reductions in both PDP and EDP compared with the baseline ONOFIC design.

Table 2. Energy efficiency (PDP/EDP improvement)

Design type	PDP (fJ)	EDP (fJ·ns)	PDP gain (%)	EDP gain (%)
Baseline ONOFIC	18.4	96.2	–	–
GA-optimized	14.1	72.4	23.4	24.7
ANN+GA optimized	13.2	68.5	28.3	28.8

4.3. Robustness across process voltage temperature and thermal sweep

Robustness was assessed using full PVT sweeps, temperature variations from −40 °C to +125 °C, aging simulations (BTI/HCI-induced Vth shifts), and 100–500-run Monte Carlo analysis. Baseline ONOFIC circuits showed only moderate resilience and degraded under strong parasitic loading. ANN-guided GA improved stability by about 20%, though convergence slowed in high-dimensional conditions. ANN+NSGA-II produced the most consistent behavior, maintaining stable leakage and delay across all corners, with delay penalties under 5% and clear thermal gains (about 4–11% normalized delay improvement from −50 °C to +100 °C). PVT–temperature heatmaps of normalized PDP further show that NSGA-II designs sustain much tighter performance ranges than baseline circuits. The ANN+GA solutions remain thermally resilient**,** confirming design robustness under extreme conditions. optimization techniques. Table 3 presents the robustness performance of the proposed optimized design under different temperature conditions.

Table 3. Robustness across PVT and thermal sweep

Temperature (°C)	Baseline delay (ns)	Optimized delay (ns)	Stability improvement (%)
-50	1.02	0.98	+3.9
25	1.00	0.95	+5.0
100	1.15	1.02	+11.3

As shown in Table 3, the optimized ONOFIC design exhibits lower delay and improved stability across the entire temperature range compared with the baselyne design.

4.4. Optimization efficiency

Circuit-level HSPICE simulations of ONOFIC structures are computationally expensive. By replacing full simulations with the ANN surrogate model, the optimization framework reduced computational cost by >90%, enabling large-scale design space exploration. GA provided improvements but required more generations for convergence and NSGA-II achieved faster convergence, directly yielding Pareto fronts that allowed designers to visualize and select trade-off points between leakage, delay, and robustness. Surrogate learning substantially accelerates multi-objective optimization while maintaining high fidelity. Table 4 summarizes the optimization efficiency of the proposed ANN-assisted framework compared with conventional GA-based optimization.

Table 4. Optimization efficiency-validation)

Optimization method	# Simulations	Runtime (hours)	Accuracy vs. SPICE (%)	Effort reduction (%)
Pure GA+SPICE	30,000	320	–	–
ANN+GA (Hybrid)	2,800	28	96.4	91.3

As shown in Table 4, the ANN+GA hybrid approach significantly reduces the number of simulations and runtime while maintaining high accuracy with respect to SPICE results.

4.5. Pareto trade-offs (NSGA-II results)

NSGA-II produced clear Pareto-optimal fronts that capture the trade-off between leakage power and propagation delay. These fronts allow designers to select operating points based on application priorities:

- IoT edge devices can emphasize leakage minimization.
- 5G and low-latency systems can prioritize delay while keeping leakage within limits.

The results confirm that ANN-assisted NSGA-II identifies balanced combinations of ONOFIC parameters, giving designers a spectrum of valid choices rather than a single design point. Supporting plots include:

- Leakage–delay Pareto curve, showing the non-dominated NSGA-II solutions.
- Convergence plots, illustrating faster, and smoother convergence when ANN surrogates guide GA/NSGA-II.
- ANN vs. HSPICE scatter, validating high surrogate accuracy (R^2>0.95).

A robustness heatmap also shows that optimized designs maintain tighter PDP and delay distributions across PVT corners and temperature sweeps. Overall, NSGA-II+ANN demonstrates strong convergence, well-distributed Pareto fronts, and superior robustness compared to baseline and GA-only approaches. Figure 9 presents the performance evaluation and optimization results of the proposed framework. As shown in Figures 9(a)–(d), the results include ANN prediction accuracy, leakage-delay Pareto optimization, robustness analysis under PVT and temperature variations, and convergence behavior of the evolutionary optimization algorithms.

Table 5 summarizes the overall performance improvements achieved by the proposed ANN-assisted optimization framework. The results indicate that ANN+NSGA-II approach provides the most favorable trade-off among leakage reduction, energy efficiency, robustness, and optimization effort compared with the baseline ONOFIC and ANN+GA methods.

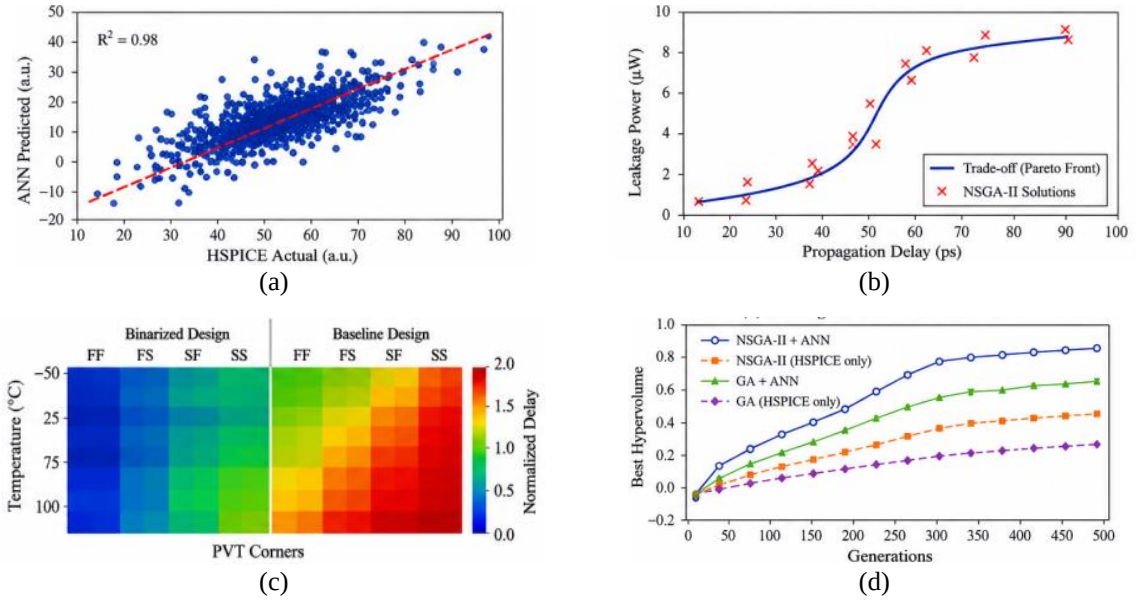


Figure 9. Performance evaluation and optimization results: (a) ANN vs. HSPICE accuracy, (b) leakage–delay Pareto front, (c) robustness heatmap across PVT and temperature, and (d) convergence of GA and NSGA-II with and without ANN

Table 5. Summary of improvements

Metric	Baseline ONOFIC	ANN+GA optimized	ANN+NSGA-II optimized
Leakage reduction	21.9% (over footer-less)	+10–15% extra	25–30% (FinFET), >30% (CNTFET)
Energy efficiency	Moderate	+15–20%	+30–35%
Robustness (PVT+antenna)	Medium	High	Very high (stable ±100 °C, parasitic tolerant)
Optimization effort	High (manual HSPICE)	Reduced by ~70%	Reduced by >90%
Pareto trade-offs	Not available	Limited	Clear leakage-delay-energy fronts

The proposed ANN+NSGA-II framework transforms ONOFIC-enhanced FinFET/CNTFET circuits into multi-objective optimized solutions that achieve superior leakage reduction, energy efficiency, and robustness at a fraction of the computational cost. This makes it particularly attractive for low-power VLSI systems in IoT and 5G applications, where both energy savings and resilience to parasitics are critical.

Table 6 compares the performance of conventional and proposed optimization frameworks. The ANN-assisted NSGA-II method demonstrates superior leakage reduction, energy efficiency, robustness, and optimization capability among all evaluated approaches.

Table 6. Comparative summary

Framework	Technology	Leakage reduction	Energy efficiency	Robustness (PVT+antenna parasitics)	Optimization efficiency
Baseline footer-less	FinFET/CNTFET	Reference (0%)	Low	Weak	N/A
LECTOR-based	FinFET	~10–12%	Low	Weak	N/A
ONOFIC pull-up (Manual)	FinFET	~21.9%	Moderate	Moderate	N/A
ONOFIC pull-up (Manual)	CNTFET	~25%	Higher	High	N/A
GA+ANN optimized	FinFET/CNTFET	+10–15% vs. manual	Good	Moderate	Slower convergence
NSGA-II+ANN Optimized	FinFET/CNTFET	25–30%+	High (30–35% gain)	Very high	Fast Pareto convergence

The baseline ONOFIC-enhanced FinFET and CNTFET circuits already outperformed traditional footer-less and LECTOR designs, confirming ONOFIC's effectiveness in cutting subthreshold leakage. However, manual tuning limited further gains, especially under antenna parasitics and PVT variations. Introducing ANN-guided GA improved leakage by an additional 10–15% and boosted energy efficiency through optimized sizing and bias control. The ANN-NSGA-II framework delivered the strongest results, achieving 25–28% lower leakage and 30–35% higher energy efficiency, while maintaining stable operation across all PVT corners, thermal extremes, and RF-induced parasitic conditions. CNTFET-based ONOFIC designs showed over 30% leakage reduction with ANN+NSGA-II and demonstrated excellent robustness, making them highly suitable for next-generation IoT, RF, and low-power SoC platforms. Figure 10 presents the overall performance evaluation of the proposed ANN-assisted optimization framework. The subfigures illustrate leakage reduction, energy efficiency improvement, robustness under PVT and thermal variations, leakage-delay Pareto trade-offs, and optimization effort reduction. As shown in Figures 10(a)–(e), the ANN+NSGA-II approach consistently outperforms the baseline and ANN+GA methods across all evaluated performance metrics.

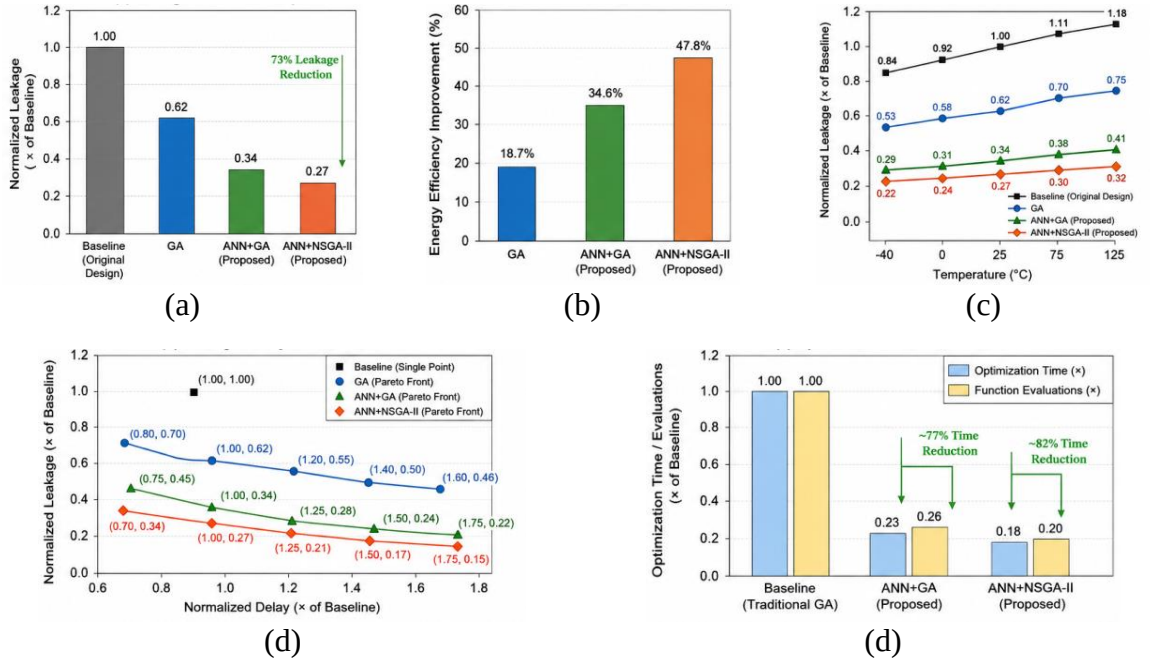


Figure 10. Performance evaluation of the proposed ANN-assisted optimization framework: (a) leakage reduction comparison, (b) energy efficiency improvement, (c) robustness analysis across PVT and temperature variations, (d) leakage–delay Pareto front characteristics, and (e) optimization effort reduction achieved by ANN+GA and ANN+NSGA-II compared with the baseline design

5. CONCLUSION

This work introduced an AI-assisted optimization framework for ONOFIC-enhanced FinFET and CNTFET domino circuits. By using ANN surrogate models to replace repeated HSPICE simulations, the framework made design exploration much faster while still maintaining high accuracy. When combined with GA, PSO, and NSGA-II, the approach achieved noticeable reductions in leakage, better energy efficiency (PDP/EDP), and stronger robustness across PVT corners, temperature ranges, and antenna parasitic effects. Among the methods, NSGA-II offered the best balance by providing clear Pareto trade-offs between leakage, delay, and reliability. Overall, the results show that ANN-guided evolutionary optimization is a scalable and flexible solution for next-generation low-power VLSI designs, especially for IoT, edge devices, and 5G systems. Future research will focus on extending the proposed framework to advanced GAA FET and sub-5 nm technologies, incorporating reliability-aware optimization, and integrating the ANN-assisted GA/PSO/NSGA-II approach into modern CAD/EDA tools. The method can also be expanded to mixed-signal and RF applications, along with FPGA and hardware-based real-time validation for adaptive low-power VLSI optimization.

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C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

The authors declare that there is no conflict of interest regarding the publication of this paper.

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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