International Journal of Reconfigurable and Embedded Systems (IJRES)
Vol. 14, No. 3, November 2025, pp. 696~704
ISSN: 2089-4864, DOI: 10.11591/ijres.v14.i3.pp696-704

The novel single-module communication subsystem architecture for industrial digital inkjet

Maksim Popov[1,2], Aleksandr Romanov[2]
[1]Bigprinter Digital Innovations, LLC, Moscow, Russia
[2]National Research University Higher School of Economics, Moscow, Russia

Article Info

Article history:

Received Jan 9, 2025
Revised Jul 7, 2025
Accepted Aug 7, 2025

Keywords:

Digital inkjet control system
Embedded system
Heterogeneous system-on-module
Optical fiber
Wide format printer

ABSTRACT

The typical challenge in embedded hardware development is the data transfer subsystem. As long as the required speeds are low and high latency is acceptable, there is quite a simple solution with serial bus like controller area network (CAN). In case of high speed (hundreds of megabits per second) with the high temporal determinism, the solution becomes significantly more complicated, requiring expensive components and growing complexity of the embedded software/firmware. We consider industrial inkjet as an example. The device typically includes moving carriage (with printheads) to jet along the media. Existing solutions use optical fiber cable or shielded twisted pair (STP) cable to connect modules. So, additional physical and logical devices are required (for example, for buffering or serial-to-parallel data conversion). For a long time, this approach has no valuable alternative. The novel single-module solution involves abandoning the intermediate high-speed channel. Instead of multiple modules and high-speed communication links between them, the single module is installed near the data destination and connected to the master PC via Ethernet. The functionality of high-speed data transfer subsystem is delegated to the shared dynamic random-access memory (DRAM) and controller, implemented with field-programmable gate array (FPGA) resources. So, the connection cable is not needed anymore and the transfer speed is virtually limited only by DRAM performance.

This is an open access article under the CC BY-SA license.

Corresponding Author:

Maksim Popov
Bigprinter Digital Innovations, LLC
Skladochnaya str. 1/53, 127018 Moscow, Russia
Email: maks@bigprinter.ru

1. INTRODUCTION

The current level of technology development is characterized by a continuous increase in requirements for the performance accuracy of information processing. This inevitably leads to the growth of data volumes and requirements for their transmission speed. This is equally true for both household and professional industrial equipment.

Nowadays industrial equipment is fully coincident with that approach – it typically has multi-module structure with portions of data that need to be transferred between them. If the data volumes are small, then the use of well-known serial buses (SPI, I2C, and CAN) solves the problem. The task becomes much more complex if it is necessary to transmit data at high speeds (hundreds of megabits per second or more) and with minimal latency, which is often found in industry, for example, when controlling actuators. In this case, a specialized intermodule communication channel is usually used.

Let's take an industrial wide-format digital inkjet printer (WFDIP) [1]-[5] as an example (Figure 1). The linear speed of the carriage can reach 2 m/s while printing, and the data flow to the print heads (PH) must be uninterrupted. A typical solution for printer control system (PCS) includes a master personal computer (MPC) and an embedded control system consisting of several modules (Figure 2). This solution involves several high-speed communication channels with intermediate data buffering to prevent any data transfer interruption.

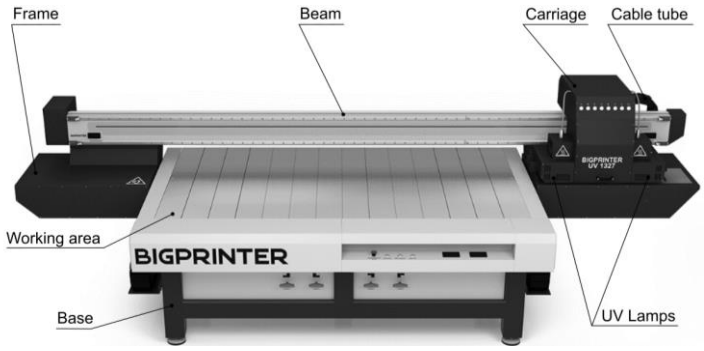


Figure 1. A typical flatbed WFDIP

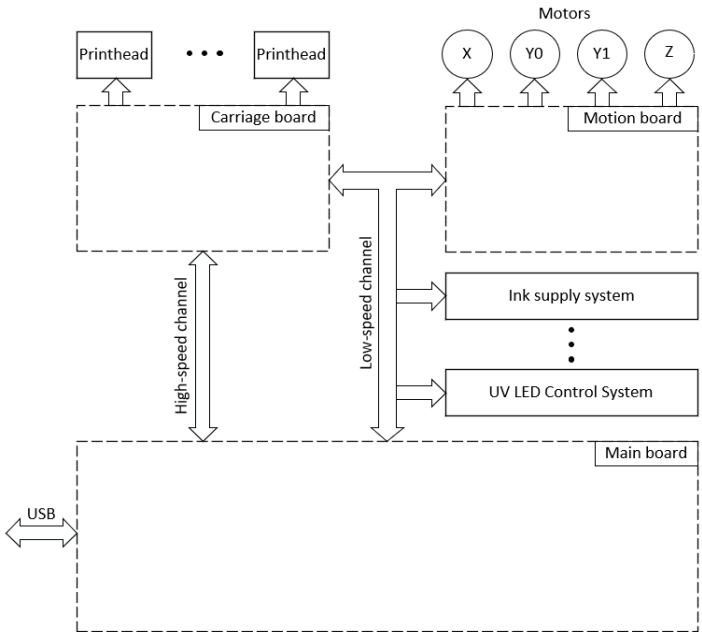
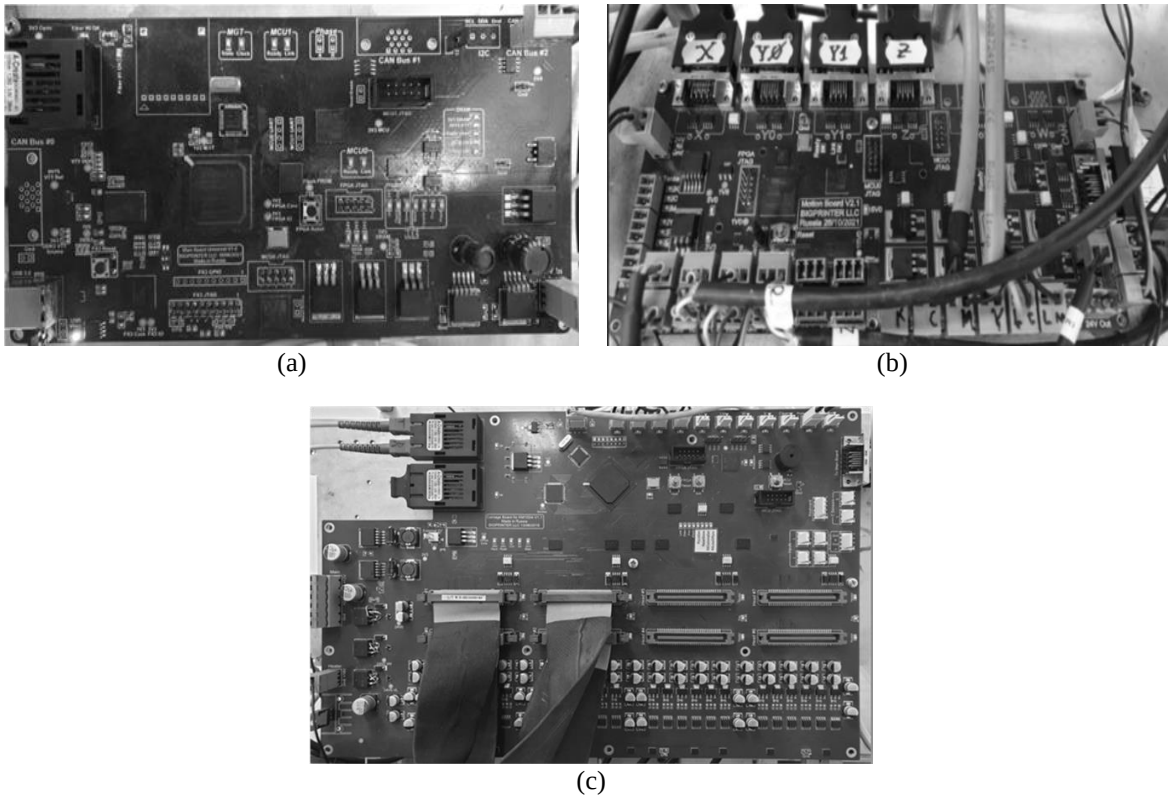


Figure 2. The simplified diagram of a PCS

That multi-channel multi-buffer approach requires a number of complex and expensive software and hardware solutions. Thus, a typical power conditioning system (PCS) implemented according to this scheme (Figure 3) was made using Xilinx Spartan-6 field-programmable gate array (FPGA) with multi-gigabit transceivers [6]-[8]. To communicate with the MPC, a USB 3.0 interface (Infineon CY3014 controller [9]-[11]) is used, and a fiber optic cable is the physical transmission medium [6]. This choice was made according to the high requirements for the wear resistance of the cable, which is subject to continuous bending during a normal printing operation (Figure 1). The required data transfer speed reaches 1.25 Gbit/s or 2.5 Gbit/s, depending on PH quantity and printing resolution.

The previous generation multi-module PCS consists of three main functional units, as shown in Figure 3. The main module (Figure 3(a)) is built around a Spartan-6 FPGA and integrates two STM32 microcontrollers along with a CYUSB3014 USB 3.0 controller, enabling high-speed data processing, synchronization, and inter-module communication. The motion control module (MCM) (Figure 3(b)), implemented using a Spartan-7 FPGA and two STM32 microcontrollers, performs real-time motion

coordination and position feedback for precise mechanical actuation. The printhead module (PM) (Figure 3(c)) employs a Spartan-6 FPGA and a single STM32 microcontroller to manage printhead operation, including timing control, firing sequence generation, and high-speed data transfer from the main module to the print elements.



(a) (b)

(c)

Figure 3. The previous generation multi-module PCS; (a) main module (based on spartan-6 FPGA, two STM32 MCUs and CYUSB3014 as USB 3.0 controller), (b) MCM (based on Spartan-7 FPGA and two STM32 MCUs), and (c) PM (based on spartan-6 FPGA and STM32 MCU)

2. METHOD

The diagram shown in Figure 2 is typical for early WFDIPs. This architecture system with the separate modules (SSM) was the result of the components' performance limitations being existed at that time: so, the calculation load falls on the host PC, while the control system only provides data tunneling to the PH set and the carriage movement control. Each of the PCS tasks was solved by one or more modules, since their structural unification was economically and technologically impractical.

As the electronic components improved, it became possible to implement more than one control system subsystem on one module. This is how a system with combined modules (SCM) appeared – the main module (MM) took over the functions of MCM. This results in a small economic effect, since the most difficult to eliminate bottlenecks are remained unchanged. There were also attempts to implement auxiliary subsystems (for example, ink supply subsystem) on the MM or MCM. As the application field of WFDIP has expanded and the time it takes for new PH models to appear has decreased, the problem of PM adaptation has arisen. The PM PCB has high complexity (usually at least 8 layers with a board size of about 300×400 mm), so its complete redesign is an expensive and time-consuming routine. Therefore, another trend in the development of PCS is a detachment of parts specific to a given PH model to a separate printhead driver module (PDM). The architecture of the SSPD is implemented as a set of separate PDMs while the PM module itself is universal for many PH types. Figure 4 visually presents the stages of PCS evolution. As a result of analysis of the observed evolution trends, we can draw a conclusion about the next stage of development, which logically follows from the previous ones – further unification of modules, up to the transition to a single-module architecture where all the functions, including MPC, are implemented within a single module (SMSEC architecture).

The single module for data receiving and processing is unified and is physically located near the final data consumer–a set of PHs. Despite its apparent simplicity, such a solution has not been used in practice for a long time due to economic infeasibility–the components for its implementation were too expensive, and the firmware was very complex too [12]–[14].

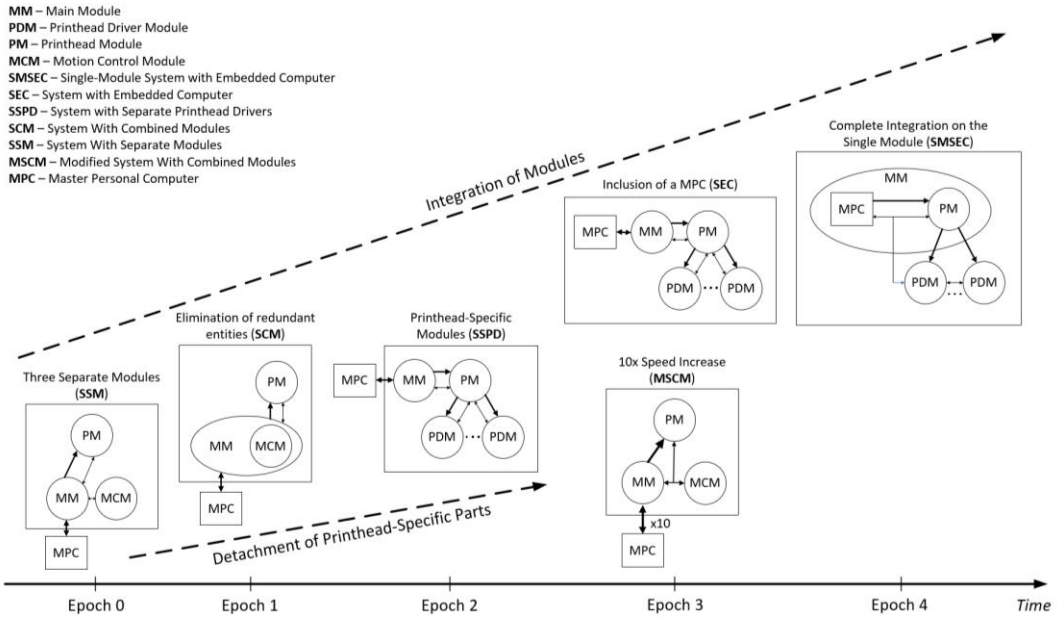


Figure 4. The WFDIP CS evolution

The so-called heterogeneous integral circuits have appeared quity recently, which combining one or more processor cores and FPGA logic resources in a single package. Examples are Intel Cyclone V [15], AMD Zynq-7000 [16], and AMD Zynq Ultrascale+ [17]. They made it possible, on the one hand, to simplify the design of the PCB, and on the other, to increase the flexibility of system configuration, since it became possible to make a significant number of connections inside the chip itself, and not on the printed circuit board.

Despite these advantages, the complexity of PCBs, combined with the high cost of heterogeneous chips, in many cases still did not make their use economically justified. This situation was typical in the most designs, which became obvious to chip manufacturers. Therefore, there has been a tendency towards the production of so-called system-on-module (SoM), which are PCBs with a heterogeneous chip itself, RAM, flash memory, and power supervisor. The ability to connect to the pins of the main chip is provided via multi-pin connectors.

An example of SoM is AMD Kria (Figure 5) [18]-[20], the key characteristics of which are given in Table 1. The combination of low cost and high performance and capabilities made it expedient to use Kria SoM when creating WFDIP and other industrial equipment with a similar architecture.

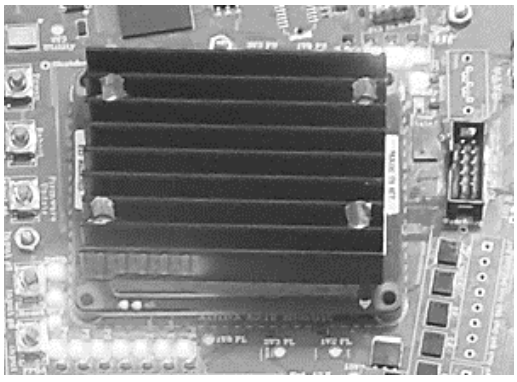


Figure 5. The AMD Kria SoM

Using the AMD Kria SoM, it becomes possible, as mentioned above, to abandon the intermodular transmission channel and the corresponding auxiliary software and hardware components. Moreover, the MPC itself is no longer a necessary part of the PCS, since Kria's hardware resources are sufficient to run a web-server on embedded Linux, which will allow access to WFDIP functions through a web interface or built-in touch screen.

Table 1. The key characteristics of the Kria SoM

Parameter	Value
MPSoC IC	XCK26-SFVC784-2LV
Core type/clock frequency, MHz	4×ARM Cortex-A53/1500 2×ARM Cortex-R5F/600 1×Mali-400 MP2/667
RAM, GBytes	4
ROM, MBytes	512 MBytes (Flash QSPI) 16 GBytes (Flash, eMMC) 64 Kbytes (EEPROM, parallel)
Interfaces	Gigabit Ethernet, DisplayPort, CAN, USB 3.0 Host/Device, PCI Express, SATA, UART, SPI, SD, and I2C
Connectors/pins	2/240
Size, mm	77×60×10.9
Weight, g	58

The roadmap of the function correspondence between an old multi-module PCS and new single-module is shown in Figure 6. Functions previously assigned to individual components within modules are now performed by a single heterogeneous integral circuit, being distributed between the cores of the processor system and the logical resources of the FPGA.

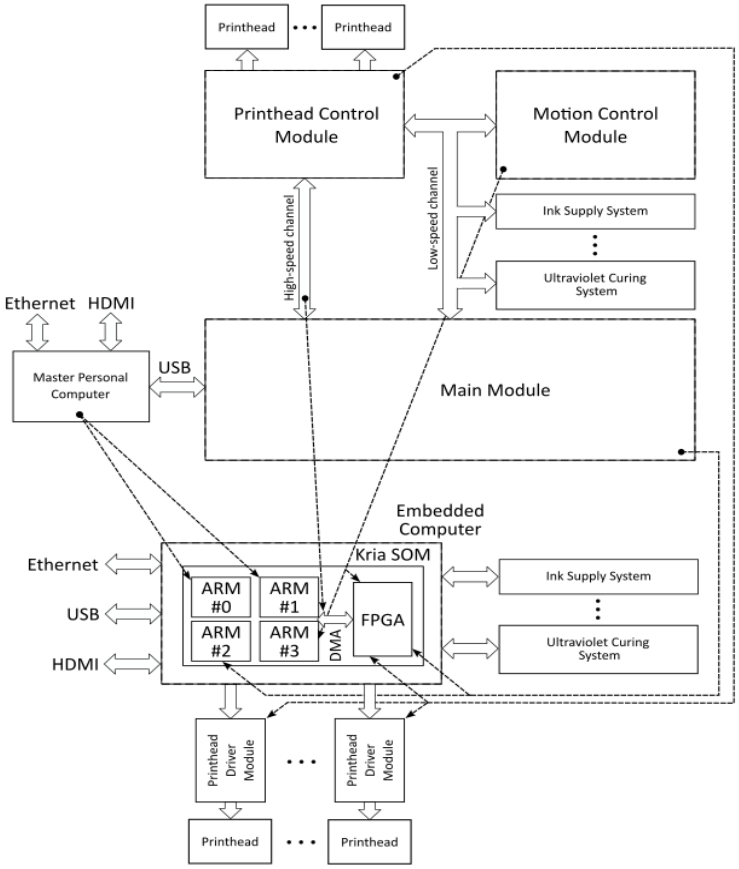


Figure 6. The simplified diagram of conversion from old-style multi-module PCS to the new single-module one (based on Kria SoM)

Thus, the MPC functions are implemented by multiprocessor system-on-chip (MPSoC) cores #0 and #1 – Linux and the user interface application are running on these cores. The main module supervisor is now implemented on core #2, and the MCM supervisor is implemented on MPSoC core #3.

The proposed distribution of functions between the MPSoC components is shown in Figure 7. It is important to note that the functions previously performed by FPGA chips on the main module, motion modules, and PH are also now performed on the FPGA logic resources within the MPSoC.

Another important component of the PCS is the PH control modules Figure 6. In previous PCS PHs were connected directly to the PH control module, which had the appropriate number of connectors (usually 8 or 12). Such a simple, at first glance, solution is not optimal, since a complicated PM is being designed compatible with a single PH model only.

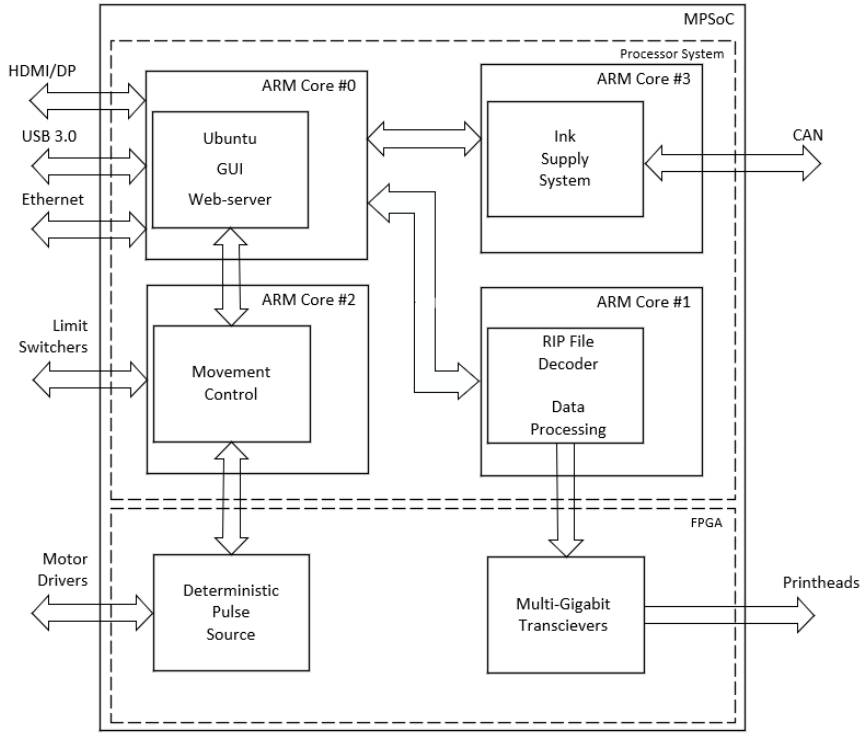


Figure 7. Tasks distribution between MPSoC components

PHs are produced by a number of manufacturers, for example [1]-[3], [21]-[25], who continuously improve their products. Each new PH model is typically incompatible with the previous one from a software and hardware point of view.

This leads to the need to develop a new PM (and in some cases, the main module too) each time, which is an expensive and time-long process that significantly slows down the overall commercial launch period for a WFDIP with a new type of PHs.

The use of a universal PH control module makes it possible to leave unchanged the most complex part of it that provides data exchange with the MM, and to implement technical solutions specific to a particular PH model on separate PDM. In this case, when a new type of PH appears, it is only necessary to develop a driver module. This approach significantly reduces total costs and time requirements. A driver module PCB is relatively simple (typically four layers and size about 100x150 mm) and requires less time to develop and test.

The PDMs are shown in Figure 8. There are two modules currently assembled and installed in the test setup. The module is based on XC7S15-1FTG196 FPGA of AMD Spartan-7 family [26]. This concept fits very well with the transition to a single-board PCS – the connectors for PDMs are located on the carrier board. This solution provides the necessary flexibility and a long-life cycle, which increases the economic effect of the transition to the new type of PCS. In this case, the number of PH connection sockets should be determined by the most typical WFDIP configuration. As already mentioned, the typical number of PHs is 8, since most WFDIPs use the black – cyan – magenta – yellow – light cyan – light magenta – white – varnish

(CMYKLcLmWV) color scheme. Cheaper printer models can use fewer colors, in which case unused sockets simply remain unoccupied. At the same time, it is advisable to provide for the possibility of expanding the functionality of the PCS. For this purpose, high-bandwidth transceivers included in modern MPSoC and FPGA [15]-[17], [25], as well as in the Kria module, should be used.

In addition to the 8 PH control channels available for direct connection on the designed carrier board, there is an additional expansion channel with a total throughput of 25 Gbps, which allows for almost any future needs. The channel includes separate differential lines for transmission, receiving and clock signals.

The physical transmission medium is a coaxial cable. The use of a fiber optic cable is not required in this case, since the PCS is installed directly in the printer's movable carriage and, due to the short distances, the coaxial cable is quite capable of performing its task.

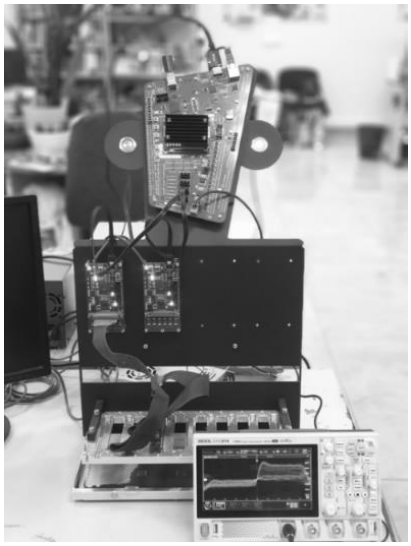


Figure 8. The test setup for PCS based on Kria SoM

3. RESULTS AND DISCUSSION

Thus, a transition has been made from a multi-module version of PCS to a single-module one, auxiliary high-speed communication channels have been eliminated, and the cost of development and production of the control system has been reduced. The transfer speed is about several Gigabits per second for typical multi-module PCS (Figure 2), while the novel PCS uses the shared dynamic random-access memory (DRAM) area for data transfer between MPSoC and FPGA parts of the SoM. So, the transfer speed is only limited by Kria DRAM subsystem theoretical bandwidth which is up to 150 Gbit/s. It covers any current and future needs. At the same time, the technological capability of the final products (printers) was increased, since the number of modules and connections between them has been reduced (cable length reduced for about 90% or at least 20 m in absolute values). The reliability of the control system and entire inkjet device has been also increased. The comparison of key parameters for SSM and SMSEC arcitectures is presented in Table 2.

Table 2. The key parameters comparison for SSM and SMSEC arcitectures

Parameter	PCS arcitecture		The ratio (if applicable)
	SSM (with MPC)	SMSEC	
Application CPU cores			
- Family	x86/x64	Cortex-A53	-
- Quantity	4 or more	4	-
- Clock frequency, GHz	3 or more	1.5	2 or more
- Data width, bits	64	64	1
- Performance per 1 core, MIPS	2096	3450	0.61
Real-time CPU cores	-	2×Cortex-R5 @600 MHz	-
DRAM, size (type)	8 GB or more (DDR4 or DDR5)	4 GB (DDR4)	2
Power consumption, W	600	25	24

The technical implementation details for competitive PCS solutions from other developers are typically covered by NDA, but some key features can be obtained [27]-[30]. The alternative solution for comparable data throughput is based on 10G Ethernet usage (one or more channels in parallel). It requires high-end MPC (most likely with hardware acceleration modules) and the complicated PCS which is able to unite the data from a number of 10G channels, process them and deliver to PH array. The total cost and complexity of such a PCS make it reasonable for a small field of usage, may be, in the textlle industry. Anyway, this approach still also requires intermodular transfer channel with the appropriate throughtput.

The developed system is, in fact, a specialized single-board computer for controlling multi-axis positioning and – at the same time – ensuring continuous high-speed data transfer based on built-in hardware accelerations features (due to FPGA resources with a heterogeneous chip).

Flexibility and expandability of PCS is ensured by support of such interfaces as PCI-Express and SATA. Peripheral devices can be connected via Gigabit Ethernet, USB 3.0, I2C, CAN, and RS-232. Monitors with a resolution of up to 4K are supported as video output devices, and can be connected using displayport and HDMI connectors.

User interaction can be performed either using the regular monitor, keyboard, mouse or touch-screen or via the built-in web server. The latter option makes it possible to include WFDIP in an enterprise local network to provide access via web interface. As a result, s significant economic advantage over traditional systems is achieved by eliminating the need to use a dedicated MPC, expensive and power-consuming.

The scope of application of such a solution is not limited to wide-format printing equipment. It is expected that the system will also be in demand when implementing industrial CNC controllers, as well as for solving other high-precision control tasks in the industrial applications.

Currently, a printed circuit board of the main module has been developed and manufactured, and a prototype has been assembled. The control modules have also been manufactured. Testing and complex debugging are currently underway.

4. CONCLUSION

The proposed single-module solution allows to solve the fundamental problems of multi-module PCS development and production, which are high-speed channels complexity, bandwidth limitation and technological disadvantages. The novel PCS provides virtually unlimited transfer speed for practical needs (up to 100 times faster than earlier systems) and completely eliminates the need of the intermodule high-speed channel. The overall cable length can be reduced for up to 90% depending on the printer type while the total module quantity can be reduced to for up to 40%. The novel PCS prototype is implemented and being tested and evaluated now.

REFERENCES

[1] W. Zapka, "Handbook of Industrial Inkjet Printing: A Full System Approach," *Handbook of Industrial Inkjet Printing: A Full System Approach*, vol. 1–2, pp. 1–908, 2017, doi: 10.1002/9783527687169.

[2] S. D. Hoath, "Fundamentals of Inkjet Printing the Science of Inkjet and Droplets," *Fundamentals of Inkjet Printing the Science of Inkjet and Droplets*, pp. 1–449, 2015, doi: 10.1002/9783527684724.

[3] M. A. Shah, D. G. Lee, B. Y. Lee, and S. Hur, "Classifications and Applications of Inkjet Printing Technology: A Review," *IEEE Access*, vol. 9, pp. 140079–140102, 2021, doi: 10.1109/ACCESS.2021.3119219.

[4] J. Liu *et al.*, "The Design of Digital Inkjet Printing Control System Based on FPGA," in *2023 4th International Conference on Information Science, Parallel and Distributed Systems, ISPDS, IEEE*, pp. 206–210, Jul. 2023, doi: 10.1109/ISPDS58840.2023.10235632.

[5] S. D. Hoath, "Fundamentals of inkjet printing the science of inkjet and droplets," *Fundamentals of Inkjet Printing the Science of Inkjet and Droplets*, pp. 1–449, 2015, doi: 10.1002/9783527684724.

[6] M. Popov, M. Shishova, and A. Romanov, "Method for high-speed fiber optic data transfer channel development using spartan-6 transceivers," in *Proceedings-2023 International Russian Automation Conference, RusAutoCon 2023*, IEEE, pp. 182–186, Sep. 2023, doi: 10.1109/RusAutoCon58002.2023.10272807.

[7] X. Hao, L. Zhan'an, L. Yunpeng, L. Lu, Z. Dixin, and G. Ya'nan, "FPGA based high speed data transmission with optical fiber in trigger system of BESIII," in *IEEE Nuclear Science Symposium Conference Record*, IEEE, pp. 818–821, Oct. 2007, doi: 10.1109/NSSMIC.2007.4436453.

[8] S. Zhou, "Design of novel optical fiber communication electronic system and big data prediction method of its loss," *Journal of Nanoelectronics and Optoelectronics*, vol. 16, no. 8, pp. 1308–1316, 2022, doi: 10.1166/jno.2021.3082.

[9] "EZ-USB FX3^{TM} SuperSpeed USB 3.0 peripheral controller," *Datasheet. 001-52136 (Rev. *Y). Infineon Technologies*, 2022.

[10] M. Popov, M. Shishova, and A. Romanov, "USB 3.0 Based Heterogeneous Data High-Speed Transfer Subsystem," in *Proceedings - 2023 International Ural Conference on Electrical Power Engineering, UralCon 2023*, 2023, pp. 200–204, doi: 10.1109/UralCon59258.2023.10291116.

[11] C. Muscari Tomajoli *et al.*, "USB 3.0 High-Transfer Rate Time-Tagging Module for High-Performance FPGA-based Time-to-Digital Converter," in *2022 IEEE NSS/MIC RTSD - IEEE Nuclear Science Symposium, Medical Imaging Conference and Room Temperature Semiconductor Detector Conference, IEEE*, 2022, pp. 1–4, doi: 10.1109/NSS/MIC44845.2022.10399038.

[12] M. A. Popov, M. S. Mashkovskaya, and A. Y. Romanov, "AMD-Xilinx Kria as a Basis for Industrial Equipment Embedded Control System," *Informacionnye Tehnologi*, vol. 29, no. 2, pp. 98–103, 2023, doi: 10.17587/it.29.98-103.
[13] I. E. Tarasov, "Xilinx Kria SoM-Based Systems (in Russian: *Системa Xilinx Kria на основе SOM*)," *Components and Technologies*, vol. 6, pp. 80–84, 2021.
[14] S. M. Wandkar, D. S. Sanjaya, G. K. Prajwal, and Basawaraj, "Object Tracking System on Zynq UltraScale+ MPSoC ZCU104," in *Lecture Notes in Networks and Systems*, pp. 59–69, 2024, doi: 10.1007/978-981-97-6681-9_6.
[15] Intel, "Cyclone V Device Datasheet CV-51002," *Intel*, pp. 1-94, 2019.
[16] ZYNQ, "Zynq-7000 SoC. Product Selection Guide. XMP097 (v1.3.2)" *AMD-Xilinx, Technical Information Portal*, pp. 1–11, 2019.
[17] ZYNQ, "Zynq UltraScale+ MPSoC. Product Tables and Product Selection Guide. XMP104 (v2.6)" *AMD Xilinx, Technical Information Portal*, pp. 1–9, 2022.
[18] "Kria K26 SOM Data Sheet DS987 *(v1.2)*," AMD-Xilinx, *Technical Information Portal*, 2022.
[19] "Kria SoM Carrier Card. Design Guide. UG1091 (v1.2)," AMD-Xilinx, *Technical Information Portal*, 2022.
[20] Y. Gorbounov and P. Peychinov, "Vision and control capabilities of autonomous systems with the Kria Adaptive System-on-Modules," in *2023 31st National Conference with International Participation, TELECOM 2023*, *IEEE*, Nov. 2023, pp. 1–4, doi: 10.1109/TELECOM59629.2023.10409757.
[21] Konica Minolta Industrial Inkjet, "Konica minolta absorbs industrial inkjet subsidiary," *Official site*, 2013, [Online]. Available: https://www.konicaminolta.com/global-en/inkjethead/products/inkjethead/. (Accessed: Jun. 01, 2025)
[22] "Fuijfilm Industrial Printhead," [Online]. Available: https://www.fujifilm.com/us/en/business/inkjet-solutions/industrial-printheads Official site, 2025. (Accessed: Jun. 01, 2025)
[23] Xaar *Printheads, Official site*. [Online]. Available: https://www.xaar.com/products/xaar-printheads/. (Accessed: Jun. 01, 2025)
[24] Official site, "Epson Inkjet Printheads," 2025. [Online]. Available: https://epson.com/inkjet-printheads. (Accessed: Jun. 01, 2025)
[25] D. Giusti, S. Costantini, S. Brovelli, and M. Ferrera, "Inkjet Printhead," in *Silicon Sensors and Actuators: The Feynman Roadmap*, Cham: Springer International Publishing, 2022, pp. 603–643, doi: 10.1007/978-3-030-80135-9_19.
[26] "7 Series FPGAs Data Sheet: Overview. Product Specification. DS180 (V2.6.1)," *AMD-Xilinx, Technical Information Portal*, pp. 1–19, 2020.
[27] T. Chen, Y. Qi, L. Dong, S. Gao, T. Bao, and R. Zhu, "Structure and Control Strategy Design of Wide-Format Ink-Jet Printing Machine," in *Lecture Notes in Electrical Engineering*, 2022, pp. 306–315, doi: 10.1007/978-981-19-1673-1_46.
[28] D. M. Kumelachew, B. T. Wagaye, and B. F. Adamu, "Digital textile printing innovations and the future," in *Digital Textile Printing: Science, Technology and Markets, Elsevier*, 2023, pp. 241–259, doi: 10.1016/B978-0-443-15414-0.00006-6.
[29] H. S. Kim and J. Suh, "Roll-to-roll printing," in *Smart and Connected Wearable Electronics: Nanomanufacturing, Soft Packaging, and Healthcare Devices, Elsevier*, 2023, pp. 123–152, doi: 10.1016/B978-0-323-99147-6.00008-9.
[30] R. Usai, "MAS+ Technology and the Future of Digital Textile," *Roberto USAI*, vol. 63, no. 1, pp. 88–93, 2024, doi: 10.11370/isj.63.88.

BIOGRAPHIES OF AUTHORS

Maksim Popov is graduated from Samara State Aerospace University (SSAU), Russia in 2003 as Electronics Engineer. He received the Master degree in biotechnical systems and technologies from BIOTECH University in 2025. Now he is the Senior Software Specialist and the Head of R&D Department in BIGPRINTER Digital Innovations, LLC. He is also a part-time teacher and a postgraduate student in the School of Computer Engineering in HSE University, Moscow. He is the author of about 30 scientific and popular science articles and brochures. His research lines are high-speed data processing and transfer, multi-axis motion control and CNC, heterogeneous IC, embedded Linux, and artificial intelligence. He can be contacted at email: maks@bigprinter.ru.

Aleksandr Romanov received the B.S. and M.S. degrees in computer systems and networks from National Technical University Kharkov Polytechnic Institute (NTU KhPI), Kharkov, Ukraine, in 2007 and 2009, respectively; and the Ph.D. degree in technical sciences from the Federal State-Funded Institution of Science Institute for Design Problems in Microelectronics of Russian Academy of Sciences (IPPM RAS), Zelenograd, Russia, in 2015. He received the Dr.Sc. degree in technical sciences from the National Research University Higher School of Economics (HSE University), Moscow, Russia, in 2024. He is currently an Associate Professor with HSE University. He is also a University Teacher of the following subjects: SoC Development, System Design of Electronic Devices, Artificial Intelligence Systems. He is the author of the book Digital Design: Practical Course, and more than 150 scientific articles. His research interests include SoC, NoC, embedded systems, FPGA, and neural networks. He is an IEEE Member and ACM member. He has received numerous awards as the supervisor of students' teams taking part in international competitions in programming, electronics and robotics, as well as the HSE University Best Lecturer Award, in 2018, 2019, 2021, and 2024. He can be contacted at email: a.romanov@hse.ru.