SPARTAN–field programmable gate array implementation for analog waveforms generation by direct digital synthesis

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ABSTRACT

In the last thirty years, low power field programmable gate arrays (FPGAs) becoming more commonly used to implement a countless of applications in different electronics industry domains. Due to their flexible design, strong compatibility, parallel computing, and compared to the CPU architecture, FPGA accentuate computing efficiency and con sidered as one of the devices with the lowest application risk and the shortest development cycle among the variety of available programmable circuits families. This article details the design and implementation of a direct digital synthesis (DDS) signal generator using the Spartan-6 FPGA, focusing on high-quality sine wave generation. The system utilizes look-up tables (LUTs) and Block RAM (BRAM) for efficient storage and retrieval of sine wave data, while an 8-bit DAC0808 digital-to-analog converter (DAC) ensures precise waveform output. The FPGA's reconfigurable architecture allows real-time adjustments of frequency and phase, making the design suitable for various signal processing applications and modulation techniques like binary phase shift keying (BPSK).

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1. INTRODUCTION

In recent years, field pro grammable gate arrays (FPGAs), particularly those in the SPARTAN series, have gained significant traction in digital systems due to their flexibility, performance, and cost-effectiveness, especially in applications like digital signal processing (DSP), communications, and embedded systems. SPARTAN FPGAs, such as the Spartan-7, provide high DSP performance (up to 176 GMAC/s) and are well-suited for real-time applications, where their parallel processing capabilities offer a clear advantage over traditional processors [1], [2]. These devices excel in efficiently handling high-throughput tasks while maintaining low power consumption, making them ideal for embedded systems and communication protocols [1]. Furthermore, the integration of DSP blocks on SPARTAN FPGAs enhances their ability to accelerate computation-heavy processes, such as convolutional neural network (CNN) inference, highlighting their growing importance in modern hardware acceleration [2], [3]. This project emphasizes the FPGA-based generation of analog waveforms using direct digital synthesis (DDS), a technique widely recognized for its ability to produce and delivering precise and stable frequencies across a broad range. DDS allows the generation of various waveforms, such as sine, square, and triangular waves, making it ideal for applications in communication systems, instrumentation, and signal processing [4].

The aim of this project is to implement a signal generator on the SPARTAN FPGA using the DDS technique to create high-quality analog waveforms. By exploiting the parallel processing, reconfigurable architecture, and look-up table (LUT) capabilities of the FPGA, this design provides significant advantages in terms of flexibility, precision, and scalability compared to traditional waveform generators [5]. Additionally, the FPGA's capabilities allow real-time modifications of signal parameters, such as frequency and phase, which are crucial in advanced signal processing applications [6], [7].

To achieve precise control of the output phase during frequency switching transitions and enhance phase noise while improving frequency agility, a non-linear digital design technique is employed [8]. This method generates analog waveforms using stored digital samples from a LUT that contains digital data of a sinusoidal waveform [9], [10]. By sequentially reading these values and sending them to the input of a digital-to-analog converter (DAC), the system synthesizes and outputs a smooth sinusoidal signal [11]. To achieve this, we implemented a very high speed integrated circuit hardware description language (VHDL) program that constructs a read-only memory (ROM) configured as a LUT specifically designed for sinusoidal waveform generation.

In order to maximize efficiency and reduce the usage of the FPGA’s general logic resources, we took advantage of the Xilinx Spartan-6 FPGA’s embedded Block RAM (BRAM). This allowed us to model the ROM in a way that minimized the impact on the device's logical resources, optimizing both memory usage and performance [12]. By using BRAM for the ROM, we were able to create a compact and efficient design that maintains high accuracy in waveform generation without compromising the FPGA’s processing capabilities for other tasks.

The design was programmed and synthesized within the Xilinx ISE Design Suite, a robust development environment that provides extensive support for the Spartan-6 series. This tool chain facilitated the implementation, simulation, and verification of our design, ensuring that it met performance criteria while maintaining efficient resource usage on the FPGA [13], [14].

To convert the digital samples stored in the LUT into an analog signal, we used an 8-bit monolithic DAC, specifically the DAC0808 model. This DAC operates with ±5 V power supplies, ensuring accurate conversion of digital data into an analog signal [15]. With this configuration, we were able to achieve high-quality waveform generation suitable for a wide range of applications that require stable and precise analog signals. The choice of the DAC0808 was made due to its high performance, particularly in terms of resolution and signal fidelity, which is essential for applications where waveform precision is critical [16].

2. METHOD

The MIMAS V2 is an FPGA development board that integrates the AMD Spartan-6 XC6SLX9 CSG324, providing an efficient platform for prototyping and implementing digital designs. It features 512 Mb DDR SDRAM, allowing for enhanced data storage and faster processing capabilities, which is essential for complex applications. Additionally, the board includes onboard SPI flash used for storing the bitstream, facilitating easy configuration and reprogramming of the FPGA. A downloader cable is typically employed to transfer the bitstream to the board, enabling straightforward programming and testing. This setup supports various applications, including DSP, embedded systems, and educational projects, making it a versatile tool for both professionals and students in electronics and computer engineering [17].

The Figure 1 show the used MIMAS V2 FPGA development board which features multiple GPIO pins that enable versatile interfacing with external devices, enhancing its functionality for various applications. Additionally, it includes header connectors that simplify access to these pins, making prototyping and integration easier for developers [17]. The Spartan-6 MIMAS V2 FPGA integrates embedded internal storage, utilizing DDR SDRAM operating at 166 MHz with a capacity of 512 Mb LPDDR. This type of memory is particularly advantageous for applications requiring fast data access and storage, as it allows for efficient handling of larger data sets. Each block in the DDR SDRAM is designed as simple dual-port (SDP) RAM, which enables simultaneous read and write operations. This architecture significantly enhances performance by allowing the FPGA to process multiple data streams concurrently, making it ideal for high-speed applications such as DSP, real-time data acquisition, and other compute-intensive tasks. This FPGA board features 2K×8-bit port BRAM configured as SDP architecture. This design allows for simultaneous read and write access, enhancing data throughput. The BRAM serves as a LUT for digital samples storage, enabling rapid retrieval of the pre-defined values. Table 1 summarizing the characteristics of single port BRAM in the Spartan-6 FPGA [18].

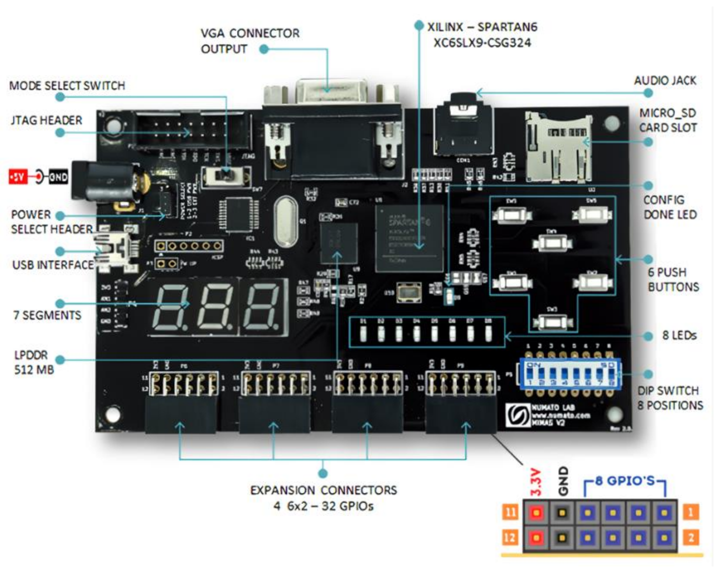


Figure 1. Mimas V2 Spartan-6 FPGA development board [17]

Table 1. Overview of single port BRAM features in Spartan-6 FPGA [9]

Feature	Description
Memory type	Single port BRAM
Memory depth	Up to 18K bits (for 1 block)
Memory width	1, 2, 4, 9, 18, or 36 bits
Total RAM blocks	36 blocks per Spartan-6 device
Configuration	Configured as 1K×18 or 2K×9 in a single port
Access mode	Read or write operations can be performed
Block size	1K, 2K, 4K, or 9K bits
Single clock cycle	Supports single clock cycle read/write
Usage	Ideal for implementing FIFOs, caches, and LUTs

In our case, the LUT presents a set of binary precalculated values recorded in memory locations and obtained using the following relation at several angles.

$$LUT(n) = A * \sin\theta \tag{1}$$

$LUT(n)$: refers to the output value of the LUT at index n which inour case is to 64 as synthesizer resolution. A: represents the amplitude of the sine wave. θ: denotes the angle in radians, which can be related to the input sample index. Using this equation, a LUT can efficiently generate the values of à sine wave, allowing for quick access during DSP tasks. This approach is widely utilized in digital audio, telecommunications, and other applications requiring precise waveform generation.

The change in angle between successive samples in a discrete representation of the sinusoidal wave is represented by the following (2) [19].

$$\Delta\theta = \theta(i) - \theta(i-1) = \frac{2\pi}{L} \tag{2}$$

where: $\Delta\theta$ is the phase difference between two consecutive samples; $\theta(i)$ is the phase angle at the i-th. sample; $\theta(i-1)$ is the phase angle at the previous sample; and L is the total number of samples (or points) in one complete cycle of the waveform.

This relationship shows that the phase increment between samples is determined by dividing a full cycle (2π radians) by the total number of points (L) in the waveform, which is essential for accurately generating smooth and continuous sinusoidal signals in applications such as DSP and waveform synthesis. The variation of L for a fixed frequency in the input clock results a variation of sinusoid and we can have the angle of any index [20].

$$\theta(i) = \Delta\theta * i \tag{3}$$

From (1) and (3), we get:

$$LUT(n) = A * sin\frac{2\pi}{L} * i \tag{4}$$

We can vary the resolution with a change in L. The output wave form amplitude depends on the value of ‘A’ in (1). Following design requirements, we can select and scale the value of ‘A’ to maximize the synthesizer’s output dynamic range. We used DAC0808 as an 8-bit digital to analog converter with an output span in positive side between 0 V to 5 V by modifying (1).

The sample values of the LUT are calculated using (5) and stored in ROM modeled in VHDL. For our DAC: A=255_{10}=FF_H. The calculated value using (5) with L=64 results in the LUT shown in Table 2.

$$LUT(n) = \frac{A}{2} + \frac{A}{2} * sin\frac{2\pi}{L} * i \tag{5}$$

Table 2. Sine LUT with length, L=64

Address (HEX)	Data (BIN)	Address (HEX)	Data (BIN)	Address (HEX)	Data (BIN)
00	10000000	16	11101010	2C	00001010
01	10001011	17	11100010	2D	00000110
02	10011001	18	11011010	2E	00000011
03	10100101	19	11010001	2F	00000001
04	10110001	1A	11000111	30	00000000
05	10111100	1B	10111100	31	00000001
06	11000111	1C	10110001	32	00000011
07	11010001	1D	10100101	33	00000110
08	11011010	1E	10011001	34	00001010
09	11100010	1F	10001011	35	00001111
0A	11101010	20	10000000	36	00010110
0B	11110000	21	01110011	37	00011101
0C	11110110	22	01100111	38	00100110
0D	11111001	23	01011010	39	00101111
0E	11111101	24	01001111	3A	00111001
0F	11111110	25	01000011	3B	01000011
10	11111111	26	00111001	3C	01001111
11	11111110	27	00101111	3D	01011011
12	11111101	28	00100110	3E	01100111
13	11111001	29	00011101	3F	01110011
14	11110110	2A	00010110	-	-
15	11110000	2B	00001111	-	-

Our 64×8 bit ROM is implemented using BRAM on a Xilinx Spartan-6 FPGA. The design stores a sine LUT, enabling efficient retrieval of pre-calculated sine values. The ROM is programmed in VHDL, ensuring hardware-level control and flexibility. A flowchart (Figure 2) is used to represent the design process, including steps such as initialization, address generation, and data retrieval from memory. This approach optimizes resource utilization and performance, leveraging the capabilities of Spartan-6 BRAM for compact and efficient storage [21].

To map the ROM addresses from 00H=000000_2 to 3FH=111111_2, a 6-bit counter can be used to sequentially generate these addresses with each increment. For that we declared the variable cnt as integer range 0 to 63 to be able to call the LUT values from a table of 63 integers, the counter incorporates an asynchronous RESET feature, which ensures that the RESET test takes priority over the clock (CLK) signal. This means that whenever the RESET signal is activated, it can immediately set the counter back to its initial state, regardless of the clock's status. Such priority for the RESET signal is crucial for ensuring system stability and preventing erroneous counting during power-up sequences or unexpected conditions. Implementing asynchronous resets is a common practice in digital design to enhance reliability and control over counter behavior [22]. As the counter progresses, it effectively feeds the stored data from the ROM to the DAC0808's input. The data delivery speed is directly proportional to both the counter's clock speed and the ROM's output capability, to avoid distortion at the DAC output, it's essential to limit the clock speed to prevent exceeding the slew rate of the DAC. The slew rate is the maximum rate at which the output of the DAC can change, and exceeding this rate can lead to errors in signal reproduction. If the clock speed is too high, the DAC may not be able to track the rapidly changing input signals, resulting in distortion or inaccurate output waveforms [23], [24].

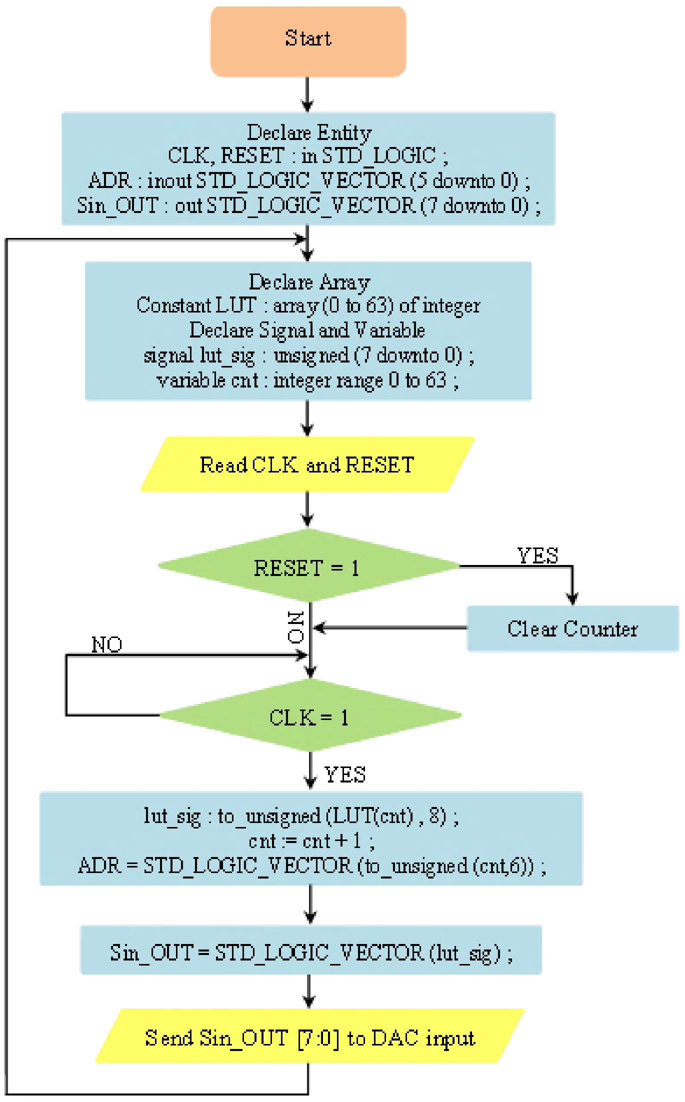
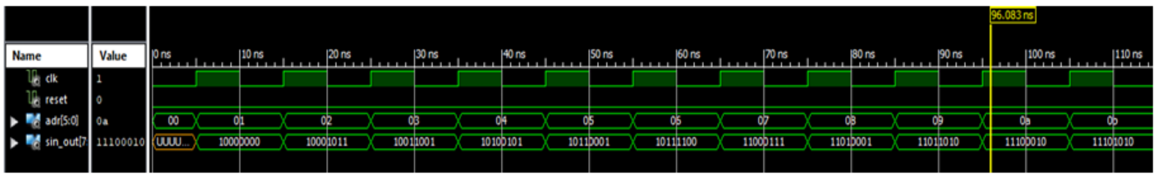

Start
Declare Entity
CLK, RESET : in STD_LOGIC ;
ADR : inout STD_LOGIC_VECTOR (5 downto 0) ;
Sin_OUT : out STD_LOGIC_VECTOR (7 downto 0) ;
Declare Array
Constant LUT : array (0 to 63) of integer
Declare Signal and Variable
signal lut_sig : unsigned (7 downto 0) ;
variable cnt : integer range 0 to 63 ;
Read CLK and RESET
RESET = 1
YES
Clear Counter
NO
NO
CLK = 1
YES
lut_sig : to_unsigned (LUT(cnt) , 8) ;
cnt := cnt + 1 ;
ADR = STD_LOGIC_VECTOR (to_unsigned (cnt,6)) ;
Sin_OUT = STD_LOGIC_VECTOR (lut_sig) ;
Send Sin_OUT [7:0] to DAC input

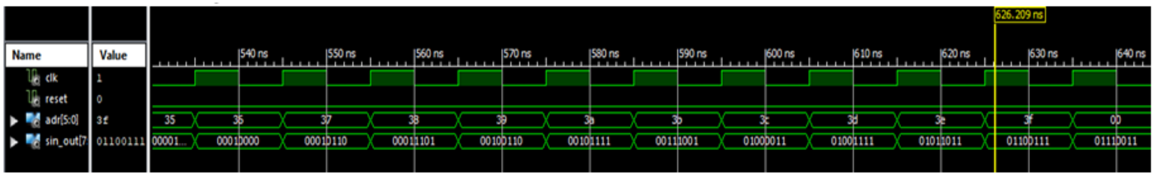
Figure 2. Flowchart of VHDL description

ADR is declared in the entity of our program as an inout STD_LOGIC_VECTOR (5 downto 0) to serve as a bidirectional port for providing addresses to the ROM. This configuration is essential for address management in memory architecture, enabling both reading from and writing to memory locations. Implementing a high-state asynchronous RESET is crucial for ensuring that the counter operates reliably. The initial condition checks whether reset=1. If true, it clears all flip-flops in the counter, ensuring a known starting state. If reset is not activated, the design proceeds to check for a rising edge on the CLK signal. Upon detecting a rising edge, the design accesses the corresponding LUT value located at the index of the cnt array. This value is then converted to an unsigned 8-bit format and assigned to the lut_sig signal [25].

At the end of each process execution of our VHDL behavioral description, we must assign the resulting value of lut_sig, converted to STD_LOGIC_VECTOR, to the Sin_OUT signal, which is declared as an output in our entity. This step is crucial for generating the corresponding analog signal from digital representation. The flowchart in Figure 2 summarizes the design steps involved, while Figure 3 illustrates waveform simulations with ROM addresses (ADR) ranging from 00 to 3F divided into two figures Figure 3(a) from 00 to 0B and Figure 3(b) from 35 to 3F, conducted using a test bench in Xilinx ISE, which is a simulation environment used to verify the functionality of digital designs. It contains the instantiation of the design under test (DUT) along with stimulus signals and input vectors to exercise the DUT. The test bench generates input and monitors outputs, allowing designers to analyze the behavior of their design before implementation on hardware. This process helps identify errors and ensures that the design meets specifications. It does not require physical hardware and runs entirely within the simulation environment [26].


Name
Value
clk
reset
adr[5:0]
sin_out[7
96.083 ns
00 01 02 03 04 05 06 07 08 09 0a 0b
UUUU... 10000000 10001011 10011001 10100101 10110001 10111100 11000111 11010001 11011010 11100010 11101010

(a)

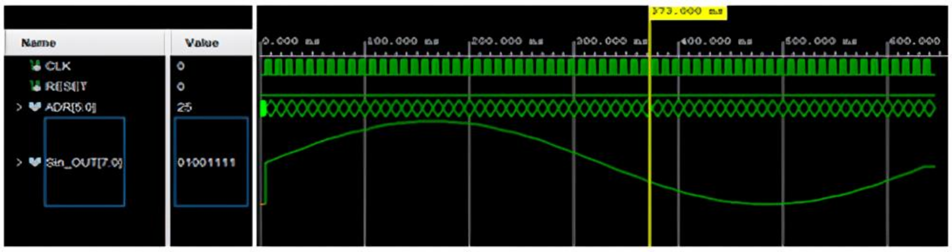


(b)

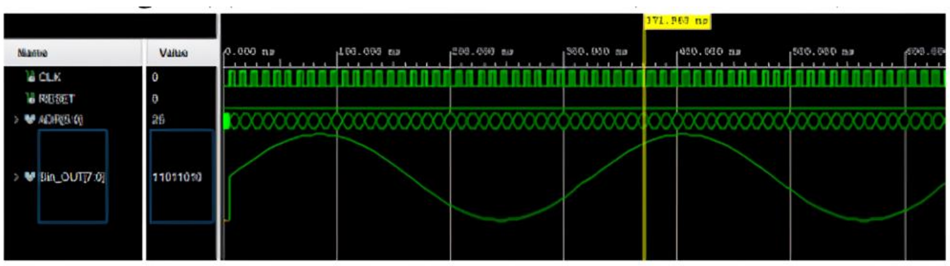
Figure 3. Waveform simulation with ROM ADR from (a) 00 to 0B and (b) 35 to 3F

3. RESULTS AND DISCUSSION

To visualize our experimental results of analog waveforms obtained at the output of the DAC shown in Figure 4, we use Vivado design suite which provides a comprehensive set of tools for hardware description, synthesis, simulation, and programming of Xilinx devices. Vivado is an advanced IDE by Xilinx, designed for creating complex FPGA designs, especially for newer families like the 7-series, UltraScale, and Versal. These FPGA families offer high performance and low power consumption, with Vivado optimizing their capabilities. It supports HDLs like VHDL and Verilog, as well as high-level synthesis (HLS) for C, C++, and OpenCL. Vivado enables synthesis, simulation, and optimization for high-speed applications and includes tools for debugging and real-time simulation. It also supports IP Integrator for integrating pre-built blocks, making it ideal for embedded systems and high-performance computing [27]. As shown in both Figures 4(a) and 4(b) for L=32 and L=64, with the increase of L, memory demand rises, which leads to a greater number of digital samples and extends the time required to access the LUTs. By adjusting the value of L, the system can be configured to generate various sinusoidal frequencies, making it suitable for creating different types of modulated signals, such as binary phase shift keying (BPSK) and amplitude shift keying (ASK). These modulation techniques rely on altering the phase or amplitude of a carrier signal and by controlling L, the system can efficiently switch between different frequencies to achieve the desired modulation format [28].



(a)



(b)

Figure 4. Sinusoid with (a) L=64 (f=2.5 KHz) and (b) L=32 (f=5 KHz)

4. FIELD PROGRAMMABLE GATE ARRAY IMPLEMENTATION

To download The VHDL program on Mimas V2 Spartan-6 FPGA we need to generate programming file and run it. This will create a .bit file, which is the binary file used to load the VHDL design onto the FPGA. To interact with Xilinx's implementation tools we used an user constraint file (UCF) file which is a case sensitive ASCII file generated by the user to defines how the logical design in the VHDL code maps to the physical pins and resources on the FPGA [29].

In a UCF file, both # and // are used for comments, allowing designers to annotate the file and explain the constraints. Each command or statement is terminated by a semicolon (;), which is standard syntax. Most of the content consists of mapping signals to specific pins using the following key commands:

- NET: refers to the logical signal in the design.
- LOC: specifies the physical location (pin) on the FPGA to which the signal is mapped.

Specifically, the UCF file allows constraining the following aspects of the FPGA design:

- Pin Assignments: maps logical signals to specific physical pins on the FPGA.
  Example: `NET "clk" LOC = "P85"`; (assigns the "clk" signal to pin P85).
- I/O standards: defines the voltage standard for each signal (e.g, LVCMOS33, SSTL).
  Example: `NET "clk" LOC = "P85" | IOSTANDARD = LVCMOS33;`

5. CONCLUSION

This project successfully implemented a DDS signal generator on a Spartan-6 FPGA. The use of LUTs in BRAM enables precise generation of analog waveforms, such as sine and square signals. The integration of the DAC0808 DAC ensures accurate conversion of digital samples. Thanks to the FPGA's reconfigurable architecture, signal parameters like frequency and phase can be adjusted in real time. This design is particularly suitable for applications in DSP and modulation techniques such as BPSK and ASK. Overall, this project demonstrates the advantages of FPGA technology for high-precision and scalable signal generation. For future research, it would be valuable to explore the integration of higher-resolution DACs and investigate the potential for real-time signal synthesis across a broader frequency range, which could enhance the versatility and performance of DDS systems in more complex applications.

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