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Low-noise amplifier with pre-distortion architecture for ultra-wide band application in radio frequency

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ABSTRACT

Ultra-wide band (UWB) is a wireless technology deployed for transmitting data at high rates over short distances. Similar to Wi-Fi and Bluetooth, UWB is a radio frequency (RF) technology that operates via radio waves. To remove minor noise and glitches, low noise amplifier (LNA) is required because it amplifies weak signals without significantly adding noise. However, UWB has multiple frequencies that require coefficient change due to frequency variations. When low-pass filter (LPF) is employed to solve this, updates are necessary to manage delay and power because the LPF feedback is connected to LNA to increase delay and power consumption. In this research, LNA with a pre-distortion architecture is proposed to remove minor noises and small glitches. It is processed by using pre-distortion as an active component which reduces delay and power consumption in UWB. The pre-distortion process operates in the subthreshold voltage range by providing a transistor to each frequency as input, inturn effectively reducing the noise. The proposed LNA with pre-distortion architecture is developed on 180-nm complementary metal-oxide semiconductor (CMOS) technology using Cadense ASIC tool. The proposed architecture achieves a noise figure (NF) of 2.16 dB and less power consumption of 43.06×10-6 W when compared to the existing techniques namely, cascade amplifiers, W-band LNA, reflectionless receiver (RX), and broadband RF receiver front-end circuits.

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1. INTRODUCTION

A low noise amplifier (LNA) is the most significant component of a radio frequency (RF) front-end receiver system [1], [2]. Recently, the LNA power amplifier module with integrated duplexers is used to minimize RF complexity in high-end platforms [3], [4]. Traditionally, resistive/reactive, balanced, distributed, and feedback technologies are utilized to increase the bandwidth. The balanced amplifier involves two 3 dB quadrature couplers and two identical amplifiers. It is viable to attain input/output return loss and good gain flatness, but the 3 dB couplers obtain a large area and introduce noise to the circuit [5]. The transmission line contains a drain line inductor and drain-source capacitor device, a gate line inductor, and gate-source capacitor device [6]. Numerous gain cells are added and amplified to produce ultra wide band (UWB) features [7]. However, multiple gain cells require a large area which results in high noise and high power consumption in distributed amplifiers [8]. Recently, there has been a growing interest in RF-based device-free sensing and positioning, particularly leveraging the availability of physical-layer information (channel response) for low-cost commercial radio devices like UWB, Wi-Fi, and RF

identification [9]. Without the requirement of attachment or visibility of sensors to the users, passive RF-based sensing is significant for various applications that consider security, feasibility, and privacy problems [10]. Certain RF bands like 2.4 and 5 GHz are greatly populated bands that offer coverage and connectivity, but have much interference from the large demand of other devices [11]. To increase the demand for higher data rates and greater system capacities of wireless communications, 5G technology is moving towards mm-wave frequencies [12]. As the carrier frequency increases, it becomes challenging to manage the performance of noise in LNA which is a receiver key block, because the minimum noise figure (NF) of a single metal oxide semiconductor (MOS) device is proportional to its operating frequency [13]. Numerous noise-matching networks with band-pass filters (BPF), low-pass filter (LPF), and high pass filter (HPF) structures that exhibit high-performance LNA in the complementary metal-oxide semiconductor (CMOS) process [14], [15]. However, UWB has multiple frequencies which require to change coefficient due to the frequency variations. When using an LPF to address this, updates are required along with a LPF feedback connected to the LNA which increases the delay and power consumption. Chung and Iliadis [16] implemented a cascade amplifier with inductive load and generation to optimize highly sensitive LNA for RF environments. The main focus on cascade topology was despite the slightly high NF due to the addition of one more transistor than the common gate and common source structure. The cascade amplifier topology was beneficial in terms of gain, linearity, and bandwidth due to the dual-transistor configuration which reduced early voltage effects and Miller capacitance. However, the cascade amplifier introduced more noise due to the additional transistor stage which impacted the overall NF in LNA.

Agarwal *et al.* [17] suggested a narrowband inducer degenerated cascaded LNA design for attaining efficient NA and maximum gain in real-time applications. Initially, the narrowband inducer degenerated the cascaded LNA design analyzed input matching values, high gain, and high reverse isolation coefficient values. These values were plotted in a Smith chart after performing an analysis of the S-parameter to determine the system stability. The NA was decreased due to the topology of inductor degeneration adopted in LNA, which eventually raised the gain and limited noise performance. However, the narrowband cascade LNA suffered from increased power consumption and delay due to the inclusion of multiple cascade stages. Hamdi [18] developed a W-band LNA in CMOS technology for wideband and narrowband applications. The developed LNA employed extensions of input matching bandwidth depending on the source degeneration topology, optimized at the supply voltage and center frequency. The LNA design was based on an agreeable tradeoff between NA and gain which led to high linearity and better bilateral stability represented by an input third-order intercept point. However, W-band LNA faced difficulties with high power consumption due to constraints in the CMOS process scaling at high frequency, impacting both narrowband and wideband. Deng *et al.* [19] introduced a reflectionless receiver (RX) to minimize in-band intermodulation and high-order mixing products. The RX had a double-balance passive mixer, absorptive intermediate frequency (IF) amplifier, and dual-path noise noise-canceling LNA. In order to prevent the out-of-band signal reflected by a mixer, the absorptive IF amplifier was employed to minimize the high-order mixing products and intermodulation caused by out-of-band remixing signals. The dual-path noise canceling LNA was utilized to achieve NA at the range of wide frequency. However, RX suffered from increased noise because of the insertion loss of reflective structures which degraded the overall performance. Zhou *et al.* [20] presented a broadband RF receiver front-end circuit for internet of things applications. The dual-path noise-canceling LNA circuit was designed to achieve balun functionality and impedance matching without the requirement of on-chip inductors. The circuit of IQ local oscillator (LO) generation was employed in RF to generate non-overlapping signals with a duty cycle which minimized the mixer's power consumption and increased its gain. However, broadband RF receivers struggled to effectively filter out unwanted signals because of the broader frequency range. From the overall analysis, the existing techniques are seen to have limitations like the introduction of more noise due to the additional transistor stage and insertion loss of reflective structures, increased power consumption, and delay due to the inclusion of multiple cascade stages. However, UWB has multiple frequencies which require to the coefficient to be changed due to the frequency variation. When using an LPF to address this, updates are required to manage delay and power because LPF feedback connected to the LNA which increase delay and power consumption. The above-stated problems need to be solved, hence taken as the motivation of this research. Therefore, LNA with pre-distortion architecture is proposed to remove minor noises and small glitches by using pre-distortion as a passive component which reduces delay and power consumption in UWB.

The main contributions of this research are as follows: i) the LNA design utilizes an architecture called pre-distortion, a linearization method to suppress inter-modulation distortion in LNA. The pre-distortion architecture obtains high power efficiency and better linearity by minimizing frequency interference and signal distortion; ii) the LNA with pre-distortion operates within the subthreshold voltage range by providing a transistor to each frequency as an input which generates thresholds and reduces noise effectively. Additionally, there is no feedback in the output; and iii) the proposed architecture is developed on 180-nm CMOS technology using Cadense ASIC tool.

This paper is structured as follows: section 2 describes the proposed method in detail. Section 3 represents the LNA with pre-distortion method, while section 4 indicates the results and discussion. Lastly, section 5 summarizes the overall conclusion of this study.

2. PROPOSED METHOD

In this research, the LNA with pre-distortion architecture is proposed to reduce noise effectively. The RF receiver contains LNA, Mixer, LPF, analog to digital converter (ADC), and codeword distortion. Initially, the analog signal is passed through the LNA to amplify weak incoming signals, where this LNA employs a pre-distortion architecture to suppress the inter-modulation distortion and obtain high power efficiency with better linearity. Then, the signal is fed into the mixer by combining an analog signal with an input signal to remove unwanted noise in the signal. Then, LPA is used to remove the high-frequency noise or interference present in a signal. ADC is employed to convert analog signal to digital signal. Finally, a codeword detector is performed to identify the type of signal to be received. Figure 1 determines a block diagram for the RF system.

The proposed architecture begins by passing the analog signal into LNA which detect variations in signals, while pre-distortion reduces the intermodulation interference. Following this, mixer, LPF, ADC, and codeword detector are employed. The overall workflow of the proposed methodology is explained:

- Initially, the analog signal is fed into LNA which detects variations in the amplitude of signal.
- LNA utilizes a pre-distortion architecture to suppress inter-modulation distortion in LNA. In the schematic LNA diagram, the first block is a pre-distortion circuit which is processed by active components that obtain high power efficiency and better linearity by minimizing frequency interference and signal distortion.
- Pre-distortion architecture enables high-speed data transmission with spectrum efficiency which achieves low power consumption effectively. Therefore, the linear relationship between input/output (I/O) and distortion is minimized, and hence the overall amplifier linearity is achieved by using the pre-distortion circuit before LNA.
- In the N-MOS transistor, 18 volts turns on, while 0 volts turns off. In the P-MOS transistor, 0 volts activates it, while the supply voltage turns it off. Then, the output is generated noise out noise-free.
- The mixer process integrates the RF input signal with a local oscillator (LO) signal. This mixing process generates sum and difference frequency components.
- Then, the mixer output is fed into LPF to check whether it contains noise. After eliminating the noise, ADC is performed to convert an analog signal into a digital signal.
- Finally, a codeword detector is used to identify the type of signal to be received by storing predetermined patterns or codes corresponding to the signal.

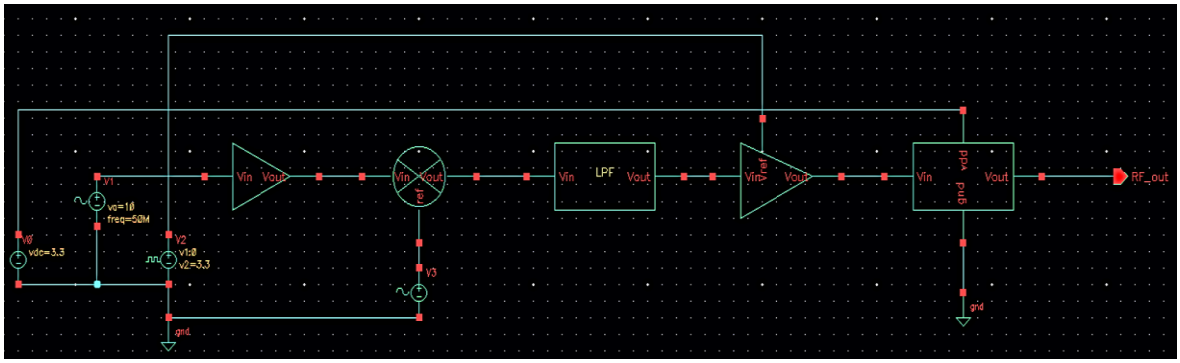

Figure 1. RF block diagram

3. LOW NOISE AMPLIFIER WITH PRE-DISTORTION ARCHITECTURE

LNA with pre-distortion is designed to reduce noise and power consumption for UWB in RF. The pre-distortion compensates for non-lineraites in LNA and enhances the signal clarity. This proposed arcitecture is significant for managing high signal integrity over wide frequency ranges to render it appropriate for UWB system.

3.1. Low noise amplifier

Initially, the analog signal is fed into LNA which detects variations in signal amplitude and plays a primary role in the receiver side. In an RF receiver, LNA is designed to amplify [21], [22] weak incoming signals while establishing minimal additional noise which enhances the receiver's sensitivity and improves the signal-to-noise ratio. LNA is essential in applications that need accurate signal processing such as in wireless communication systems and RF. The LNA performance is mainly affected by three parameters which are NF, gain, and input impedance of the amplifier. To achieve these goals simultaneously, a two-phase topology is utilized with the first phase optimized for low-noise and high-gain operation. The second stage aims for high linearity and high 1db point compression by employing negative feedback. The cascade topology with inductive degeneration is utilized to enable appropriate impedance matching and isolation. The first step is the estimation of the optimum width of the input transistor M_1 to acquire the best noise performance which is expressed in (1):

$$W_1 = W_{opt1Fmin} = \frac{1}{3\omega L C_{ox} R_s} \quad (1)$$

where, C_{ox}, R_s, and L respectively represent the transistor length, oxide capacitance, source resistance, and operating frequency. The cascading transistor dimension M_2 is same as that of M_2. This needs a trade-off to prevent the magnitude of noise M_2 and Miller effect M_1. The refernce current I_{ref} is evaluated depending on the circuit power consumption. The overall gate-source capacitance C_{gst} of transistor M_1 is expressed in (2).

$$C_{gst} \cong \frac{2}{3} W_1 L C_{ox} \quad (2)$$

Transistor M_3 is utilized as an LNA biasing network that constructs a current mirror with M_1. Further to reduce the noise and power consumption, the transistor width M_3 is set to a M_1 fraction. From (3), it is determined that the source inductor is utilized for impedance matching and the inductor of the gate is employed for input resonance frequency.

$$\omega_0 = \sqrt{\frac{1}{(L_s+L_g)C_{gst}}} \frac{g_m}{C_{gst}} L_s - 50 \quad (3)$$

A resistance R_b is utilized to determine the gate-source capacitance effect in M_3 transistor and its value is 2-4 $k\Omega$ in 0.18 μm. Typically, C_1 is considered to be 5-10 times > C_{gst}. At the output, an inductor is kept at the drain for the main reasons. Initially, it is to attain the desired frequency at the drain inductor that resonates by the overall drain capacitance. Next, it generates a high impedance to acquire a better gain. The voltage gain for LNA is computed as formulated mathematically in (4). Where, g_{m1} indicates transconductance of M_1, Z_1 represents load impedance, and Q_{in} denotes network quality factor in input matching. Figure 2 represents a schematic diagram for LNA.

$$A_v \cong Q_{in} g_{m1} Z_L, Q_{in} = \frac{1}{2\omega_0 R_s C_{gst}} = \frac{\omega_0 (L_g + L_s)}{2R_s} \quad (4)$$

3.1.1. Pre-distortion amplifier

The LNA design utilizes an architecture called pre-distortion which is a linearization method that suppresses the inter-modulation distortion in LNA. In the schematic LNA diagram, the first block is a pre-distortion circuit which is processed by active components. In that, the variable voltage 1.82 peak voltage (V_p) is given to the frequency which removes minor noise. The main goal is to implement a pre-distortion to obtain high power efficiency and better linearity by minimizing frequency interference and signal distortion. The pre-distortion architecture is developed on 180-nm CMOS technology which achieves better linearity. Before amplification, the pre-distortion adjusts the signal that reduces distortion and renders the signal output matchable to the input which leads to enhnaced efficiency, and signal quality in UWB. Pre-distortion is one of the generic terms added in the architecture that helps linearize the minor noise amplifier by making suitable modifications through its insertion at the front of the main device to cancel the modulation distortion of a major device to the I/O signal and amplitude-phase. Figure 3 depicts the schematic diagram for the pre-distortion circuit.

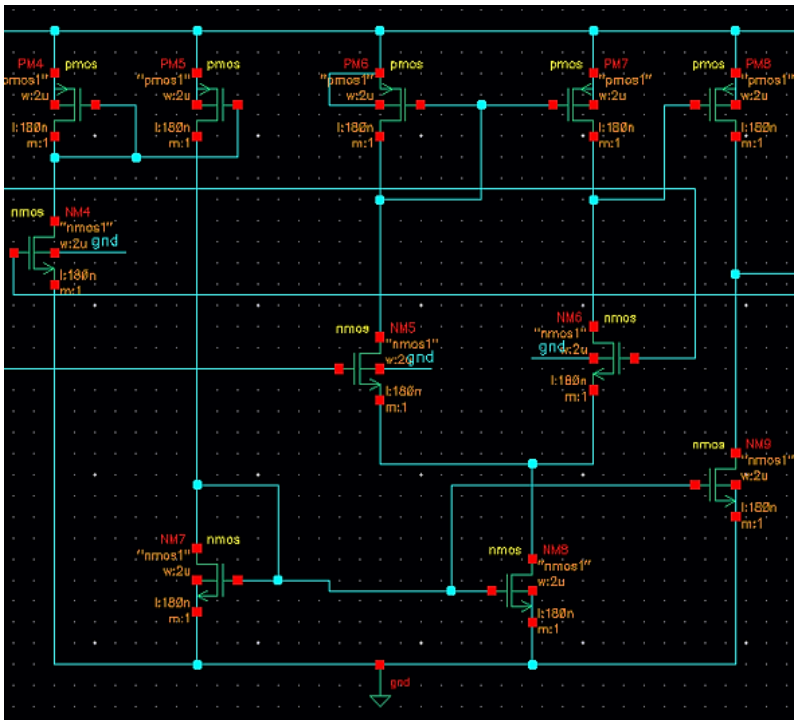

Figure 2. The schematic diagram for LNA

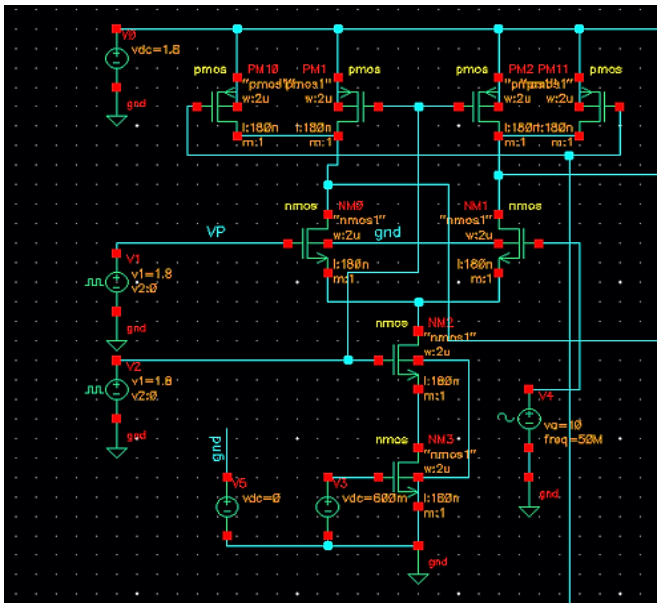

Figure 3. The schematic diagram for pre-distortion circuit

Pre-distortion is inserted in at the front of the primary device and hence helps to cancel modulation distortion of the major device. The primary role of the pre-distortion architecture is to enhance linearity in the I/O broad range without NF degradation. This architecture enables high-speed data transmission with spectrum efficiency, alongside low power consumption effectively achieved. Therefore, the linear relationship between I/O and distortion is minimized and hence the overall amplifier linearity is achieved by using the pre-distortion circuit before LNA. The capacitor and resistor are used as loads to filter out passive components. In the N-MOS transistor, 18 volts turns on, while 0 volts turns off. In the P-MOS transistor, 0 volts turns on, while the supply voltage turns off. Then, the output is generated noise-free by eliminating the

noise. Figure 4 indicates the overall diagram for the LNA-pre-distortion architecture. Then, the output of pre-distortion is fed into the mixer process.

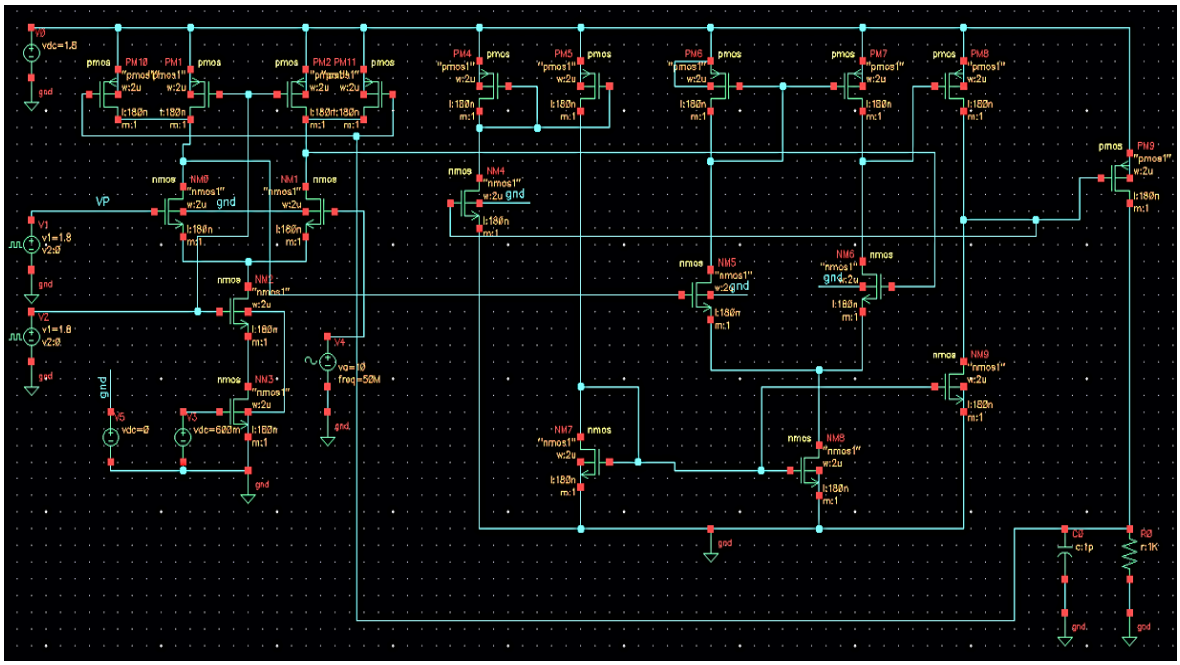

Figure 4. The overall schematic diagram for the LNA-pre-distortion circuit

3.2. Mixer

The mixer process integrates the RF input signal with linear amplifier (LA) signal which generates the sum and difference frequency components. The primary structure of a single mixer is that it has 2 input ports and 1 output port. It integrates a carrier signal RF subject to down-conversion [23] or up-conversion with input from a LO.

The properties of mixer are time-variance and nonlinearity, and the operation is determined in the time domain by multiplying 2 input signals which are numerically expressed in (5) and (6). The output of the mixer is expressed in (7). The mixer output contains the sum and difference of the input signal and LO frequency. Then, the output of the mixer is fed into LPF to eliminate high-frequency noise.

$$x(t) = A\cos\omega_1 t \tag{5}$$

$$y(t) = B\cos\omega_2 t \tag{6}$$

$$x(t).y(t) = A\cos\omega_1 t\,.B\cos\omega_2 t = \frac{AB}{2}cos(\omega_1 - \omega_2)t + \frac{AB}{2}cos(\omega_1 + \omega_2)t \tag{7}$$

3.3. LPF, ADC, and codeword detector

After the mixer operation, the LPF is performed to check if it contains noise in a signal. In signal processing, an LPF [24] is commonly utilized to remove or attenuate high-frequency components from a signal when allowing the component of low-frequency. In data interpretations, it enhances the clarity of signal and reduces errors which make it crucial for exact signal processing. This process assists in isolating the desired low-frequency components, making it easier to evaluate the signal for further processing. After removing the noise, the ADC [25] is performed to convert an analog signal into a digital signal. It determines the analog input at regular intervals, quantizes the values of samples into a binary code, and assigns digital values depending on the input voltage levels. After converting to a digital signal, the codeword detector is employed to identify the type of signal to be received, while storing predetermined codes or patterns corresponding to signals. Using an LNA with pre-distortion in the RF receiver enables improved linearity, reduces noise performances by maintaining a high signal-to-noise ratio, and provides low power consumption due to optimized signal handling, resulting in overall efficiency gains in RF receiver for UWB application.

4. RESULTS AND DISCUSSION

The proposed LNA with pre-distortion architecture is simulated by utilizing the Cadence Asic tool and 180-nm CMOS technology. LNA amplifies the weak incoming signals while establishing minimal additional noise which improves signal-to-noise ratio. Pre-distortion linearizes the LNA by making suitable modifications by inserting it at the front of the main device to remove modulation distortion of a major device on the I/O signal without NF degradation. The performance of conventional LNA and proposed LNA with pre-distortion is presented in the following subsections.

4.1. Performance analysis

Figures 5 and 6 indicate the NF performance for conventional LNA and proposed LNA with predistortion architecture. NF represents the ratio of the signal-to-noise ratio at the input of a device to the signal-to-noise ratio at output, which is measured in decibels (dB). NF quantifies additional noise produced by the pre-distortion process which is associated with the original noise level of the signal. A lower NF represents that the pre-distortion architecture effectively minimizes signal distortion without increasing noise, which is shown in Figures 5 and 6.

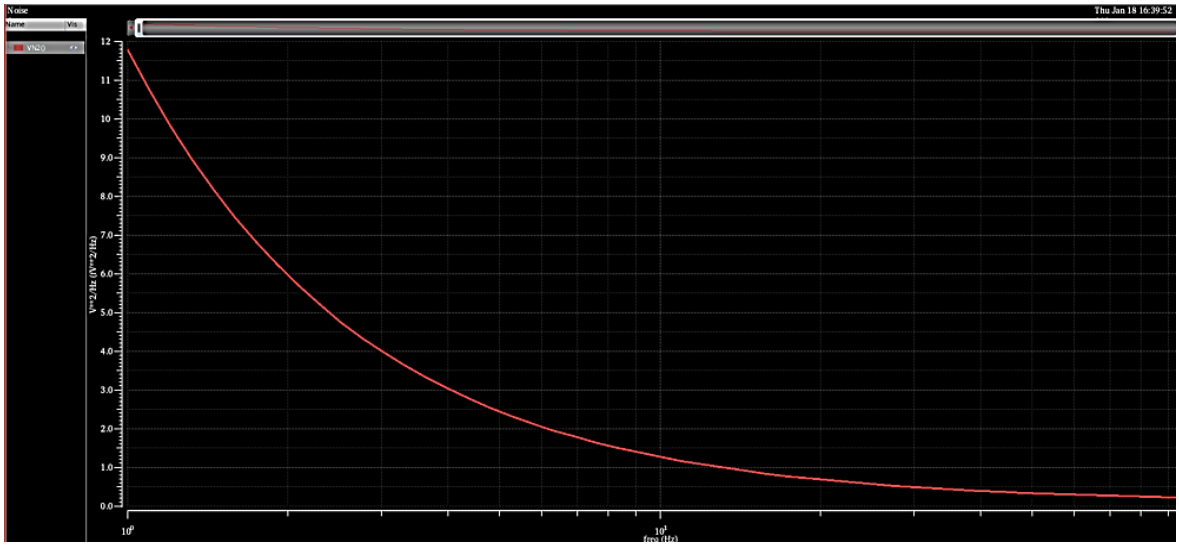

Figure 5. Performance of NF for conventional LNA

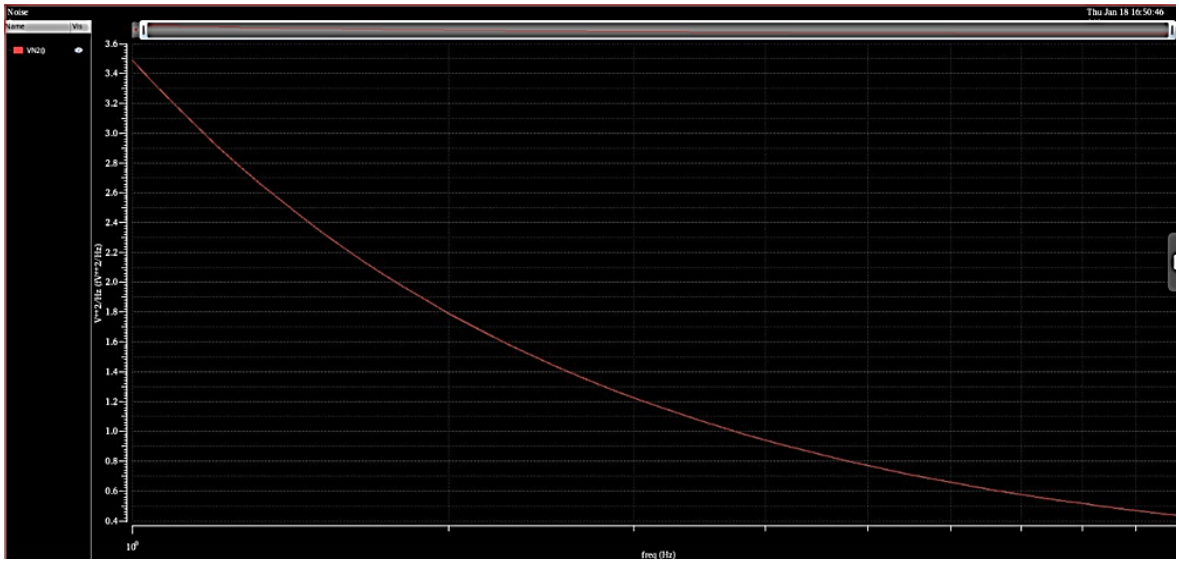

Figure 6. Performance of NF for proposed LNA with pre-distortion

On the other hand, Figures 7 and 8 illustrate the performance of power wave for conventional LNA and the proposed LNA with pre-distortion architecture. Power wave performance measures the efficiency with which the amplifier manages power signals, minor noises, and glitches. The proposed architecture exhibits better performance in power waves, as compared to the conventional LNA due to reduced minor noises and glitches which prove it to be more efficient in power management. This results in clearer, more stable signal transmission in power wave characteristics in th proposed LNA with pre-distortion.

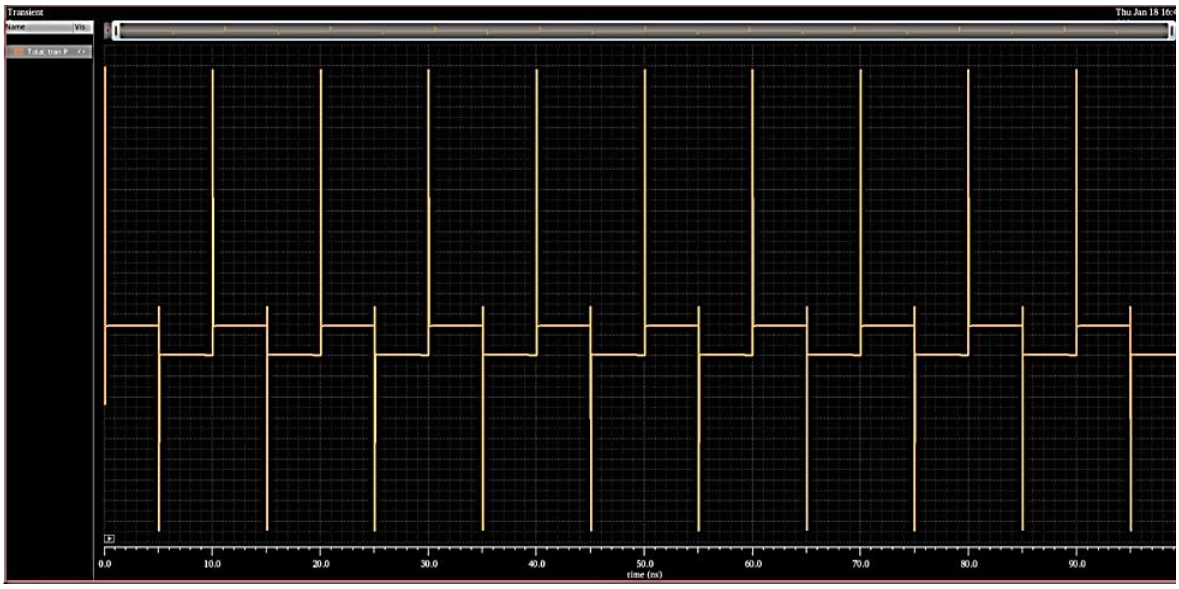

Figure 7. Performance of power wave for conventional LNA

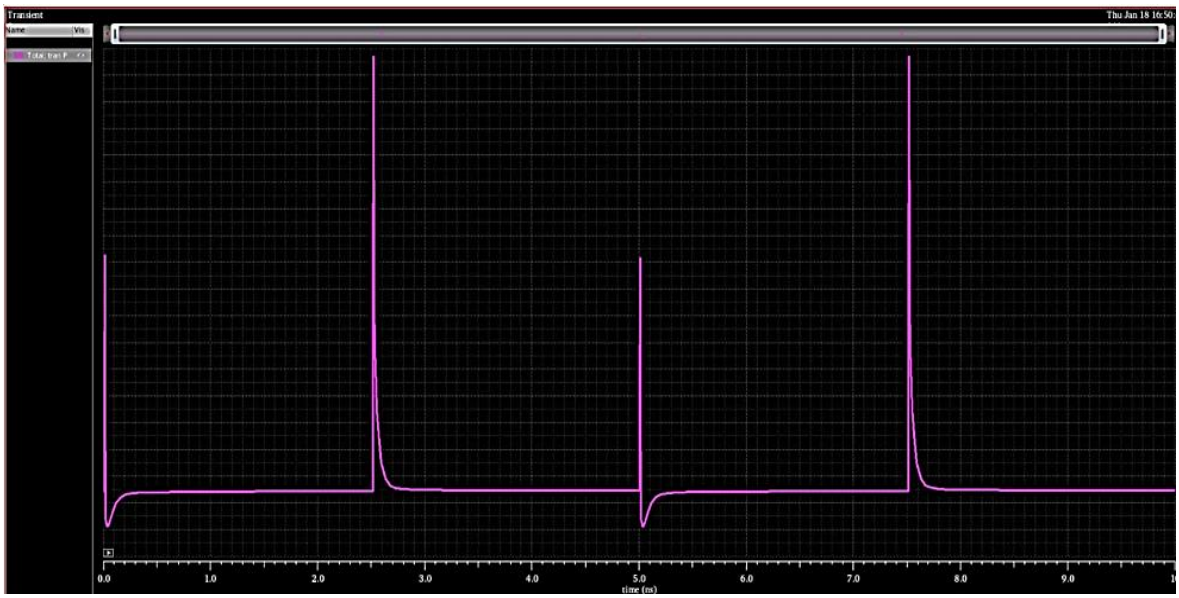

Figure 8. Performance of power wave for proposed LNA with pre-distortion

Figures 9 and 10 indicate the delay performance for conventional LNA and proposed LNA with pre-distortion in 180 nm CMOS technology. From this analysis, it is clear that LNA with pre-distortion architecture has less delay of 2.516 ns, wheares the conventional LNA exhibits 5.013 ns. The proposed method achieves less delay due to pre-distortion adjusts for nonlinearities in the amplifier stage. This sreamlined signal management not only minimizes the delay but also increases the speed and quality of

transmitted signal which enables the proposed LNA with pre-distortion to be more reliable. This streamlined process minimizes delay, enhancing the overall signal quality and speed.

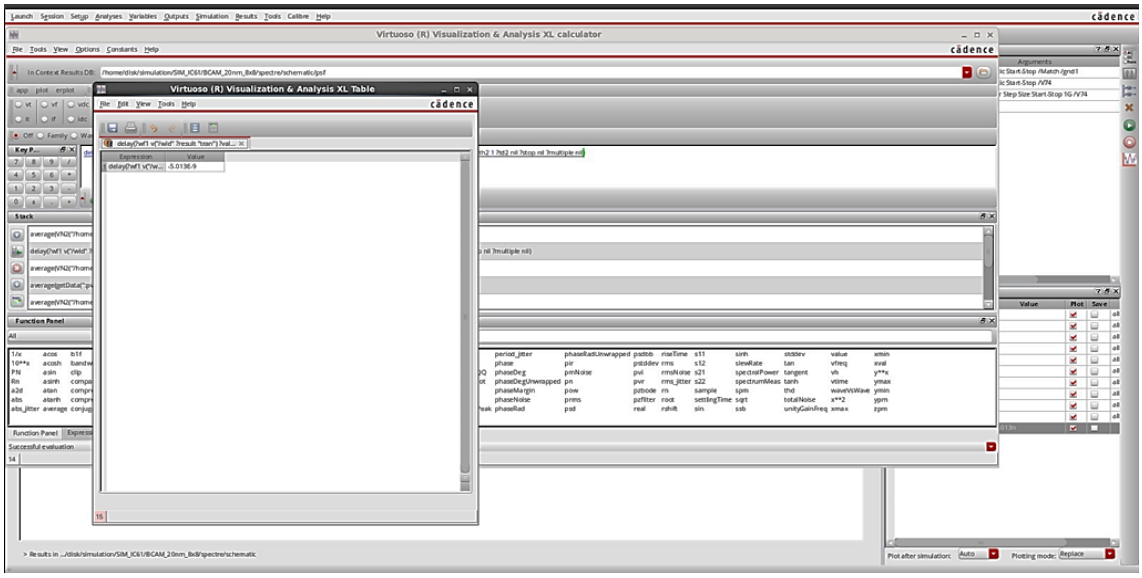

Figure 9. Delay performance for conventional LNA

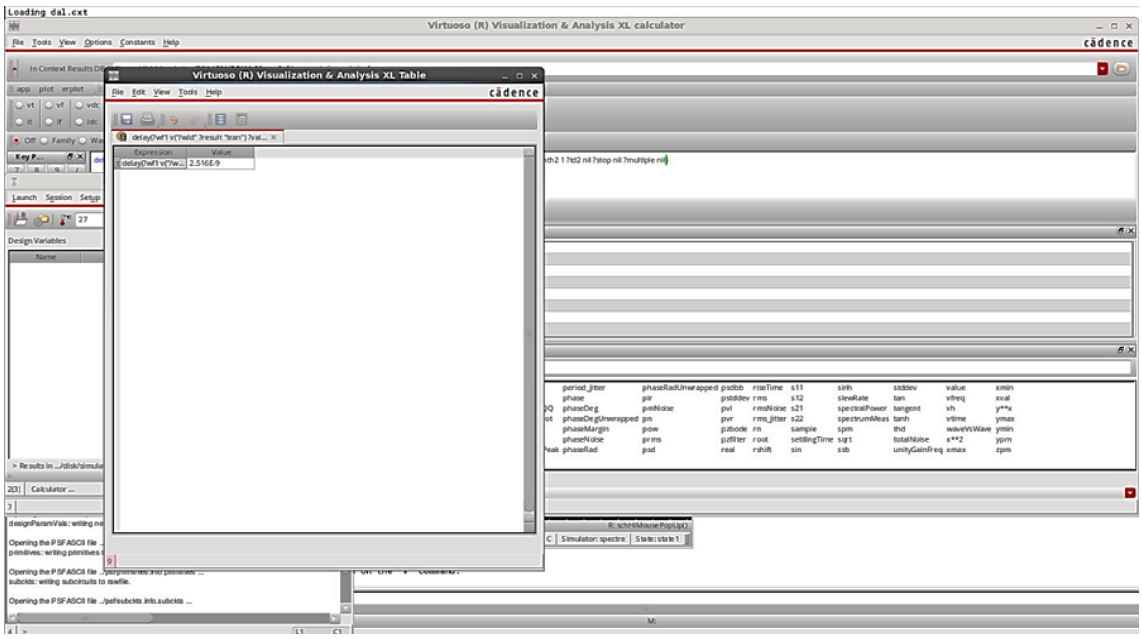

Figure 10. Delay performance for proposed LNA with Pre-distortion

Figures 11 and 12 demonstrate the performances of power consumption for conventional LNA and proposed LNA with pre-distortion. Their observation proves that the proposed approach obtains a better power consumption of 43.06×10-6 W, as opposed to conventional LNA of 1.256 10-3 W. This is because of the pre-distortion architecture which minimizes the non-linearities in the amplifier, and hence does not require as much power to fix distortions. This in turn empowers the LNA with pre-distortion, thereby standing more persuasive with lesser by power consumption.

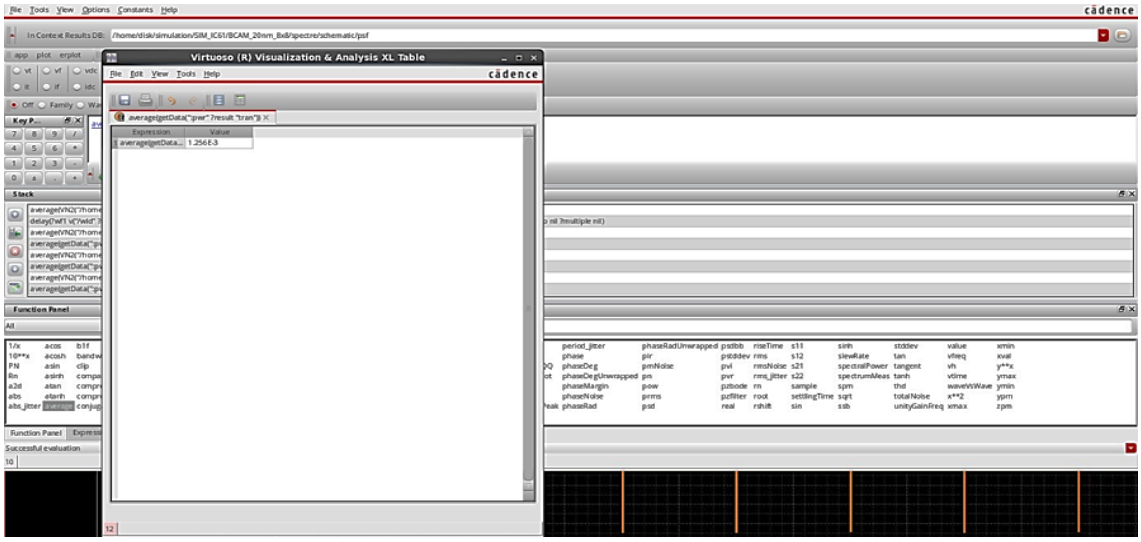

Figure 11. Performance of power consumption for conventional LNA

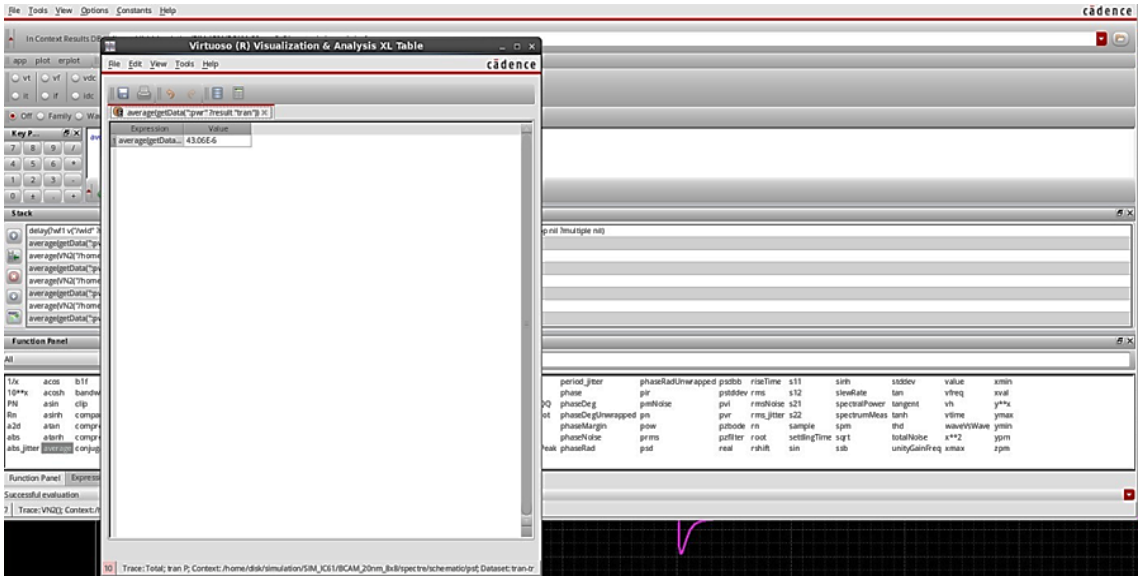

Figure 12. Performance of power consumption for proposed LNA with pre-distortion

Table 1 determines the performance analysis of conventional LNA and proposed LNA with pre-distortion in 180 nm CMOS technology. The performance of LNA is compared against the proposed architecture. The obtained results show that LNA with pre-distortion achieves a superior NF of 2.16 dB because the proposed approach enables linearity. This hence reduces noise performances by maintaining a high signal-to-noise ratio, and provides low power consumption due to the optimized signal handling which leads to overall efficiency gains in RF receiver. The results emphasize the effectiveness of incorporating pre-distortion in boosting the resourcefulness and execution of LNA in RF.

Table 1. Performance analysis for conventional LNA and proposed LNA with pre-distortion

Performance	Conventional LNA	Proposed LNA with pre-distortion
NF (dB)	3.68	2.16
IIP3 (dBm)	6.157	3.874
Area (mm2)	1.46	0.15
S11	<-6	<-9
Power (W)	1.256×10-3	43.06×10-6
1 dB compression point	8.5	7.2

4.2. Comparative analysis

Table 2 and Figure 13 presents a comparative analysis of the existing techniques using 180 nm CMOS technology. The existing methods: cascade amplifier [16], N-LNA [17], and W-band LNA [18] are compared with the proposed LNA with the pre-distortion technique. In relation to the existing techniques, LNA with pre-distortion attains a finer NF of 2.16 dB, IIP3 of 3.874 dBm, area of 0.15 mm^2, and power of 43.06×10^{-6} W due to incorporating pre-distortion. The LNA compensates for non-linearities and distortions that typically occur in signal amplification which gives rise to enhanced signal fidelity. Also, the reduced NF of LNA contributes to elevated SNR, significant for managing high-quality communication over wide frequency ranges. The proposed architecture maintains lineraity across varying signal amplitudes which further provides preeminent performance.

Table 2. Comparative analysis of existing techniques

Methods	CMOS technology	NF (dB)	Area (mm^3)	Power (W)
Cascade amplifier [16]	180 nm	3.54	0.26	9×10^{-3}
N-LNA [17]	-	3	-	-
W-band LNA [18]	0.18 µm	3	N/A	N/A
Proposed method	180 nm	2.16	0.15	43.06×10^{-6}

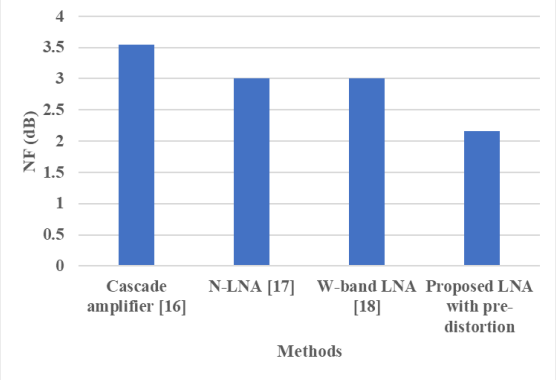

Figure 13. Graphical representation of proposed architecture with existing methods

4.3. Discussion

The research presents a LNA with pre-distortion architecture by representing significant improvements over the existing approaches. The significant interpretations of the findings demonstrates that the proposed LNA with pre-distortion effectively solves the key problems determined in existing models. Especially, the cascade amplifier [16] introduces more noise due to the additional transistor stage which impacts the overall NA in LNA. Narrowband cascade LNA [17] suffers from increased power consumption due to the inclusion of multiple cascade stages. W-band LNA [18] faces difficulties with high power consumption due to the constraints in CMOS process scaling at high frequency which impacts both narrowband and wideband. RX [19] suffers from increased noise because of the insertion loss of reflective structures which degrades the overall performance. Broadband RF receiver [20] struggles to effectively filter out unwanted signals because of the broader frequency range. The proposed LNA with pre-distortion architecture overcomes these existing techniques' limitations by adding pre-distortion before LNA and achieves a superior outcomes.

The pre-distortion technique enhances linearity in the I/O broad range without NF degradation. This pre-distortion architecture enables high-speed data transmission with spectrum efficiency which obtains effective low power consumption. This pre-distortion architecture increases the linearity. Therefore, LNA with pre-distortion achieves a superior NF of 2.16 dB with a power consumption of 43.06×10^{-6} W whereas the existing method obtains 3.54 dB noise with 9×10^{-3} power consumption. When this comparison is taken into consideration, the existing research upholds numerous benefits of the proposed architecture. Nonetheless, the proposed architecture is effective in reducing non-lineraities but does not fully eliminate all forms of distortions, especially at high frequencies. This is due to complex interaction between amplifiers characteristics and pre-distortion process. Therefore, certain residual distortion still impacts the signal integrity, subsequently affecting the high-frequency performance.

5. CONCLUSION

In this research, LNA with pre-distortion architecture is proposed to reduce the minor noise and small glitches for UWB applications. LNA amplifies weak incoming signals while establishing minimal additional noise which accordingly increases the receiver's sensitivity and improves signal-to-noise ratio. The inclusion of pre-distortion in the architecture plays a signiifcant role by linearizing the minor noise amplifier. This is obtained by presenting the modifications at the front of the main device which assists to cancel out modulation distortions by ensuring a more acurate I/O relationships. This architecture significance enhnaces the spectrum efficiency, data transmission speed, and minimizes the power consumption. The LNA with pre-distortion operates within the subthreshold voltage range by providing a transistor to each frequency as the input which generates thresholds and reduces noise effectively. By performing these operations, the proposed approach achieves commendable NF of 2.16 dB with a power consumption of 43.06×10^{-6} W in contrast to the existing architecture, cascade amplifiers. For practical implementation, it is recommended that future work continues to use advanced pre-distortion architecture to continue improving the model's performance.

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