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Pipelined reconfigurable architecture for 5G software-defined radio systems

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ABSTRACT

The filters are used to allow a specific band of frequencies. In a wireless communication, the filter is used to select the frequency of operation with a narrow or broad band. As the generations increase the amount of data handled increases drastically. 5G data rate can be significantly deliver up to 20 Gigabits per second while 4G communication data rate is handled in the order of 100 Megabits per second. Now the challenge becomes processing data at such a speed with low power and low area specifications. The filters that can configure themselves as per the data received are reconfigurable filters so that the bandwidth is saved. Also, when the pipelining is introduced, the reconfigurable filter improves the performance of the design. This paper details about the pipelined reconfigurable finite impulse response (RFIR) filter with the simplest algorithm with auto updating capability. The design is modelled in Verilog hardware description language (HDL) language, synthesized for Cyclone III field-programmable gate array (FPGA). The results prove that the proposed filter increases only slightly with respect to delay and power dissipation with a trade off in area and maximum possible clock frequency.

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1. INTRODUCTION

The use of software-defined radio (SDR) in wireless technologies is becoming more important. As SDRs may be configured to support a broad variety of operating modes, radio frequency ranges, air interfaces, and waveforms, they are poised to replace many of the conventional approaches to constructing transmitters and receivers. The primary goals of research in this area are to enhance the design and computing efficiency of SDR systems [1]. As it uses the maximum sampling rate, the channelizer in an SDR receiver requires the most computational efficiency. The extraction of several narrowband channels from a broad signal by means of multiple band-pass filters termed channel filters is known as channelization in SDR receivers [2]. The channelizer needs fast finite impulse response (FIR) filters that use little power. Many communication systems, such as SDR, make use of the FIR digital filter for echo cancellation, noise reduction, and voice processing, among other things [3]. With the advances in semiconductor industry, the optimization with respect to area is possible due to scaling in technology, performance is improved by using

various techniques pipelining, retiming, and power dissipation is reduced by various low power techniques like power gating [4], signal gating, and pin reordering.

The FIR filters are chosen over infinite impulse response filters so that the filter remains stable and has a linear phase for easy retrieval of signals. A significant increase in data rate from generation 1G to 5G provokes the research towards the high performance FIR filter design [5]. The digital RF transceiver with the necessary filters is as shown in Figure 1. Reconfiguration is the process of changing how bits flow through a bit stream to improve performance or add a new feature. In this way, hardware may have the same adaptability as software. The potential computing capacity of such fabrics is examined across a variety of reconfiguration platforms [6].

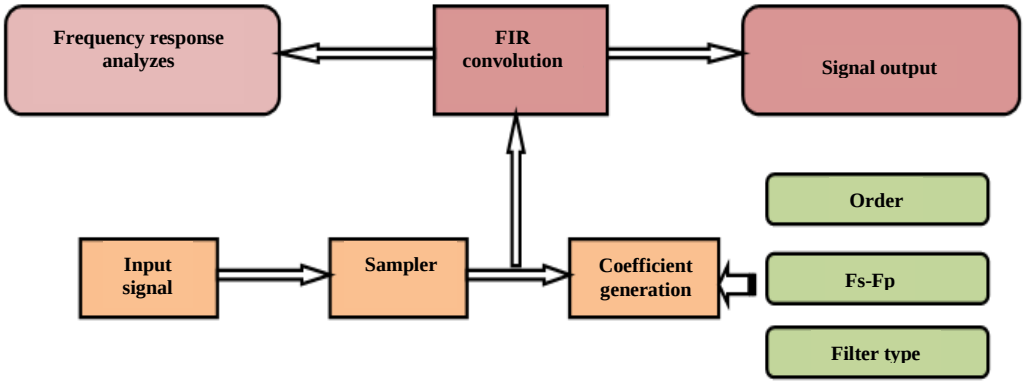

Figure 1. FIR filter

The FIR filter has the architecture as shown in Figure 1, consists of adders, multipliers and delay elements. It can be designed based on two parameters i.e., word size and number of taps. The word size represents the number of bits processed at a time by the filter considering the digital format. The number of taps decides the order of the filter. As the order of filter increases, area occupied and design complexity increases. A linear phase FIR filter with length N=2M+1 has a transfer function that is symmetrical with relation to the impulse response coefficients.

$$H(Z) = \sum_{n=0}^{N-1} h(n)\, Z^{-n} \quad (1)$$

$$H(Z) = Z^{-M} \left[h(M) + 2 \sum_{m-1}^{M} h(M-m) \frac{1}{2} \left(Z^{m} + Z^{-m} \right) \right] \quad (2)$$

Physical channels have both phase (I) and quadrature phase (Q) components in real time (Q). There should be two digital filters for each channel on the SDR transmitter. As demonstrated in (3), to account for the impact of fixed arithmetic, the filter specs are adjusted in accordance with the requirements. Figure 2 illustrates the structure of the reconfigurable FIR filter, showing the use of delay elements, multipliers, and adders to implement the convolution operation.

$$y[n] = \sum_{k=0}^{N-1} b_k . x[n-k] \quad (3)$$

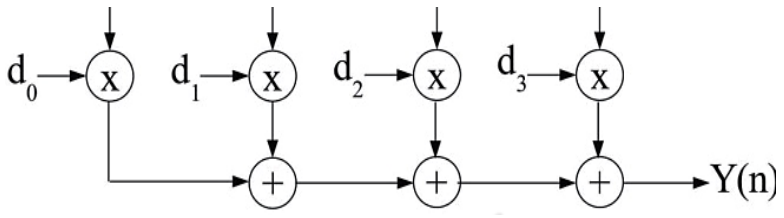

Figure 2. Reconfigurable FIR filter architecture

To adopt for the versatile conditions that prevail in wireless communication channel, reconfigurable filters are designed which extract the hardware as and when required as shown in Figure 3. Depending upon the requirement or the received data, the number of processing elements are extracted. Here, it is shown in terms of multiplexers, shifters, and adders to model in hardware. The primary goal of a SDR is to make transceivers more amenable to modification by switching the majority of their signal processing from analogue to digital. Several wireless communication protocols may thus be used since each can be implemented on the same generic hardware platform. To fulfil the demanding requirements of low power consumption and fast speed, wideband receivers in SDR must be realised. One of the most important features of a SDR is its receiver's flexibility in supporting many wireless communication protocols [7].

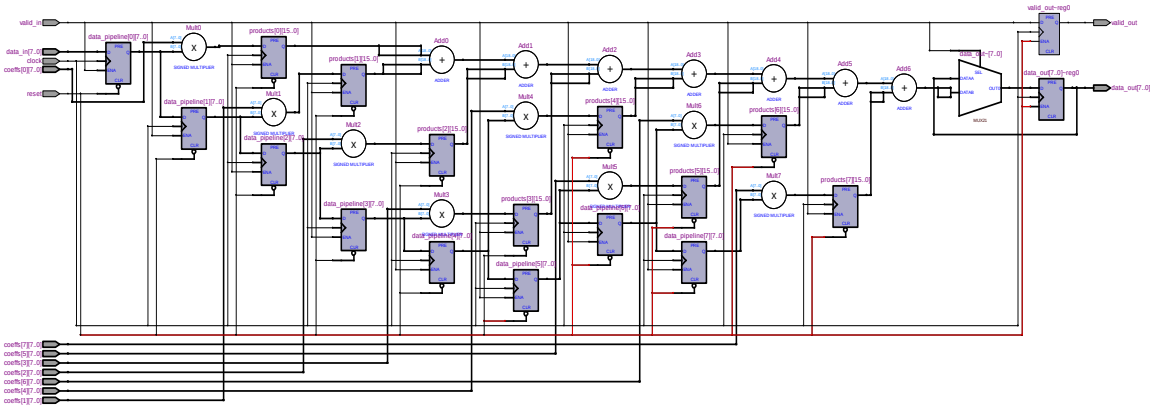

Figure 3. RTL schematic for 8-tap 8-bit reconfigurable FIR filter

The channelizer in a SDR receiver has the greatest sampling rate, making its computations the most taxing. Many channel filters, which are FIR filters, are used to separate the wideband signal into its component channels [8]. This paper aims to propose a simple algorithm for a pipelined reconfigurable FIR filter for 5G SDR systems and analyze its impact on area utilization, delay, power dissipation, and maximum possible operating frequency. The section 2 describes the literature review, followed by proposed algorithm in section 3 and the results are discussed in section 4 followed by conclusion in section 5.

2. RELATED WORK

The FIR filter may be configured in a variety of ways, making it useful for both static and reconfigurable (RFIR) purposes. Several of the most novel methods are addressed in this research. Research by Nicholson *et al*. [9], the complete details about the blocks in an RF communication system are discussed, where the filters need to process a high sampling speed of nearly 20 G samples/s with linearity >100 dB spur-free dynamic range at the receiver. Also explained are the benefits of future wireless systems in terms of an expanded range of high-data-rate coverage, lower handset battery power, higher spectral efficiency, and a lower cost for multi-carrier base stations The article highlights the challenges faced by the RF communication system and the need for advanced technology to overcome them. It also emphasises the potential advantages of future wireless systems in terms of cost, efficiency, and performance.

A filter circuit is necessary for any communication system that either allows a signal to pass through it or does not [10]. It may be acting as an amplifier in some areas of its design. They are essentially just a FIR-shaped data shaping filter. To enable the multi carrier modulation (MCM) schemes used in 5G, prototype filters will be used. The filters that will be used must have strong time localization capabilities. 5G will make use of the universal filtered multi-carrier (UFMC) structure, which has a large number of carrier signal subbands. The filtering must be applied to each subband that is present in the signal. Therefore, synchronisation is necessary after filtering for all frequency subbands has been completed. While the filter is in use, it shouldn't have an effect on the system's bit error rate (BER) or peak-to-average power ratio (PAPR). A variety of prototype filters are available to eliminate the error. A communication channel's interference characteristics can be significantly reduced by a well-designed filter.

Algriree *et al*. [11] suggested method used a combination of the cosine filter, Bartlett, and hamming windowing. As the cosine consists solely of real bases, it was possible to use cosine filtering to differentiate

between 5G data and noise using fewer samples. It is critical to have access to authentic databases with limited data. To further reduce the noise variance, Bartlett segmentation is used to the filtered signals. The Bartlett chart divides the newly collected data set into subsamples, then averages these subsamples together, rate-wise, to arrive at an overall rate value. For this reason, we just do arithmetic and rate determination on the data, and we apply Hamming windowing to each segment to keep the signal as sharp as possible. As there are no natural logarithms, integrals, or differentials, the mathematics is easy to understand and use.

Two reconfigurable FIR filter topologies i.e., programmable shift method (PSM) and constant shift method (CSM) which focuses in reduction of the number of adders in multipliers to enable efficient flexibility and the canonic signed digit (CSD) coefficient multiplier encoding is used to minimize convolutions [12]. This has improved performance and effective area utilization with a trade off in power dissipation. A high speed residue number system (RNS)-based FIR filter design with distributed-arithmetic based on pipelining and retiming techniques is discussed [13]. The results prove that a retimed filter offers better operating prospects than pipelined filter.

Wagner *et al*. [14] proposed 31-tap reconfigurable analog FIR filter using heterogeneously integrated polystrata delay-lines which can be adopted easily for 5G communications. Here the center frequency is 1 to 20 GHz and contains 7-bit programmable weighting circuits at each delay-line tap to allow synthesis of arbitrary frequency responses limited only by the Q-factor and dynamic range of the weighting elements.

Goldsmith *et al*. [15] proposed design of a natively fixed-point filter design method that targets field-programmable gate array (FPGA)-based reconfigurable finite impulse response (RFIR) filters for software defined radio applications. This Filter is capable of reconfiguring cut-off frequencies on-the-fly at run-time; with other parameters, such as filter length and window type, configurable at compile-time. This yields much lower latencies with hybrid method combining window and frequency sampling methods. Results proved that the proposed algorithm generates good-quality filters that display stopband attenuation up to 88dB, transition bandwidths less than 1% of the sample rate, and low resource utilisation. This method gives up to three orders of magnitude faster than an equivalent software implementation, with execution times as low as 2.52 μs, enabling radio applications in which latency is a principal constraint.

Jagadeeswari *et al*. [16] focussed on an efficient reconfigurable FIR filter design based on the sub-expressions for low power applications using reversible gates and sub-expression elimination in cadence EDA tool. The results prove that the proposed algorithm power consumption is reduced by 140558.856 nano watts along with an improvement in the power saving ratios to 7.6%, 20.6%, and 28% with the existing techniques respectively.

The frequency response of the RRC FIR interpolation filter considered during FIR coefficient extraction depends on various measures like interpolation factors, roll-off values, and order. These measures are varied for different wireless standards. In order to support a wide range of standards, digital implementation of the FIR filter requires a bank of FIR coefficients with improved flexibility and high performance. Several works introduced different methodologies (Darak *et al*. [17]), (Sakthivel and Elias [18]) to design a low-complexity reconfigurable FIR filter for an SDR system.

Jia *et al*. [19] proposed that CSD coefficients be grouped in a different fashion. Finding out whether there is just one "zero" bit between two "non-zero" bits is all that's required. Certain statistical traits are detected and taken advantage of by analysing the distributions of the chosen CSs among a large number of CSD coefficients drawn from a broadly representative FIR filter design. When applied to the implementation of FIR filters, the suggested approach may drastically minimise the number of multiplications. This makes it a potentially useful strategy for high-performance digital signal processing with minimal power consumption.

Sharma *et al*. [20] proposed a hybrid idea of artificial bee colony-particle swarm optimization (PSO-ABC) algorithms for the efficient construction of a tree-structured non-uniform filter bank (NUFB) that doesn't have any multipliers. Filter coefficients are created, quantized, and represented as a CSD or binary value inside the same optimization procedure, making this method more efficient than previously available methods. As a result, it is unnecessary to use two distinct optimization strategies, one for filter coefficient creation and another for optimization. Because of its low complexity and small number of adders, the suggested method is the most promising way to create multiplier-less NUFB. A thorough examination of several CSE approaches was performed to determine their efficacy. The proposed algorithm's standout feature is its ability to optimally construct a prototype filter for multiplierless NUFB using a combination of PSO-ABC and CSE in a single optimization. In addition to its potential usage in digital hearing aids, the suggested algorithm also has potential as an effective approach in filter-bank multicarrier communication and channelization.

An efficient and low-power design for a FIR adaptive filter is presented in [21] using approximation computing, distributed arithmetic (DA), and the radix-8 Booth algorithm. To the best of the authors' knowledge, this is the first application of the radix-8 Booth algorithm to the construction of an integrated FIR adaptive filter inside a DA architecture. The suggested approximation FIR adaptive filters demonstrate very minimal accuracy loss compared to the precise implementation in applications involving system

identification and the saccadic system. The suggested system has been shown to reduce EPO by roughly 55% via synthesis and increase throughput per unit space by a factor of 3.2. (TPA).

Liacha *et al*. [22] focused on exploring the spatial properties of RADIX-2r. Area efficient techniques, such as the cumulative benefit heuristic (Hcub), which is noted for having the lowest adder-cost, are a challenge for RADIX-2r. Several different types of sophisticated FIR filters were employed as standards for evaluation. The evaluation results showed that Hcub outperformed other area efficient techniques in terms of adder-cost and that it was competitive with the sophisticated FIR filters in terms of filter performance. These findings suggest that Hcub is a promising technique for designing area efficient FIR filters.

The functionality of FIR may be modified according to certain design requirements. Thus, there must be some well-defined FIR design procedures that meet these standards. The approaches for filter design are broken down into these three broad categories in frequency sampling [23], windowing [24], and optimization [25]. We start with an overview of the fundamental ideas behind each approach, then provide some instances of how these ideas are often implemented in practise. Finally, the benefits and drawbacks of the summarised approaches are covered in the proposed design.

3. RESEARCH METHOD

The proposed Algorithm 1 is where the variables are considered as number of taps, the filter coefficient and data widths. The inputs include the clock, reset, filter coefficient values, valid input signal and data input signals. The ouput signals include data output and valid output signals.

Algorithm 1. Variables are considered as number of taps, the filter coefficient and data widths

```
Variables: taps, coeff_width, data_width
Inputs: clock, reset, coeffs, data_in, valid_in
Outputs: data_out, valid_out
if reset is 0
data_1, products, data_out are 0
else
for every rising edge clock
        if valid_in = '1' then
                data_1 = data_in & data_1(0 to taps-2)
for i = 0 to taps-1
                        products(i) <=coeffs(i)) * data_1(i)
                        data_out:= data_out + products(i)
end loop
        valid_out <= '1';
      else
      valid_out <= '0';
```

The algorithm works as when valid input signal is available or logic 1, for every rising edge clock, if reset is enabled outputs will be by default zero else the filter coefficients are updated with the multiplier and adder modules as mentioned.

4. RESULTS AND DISCUSSION

The designs are modelled in Verilog hardware description language (VHDL) language. The designs are verified for Cyclone III FPGA with part number EP3C40F780C8 in Quartus II Tools. It consists of 39600 logic elements, operates at 1.2V core voltage, with 536 user I/O pins. Here the area is evaluated in terms of logic elements (out of 39600). The RTL schematic of the reconfigurable filter for 8 taps and 8 bit word length is as shown in Figure 3.

The Table 1 shows the details of the reconfigurable FIR Filter using pipelining with maximum possible number of taps and number of bits processed at a time. It shows that as the number of taps increases, the area occupied nearly doubles. The delay also increases by 35.3% along with power dissipation by 3.9% but the maximum possible frequency of operation decreases by 10.7%.

The Table 2 shows the details of the power dissipation for reconfigurable FIR filter. It shows that as the dynamic power remained constant at 0 but very slight changes of 0.07% occur in static power but as number of taps or bits increase, it increases I/O power by atleast 18.1%. Figure 4 presents the performance trade-off comparison of the reconfigurable FIR filter in terms of area, delay, power, and maximum frequency. Figure 5 illustrates the power performance analysis of the filter with different tap and bit-width configurations, highlighting the changes in static and I/O power.

Table 1. Reconfigurable FIR filter with specific taps with pipelining

#Taps	#Bits	Area (logic elements)	Delay (ns)	Power dissipation (mW)	Fmax (MHz)
4	8	79	1.534	109.21	182.72
4	16	151	2.371	113.72	143.23
4	32	718	3.962	122.77	95.97
8	8	185	2.868	112.22	123.29
8	16	353	3.799	119.75	100.55
8	32	1632	4.645	134.85	85.63
16	8	397	4.098	118.24	93.14
16	16	819	4.652	131.79	83.82
32	8	963	4.731	130.29	80.68

Table 2. Reconfigurable FIR filter with detailed power dissipation

#Taps	#Bits	Power dissipation (mW)	Static power (mW)	I/O power (mW)
4	8	109.21	88.86	20.35
4	16	113.72	88.86	24.85
4	32	122.77	88.93	33.84
8	8	112.22	88.87	23.35
8	16	119.75	88.90	30.84
8	32	134.85	89.01	45.84
16	8	118.24	88.90	29.35
16	16	131.79	88.95	42.84
32	8	130.29	88.95	41.34

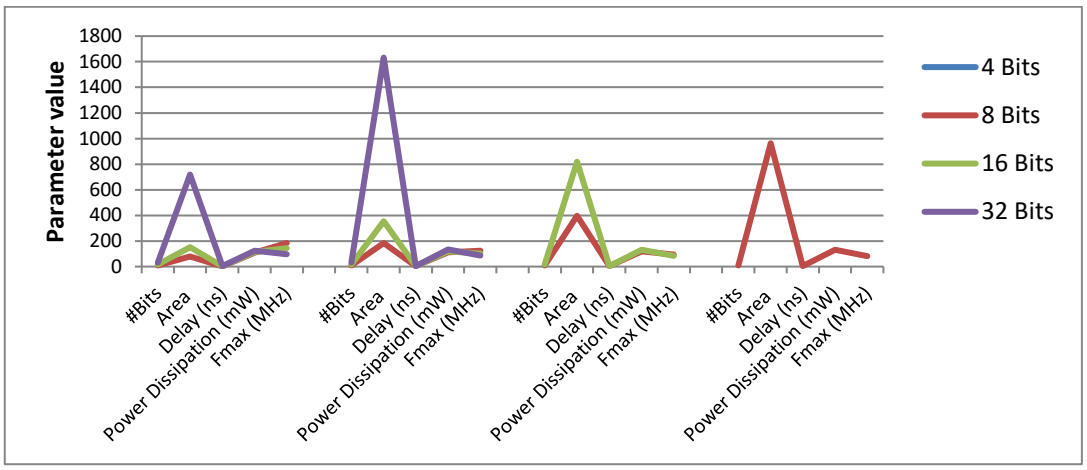

Figure 4. Performance trade off comparison analyses of proposed reconfigurable FIR filter

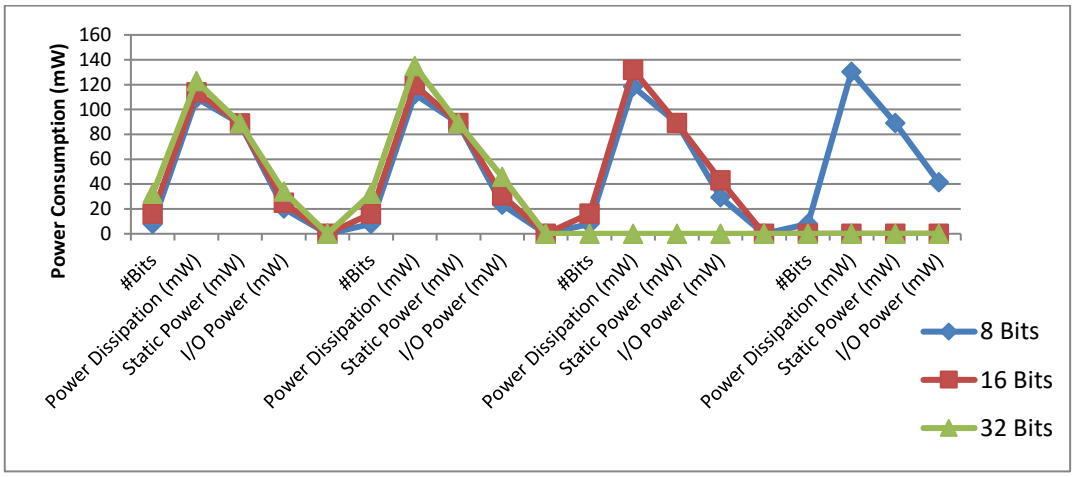

Figure 5. Power performance analysis of different tap reconfigurable FIR filter

5. CONCLUSION

The reconfigurable FIR filters are used to configure as per the incoming data stream density to save bandwidth and to handle higher data rates of 20 Gigabits per second to support 5G communication. The imposed challenges include need for enhanced data processing capability with low power and low area requirements. The proposed pipelined reconfigurable FIR filter is modelled in VHDL language, synthesized for Cyclone III FPGA. The results prove that for the proposed filter, as the number of taps increases, the area occupied nearly doubles. The delay also increases by 35.3% along with power dissipation by 3.9% but the maximum possible frequency of operation decreases by 10.7%.

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