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An active two-stage class-J power amplifier design for smart grid's 5G wireless networks

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ABSTRACT

The wireless communication networks in the smart grid's advanced metering infrastructure (AMI) applications need 5G technology to support large data transmission efficiently. As the 5G wireless communication network's overall bandwidth (BW) and efficiency depend on its power amplifier (PA), in this work, a two-stage class-J power amplifier's design methodology that operates at 3.5 GHz centre frequency by utilizing the CGH40010F model gallium nitride (GaN) transistor is presented. The proposed design methodology involves proper designing of input, output, and interstage matching networks to achieve class-J operation with improved power gain over desired BW using the advanced design system (ADS) electronic design automation (EDA) tool and estimating its integration feasibility through active element-based design approach using the Mentor Graphics EDA tool. The proposed PA provides 54% drain efficiency (D.E), 53% power added efficiency (PAE) with a small signal gain of 27 dB at 3.5 GHz and 41 dBm power output with 21 dB of improved power gain across a BW of around 400 MHz using 28 V power supply into 50 Ω load. By replacing the two-stage PA's passive elements with active elements, its layout size is estimated to be (15.5×29.2) μm^2. The results of the proposed PA exhibit its integration feasibility and suitability for the smart grid's 5G wireless networks.

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1. INTRODUCTION

With the revolution in wireless communication technology, along with the "mobile communication sector," the "power sector" also has a significant need for upcoming 5G technology [1], especially for the smart grid's wireless communications, due to the enormous rise in the data to be transmitted. The smart grid includes communication technologies [2] and [3] that offer bidirectional data transfer in contrast to the conventional power grid for more reliable and efficient energy transmission and distribution. The advanced metering infrastructure (AMI)/smart metering applications [4] play a crucial role by enabling two-way communication for transmitting a large amount of data between the meter data management system (MDMS) of the operation centre and smart meters in the smart grid. To overcome the practical limitation in the centralized communication architecture of AMI, such as congestion or loss of data due to the rapid increase in the smart meters count and their frequent readings, a distributed architecture [5] can be used, wherein the smart meters data collected using data concentrators will be transmitted to the MDMS of the distributed operation centre using a suitable communication technology, which improves the communication architecture's efficiency and cost-effectiveness [6].

Therefore, based on the communication requirements [7] and the necessity of 5G technology in smart grid [8], the existing (3G/4G) wireless communication networks used for transmitting the data from data concentrators to the distributed operation centre can be replaced with the 5G wireless communication networks. The deployment of 5G technology will offer the reliability and desirable bandwidth (BW) to support large data transfer in the AMI applications of the smart grid. The energy consumption and BW of the 5G wireless communication networks are two important factors to consider when deploying them in AMI/smart metering applications. It is well known that a wireless communication network's BW and total energy consumption are significantly influenced by its power amplifier (PA). Therefore, choosing a PA that complies with the standards of 5G wireless communication networks utilized in the smart grid's AMI is crucial. A variety of linear mode PAs, like class-A, class-B, and class-AB with lower efficiency, and switching PAs, which deliver higher efficiency with lower linearity, like class-E and class-F described in the existing methods [9]–[15] are restricted to narrow BW and not appropriate for wideband applications. However, the class-J PA [16] has demonstrated its ability to provide good efficiency and linearity across a broad BW.

Therefore, this paper proposes a design methodology for two-stage class-J PA that operates at 3.5 GHz centre frequency by utilizing the CGH40010F model gallium nitride (GaN) transistors, which is suitable for the 5G wireless communication networks in the smart grid's AMI applications. The design model and ideology of the proposed two-stage PA focus mainly on producing output power with improved power gain along with linearity and achieving integration feasibility. The proposed design methodology involves the following key steps: choosing the transistor and its technology, analyzing its load line impedances and stability, validating the driver and power stages using load pull and spectrum analysis, validating the full stage PA design using the input matching network ((IMN), output matching network (OMN) and interstage matching network (ISMN) and estimating its integration feasibility. Following its effective design methodology, the advanced design system (ADS) and the mentor graphics electronic design automation (EDA) tools were used to run schematic and layout simulations of the proposed two-stage PA respectively.

This manuscript is organized into the following sections. Section 1 involves an overview of AMI in the 5G smart grid, the scope and objective of this manuscript, a brief methodology of the proposed PA, and its expected outcomes. Section 2 describes the existing works on class-J PAs designed for various applications with the pros and cons of the respective authors. Section 3 explains the proposed two-stage PA's design methodology in detail using a flow chart. In section 4, the results of simulated two-stage PA are presented and compared with other PA designs. The paper's conclusion is summarized in section 5 based on the simulation results obtained.

2. LITERATURE REVIEW

Since the introduction of class-J mode PA by Wright *et al.* [16], researchers have reported several previous studies demonstrating its potential to obtain good efficiency and linearity across a broad BW. Various class-J PA designs were reviewed and analyzed to verify their suitability for upcoming 5G wireless networks utilized in the AMI applications for the smart grid. Among these, Rezaei *et al.* [17] presented a class-J PA design using GaN technology by considering its OMN element losses. However, it has a lower power output (P_{out}) and efficiency compared to discrete-type PAs due to low Q and device technological constraints. Dong *et al.* [18] proposed a class-J PA design based on complementary metal oxide semiconductor (CMOS) technology with its design equations updated based on the impact of threshold voltage to analyze second harmonic losses. However, due to lower breakdown voltage restriction, CMOS-staked FET design must be employed for PA design. In [19], [20] demonstrated a class-J PA with the realization of proper half-rectified sin waveforms at the transistor gate to improve its drain efficiency (D.E) and P_{out}. Although these methods are useful, this PA's design and implementation are complicated due to the need for additional circuitry for higher-order filters. Hanna *et al.* [21] presented a two-stage class-J PA design with 28 GHz centre frequency using CMOS technology, which achieves good efficiency over enhanced BW and reveals its suitability for wideband 5G wireless communication applications.

Liu *et al.* [22] proposed a 5 GHz class-J PA design suitable for WLAN 802.11ax applications using GaN technology, demonstrating promising performance and commercial value. However, its performance can be further enhanced if digital pre distortion (DPD) is employed. Gao *et al.* [23] proposed a class-J PA for the 5GHz frequency band by introducing a dynamic matching network (M.N) to follow its optimum impedance trajectory for achieving maximum efficiency in the broadband and the P_{out}. However, this dynamic M.N can be designed using active inductors (AI) to enhance its tunability. Alizadeh *et al.* [24] also proposed an active load modulation technique for an X-band class-J PA design to improve its feasibility for integration by eliminating the filter and doubler networks used in the conventional class-J2 PA. It can be noticed that there is a compromise in BW achievement as this work is focused only on improving efficiency. However, implementing a phase shifter network with an extended BW can enhance this PA's BW. Zhang *et*

al. [25] proposed a two-stage class-J PA design with a staked CMOS structure to achieve broad BW to implement in X-band. Although this PA has achieved enhanced BW, a staked structure must be employed to improve the P_{out} due to the lower breakdown voltage of CMOS technology. Nasri *et al.* [26] proposed a broadband class-J PA using the Doherty structure with two CGH40010F transistors and achieved a saturated power output of 43–44.2 dBm over broadband. However, this PA design can be made feasible for integration to reduce its chip area using an active element-based design approach.

Based on this review, the existing class-J PA designs reported to date proved that they can provide a potential solution for the efficiency, linearity, and BW trade-off. However, these class-J mode PAs were designed for different applications with different technologies (GaN or CMOS) using passive elements like spiral inductors or transmission/microstrip lines to realize their M.N. The transmission lines on an integrated circuit take up a lot of space despite their simple layout and design, directly affecting the circuit's size and price. On the other hand, spiral inductors have limitations like bulky size, fixed inductance value with low Q-factor, temperature sensitivity at higher frequencies, and incompatibility with conventional CMOS technology [27]. To overcome these disadvantages, the passive lumped/spiral inductors can be replaced with AI [28], which have more advantages like inductive tuning, better Q-factor, compatibility with CMOS technology, and chip size reduction. Various wireless application circuits such as voltage-controlled oscillators (VCO), low noise amplifiers (LNA), filters, and M.Ns have been implemented using AIs [29]-[32] to achieve tunability and save the chip area and cost. Therefore, the novelty of this work involves the design of a two-stage class-J PA and an AI that achieves tunable inductance and Q-factor for replacing the passive lumped inductor of its output matching network (OMN). It also involves estimating the proposed PA's chip area using an active element-based design approach to check its feasibility for integration and suitability for smart grid AMI's 5G wireless communication networks.

3. TWO-STAGE POWER AMPLIFIER DESIGN METHOD

A two-stage PA is proposed with a class-J mode power stage driven by a driver stage to achieve the desired performance metrics that satisfy the 5G wireless communication network's requirements in AMI of the smart grid. As the selection of operating frequency is an important consideration in the PA design, various frequency bands such as LTE and 5G new radio (NR) [33], [34] were analyzed for their appropriate selection. Based on the analysis, a new sub-6 GHz frequency band with 3.5 GHz centre frequency, called citizen broadband radio service (CBRS) [35], was chosen as it can be appropriate for 5G wireless communications of AMI in the smart grid. Therefore, the proposed PA was initially designed with a 3.5 GHz operating frequency, and its simulations were performed with the ADS EDA tool using a 10 W GaN transistor model (CGH40010F) from CREE. The main purpose of choosing a two-stage PA topology is to get the desired P_{out} by feeding it with lower input power. Class-A, B, AB, and C modes are often used for the driver stage design of two-stage PA. In this work class AB mode is chosen due to its low distortion compared to other modes. The step-by-step process involved in the proposed two-stage PA design methodology is described in detail with the help of the flowchart shown in Figure 1.

3.1. Transistor and its technology selection

As an initial step of the PA design, a GaN transistor is chosen for this work because of its high output power density, which makes it withstand high operational voltage [36] compared to gallium arsenide (GaAs) and CMOS, and they can also provide higher efficiency over wider BW. Among different GaN transistor large-signal models, a Cree's CGH40010F transistor from Wolf speed has been chosen as the main transistor because its features can provide the desired design specifications of the proposed two-stage PA.

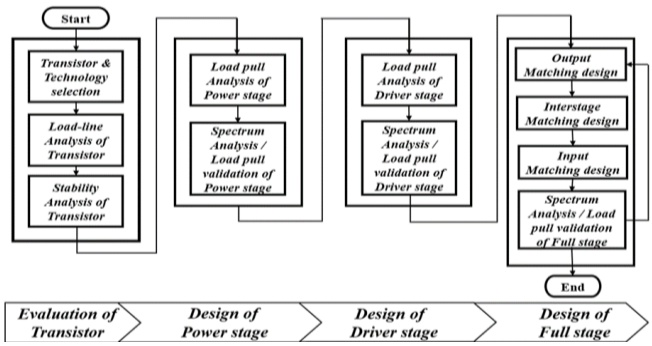


Figure 1. Two-stage PA design flowchart

3.2. Bias point selection and load line analysis

According to Wright *et al.* [16], the class-J mode operation of a transistor can be represented by its intrinsic drain voltage (V_{DS}) with a harmonic boost and phase shift along with the half-rectified drain current (I_D). The class-J mode V_{DS} and I_D waveforms can be obtained by presenting a complex impedance and a pure reactive impedance that can be expressed by (1) and (2) as fundamental and second harmonic loads to the selected transistor respectively, by biasing it with class-B mode.

$$Zf0 = \frac{(V_{DD}-V_{th})(1+j\alpha)}{Imax/2} = R_{opt} + j\alpha R_{opt} \quad (1)$$

$$Z_2f0 = -\frac{(V_{DD}-V_{th})j\alpha}{2\left(\frac{I_{max}}{3\pi}\right)} = -\frac{j3\pi}{8}\alpha R_{opt} \quad (2)$$

Where the optimum resistance (R_{opt}) can be represented using (3).

$$R_{opt} = 2(V_{DD} - V_{th})/I_{max} \quad (3)$$

Therefore, after selecting the transistor, the load-line analysis of the power stage was performed to obtain the class-J mode's target reference impedances. Based on this analysis, to achieve the maximum P_{out}, the selected transistor's drain is biased with a DC voltage of 28 V, which is the valid lowest V_{DS} that can be applied to allow the high swing in the drain voltage due to the harmonic boost in the class J operation mode up to its breakdown voltage of 84 V. The gate is biased with the near-threshold voltage (V_{th})≅-3 V to initially operate the device in class-B mode to obtain the desired half-rectified I_D. The V_{DS} of class-J mode operation can be theoretically expressed as shown in (4).

$$V_J(\theta) = V_{dc}(1 + sin\theta)(1 + \alpha cos\theta) \quad (4)$$

The "Alpha" factor (α), as shown in (4), can be varied from -1 to 1, and each V_{DS} waveform for different values of α results in the same theoretical efficiency when combined with half rectified I_D, causing the class-J mode to expand its BW.

For α=1, (4) can be expanded as shown in (5).

$$V_J(\theta) = V_{dc}(1 + sin\theta + cos\theta + \frac{1}{2}sin2\theta) \quad (5)$$

Therefore, when (α) is moved from "0" (i.e., class-B mode) to "1" on the slider, a harmonic boost and a phase shift can be noticed in V_{DS} due to the $sin2\theta$ and $cos\theta$ terms of (5) respectively, which resemble the class-J mode's V_{DS} and I_D waveforms as shown in Figure 2. The target reference load impedances corresponding to the class-J mode operation (for α=1), which are obtained from load line analysis using (1) and (2) are represented in Figure 3 using a Smith chart.

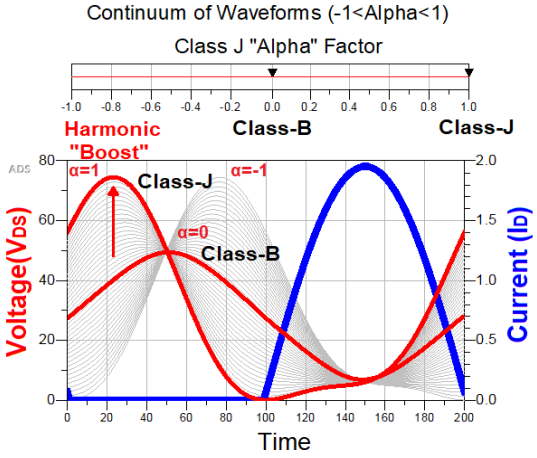


Figure 2. Class-B to J operation mode w.r.t α=0 to 1

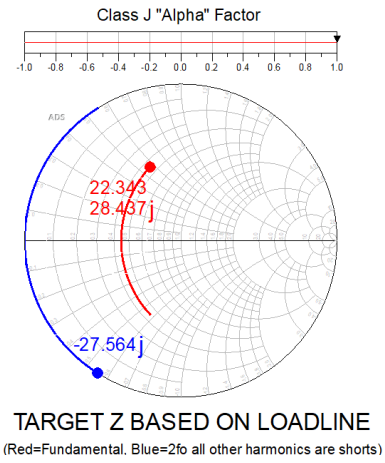


Figure 3. Target reference load impedances of class-J operation mode

Unlike the power stage, the driver stage drains and the gate bias voltages are set as 28 and -2.7 V, respectively, for the corresponding class-AB mode, and its target reference impedances are obtained directly from the CGH40010F device datasheet as 3.18-j*13.3 and 14.6+j*7.45. The selection of target reference impedances is verified by performing load line analysis using design equations in the ADS workspace.

3.3. Stability analysis

Once the power stage (class-J) and driver (class-AB) stage transistors are biased, their stability analysis was performed corresponding to the respective biasing points for a frequency range of (3-4) GHz using S-parameter network analyzer (SP_NWA) as shown in Figure 4. The unconditional stability of the transistors in the PA can be assured by satisfying two main conditions such as the Rollet stability factor (K) expressed in (6) must be greater than unity (i.e., K>1), and the stability measure (b) expressed in (7) must be a positive value (i.e.,>0).

$$K = \frac{\{1-|S_{11}|^2 -|S_{22}|^2+|S_{11*}S_{22}-S_{12*}S_{21}|^2\}}{\{2*|S_{12*}S_{21}|\}} \quad (6)$$

$$b = \{1 + |S_{11}|^2 - |S_{22}|^2 - |S_{11*}S_{22}-S_{12*}S_{21}|^2\} \quad (7)$$

In this work, a stabilization resistor of 5 Ω is connected with the transistor's gate terminal in series to ensure the transistor's unconditional stability by making (K>1) and (b>0) over a desired frequency range.

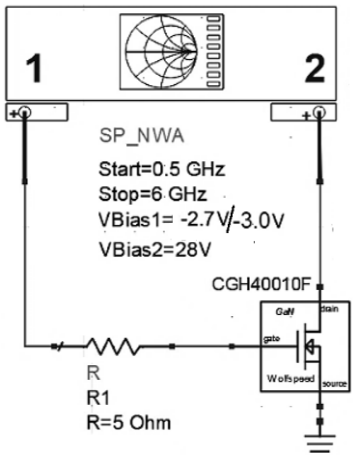


Figure 4. Stability analysis of a GaN transistor for driver and power stage

3.4. Load pull analysis

After ensuring the unconditional stability of the driver and power stage's transistors, their corresponding load-pull simulations were performed to get the optimum source (Z_S) and load (Z_L) impedances corresponding to the maximum power added efficiency (PAE) and the P_{out}. These Z_S and Z_L values obtained using load-pull analysis will be used for M.N's design. Load pull simulations can be performed on a large signal model of the GaN transistor (CGH40010F) using the harmonic balance (HB) 1-Tone load pull design guide in the ADS EDA tool. Initially, the transistor's fundamental source and load impedance values for power and driver stages obtained from load line analysis and device data sheet respectively are used as target reference impedances in the HB1-Tone load pull simulation setup, as shown in Figure 5.

The second harmonic of the driver stage was set at high impedance to keep it as an open circuit, wherein the power stage, the second harmonic impedance obtained from load line analysis, is used as the target reference impedance. The third harmonic impedance of the driver and power stages were set at high impedance to keep it as an open circuit, and other harmonics were terminated at 50 Ω. The fundamental and second harmonic load impedances at of power stage are crucial to obtaining the desired class-J operation with enhanced BW. The driver (class-AB) and power (class-J) stages with respective biasing voltages and input powers at 3.5 GHz RF frequency are validated by placing these Z_S and Z_L values at their corresponding transistor's terminals instead of their 50 Ω terminations.

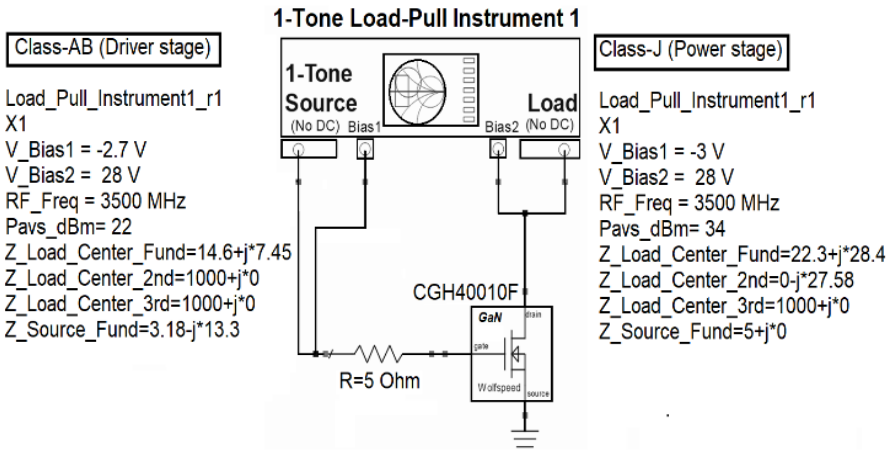


Figure 5. Load-pull analysis on the stabilized transistor for driver and power stage modes

3.5. IMN, OMN, and ISMN design

The next important step after validation of Z_S and Z_L is the design of appropriate M.Ns. Proper design of impedance M.Ns can improve the efficiency and BW of the proposed PA by mitigating the errors due to second-order effects. In general, harmonic distortion and intermodulation distortion are the crucial second-order effects that can affect the operation of the GaN transistor when a one-tone signal feeds the PA. The PA design should be optimized for low output impedance and high linearity to mitigate these harmonic and intermodulation distortions. By providing the proper impedance transformation between the source, transistor's terminals, and load, the M.Ns can minimize the reflections and improve power transfer efficiency, reducing harmonic and intermodulation distortion caused by impedance mismatch and improving overall performance. Proper M.Ns design also reduces the errors caused by the instability due to second-order effects such as variations in parasitic capacitances and can extend the usable BW.

Therefore, initially, to achieve approximately 500 MHz BW with 3.5 GHz centre frequency, 3 lumped element-based L, π, and T-type M.Ns were designed for corresponding IMN, OMN, and ISMN, because of the proposed PA's two-stage structure. The values of passive lumped inductors and capacitors in these L, π, and T-type M.Ns were calculated using their general design equations in terms of Q-factor. To validate the proper design of the M.Ns, the driver and power stage transistors are represented as "Z2P_Eqn" blocks by placing the optimum impedances Z_S and Z_L as Z [1,1], Z [2,2], and the S-parameters were measured for a desired frequency range of (3-4) GHz using the S-parameter sweep setup of the ADS EDA tool as shown in Figure 6. The transfer impedances of transistors ((i.e., Z [1,2] and Z [2,1]) are ignored, because the M.Ns will be designed to match only these Z [1,1] and Z [2,2]) of driver and power stage transistors with each other and also with the corresponding source and load terminations. In this work, as the GaN transistor is used in the class-J power stage as the active device, the second-order effects are taken care of by its drain-source capacitor (Cds), and the capacitor C3 of OMN as their values are considered as short circuit at higher harmonic frequencies.

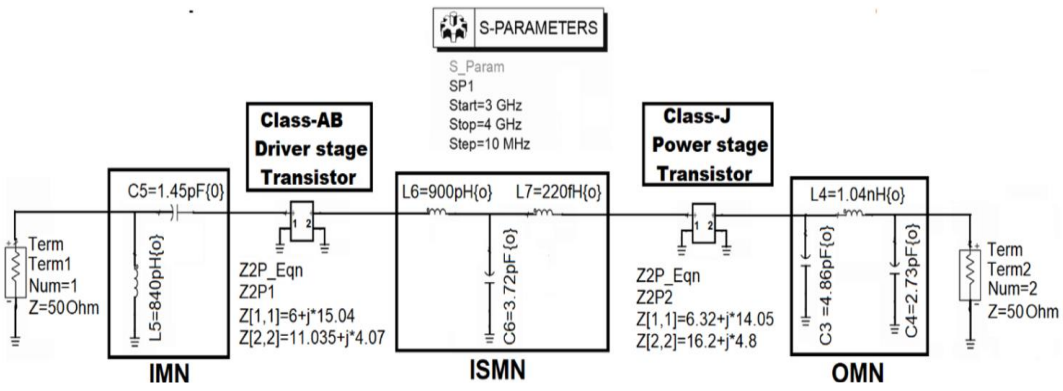


Figure 6. IMN, OMN, and ISMN with S-parameter sweep setup

3.6. Validation of proposed two-stage power amplifier

The proposed two-stage PA with 50 Ω terminations is validated by placing these designed passive lumped element-based M.Ns at the appropriate places, as shown in Figure 7, and optimizing them using the ADS optimization tool to get the desired performance. The passive lumped element-based M.Ns were initially realized to validate the proposed PA. Its simulated VDS and ID waveforms were observed to verify the standard class-J PA operating mode of the proposed PA's power stage. The validation of the proposed PA can be done by measuring its performance parameters such as P_{out}, gain, BW, D.E, and PAE using the HB simulator in the ADS tool when it is fed by input power (Pavs_dBm) of 20 dBm with 3.5 GHz operating frequency. After validation of the proposed two-stage PA design with passive lumped elements, its final layout design can be realized by replacing its ideal passive lumped elements with active elements (transistors) to check its feasibility for integration.

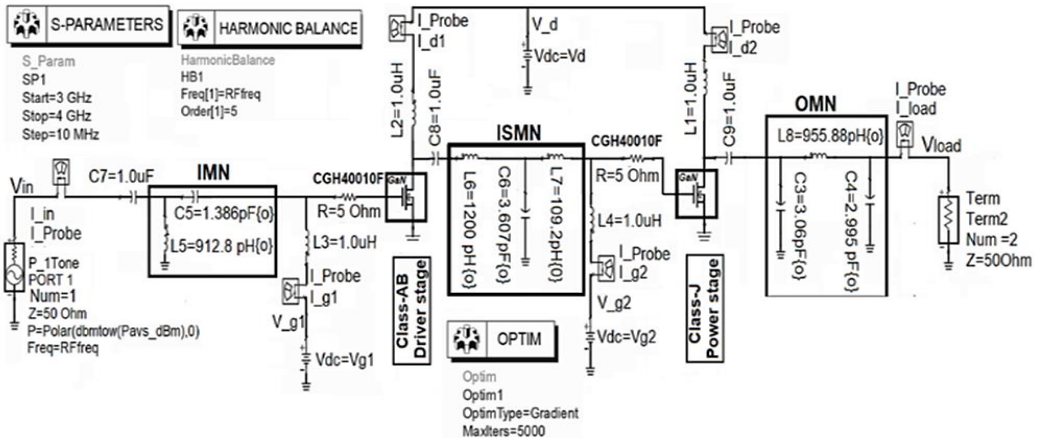


Figure 7. Proposed two-stage class-J PA's schematic circuit

3.7. Active inductor design

The proposed PA design was intended to replace its passive lumped elements with active elements to make it feasible for integration. Therefore, after validating the proposed PA design with passive lumped element-based M.Ns, as an initial step, an AI is designed to replace the passive lumped inductor in its OMN, as shown in Figure 8. The AI design allows us to overcome the disadvantages of commonly used spiral inductors [28] and achieves tunable inductance with reduced chip area.

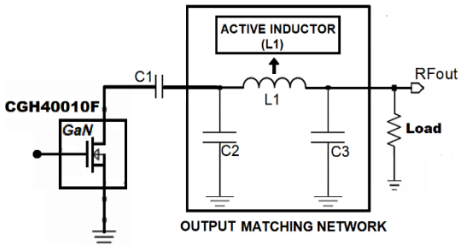


Figure 8. AI-based OMN for class-J PA

Therefore, after validating the proposed two-stage PA with lumped element-based M.Ns, as shown in Figure 7, different gyrator-C-based AI designs were reviewed and analyzed to replace its OMN's passive lumped inductor with AI. Based on the theory of gyrator-C topology, when two transconductors are connected back-to-back, it can be termed a gyrator. When a capacitor is connected to a gyrator's output, its equivalent input impedance can be synthesized as an inductor and termed gyrator-C- AI, as shown in Figure 9. Its basic topology can be represented in terms of transconductors as shown in Figure 9(a). By replacing the gyrator-C AI's transconductors with common drain and common source configured transistors (MOSFETs), respectively, as shown in Figure 9(b), its inductance along with the parasitic parameters can be depicted as shown in Figure 9(c) using an RLC equivalent circuit.

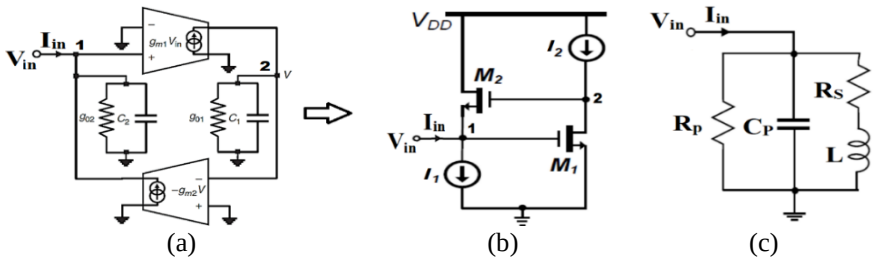


Figure 9. Gyrator-C AI (a) basic topology, (b) MOSFET-based topology, and (c) equivalent RLC circuit

The inductance (L) of the MOSFET-based gyrator-C AI, along with parasitic resistances (R_P, R_S) and capacitance (C_P), can be realized from its admittance (Y) expression as shown in (8) that is obtained by applying KCL at nodes 1 and 2.

$$Y = \frac{I_{in}}{V_{in}} = SC_{gs1} + g_{m1} + \frac{1}{S\left(\frac{C_{gs2}}{G_{m1}G_{m2}}\right)+\left(\frac{g_{ds1}}{G_{m1}G_{m2}}\right)} \tag{8}$$

This admittance (Y) expression of the gyrator-C AI shown in (8) is analogous to the admittance (Y) expression of its RLC equivalent circuit as shown in Figure 9(c), and it can be expressed as shown in (9).

$$Y = \frac{I_{in}}{V_{in}} = SC_P + \frac{1}{R_P} + \frac{1}{S(L)+(R_S)} \tag{9}$$

By comparing (8) and (9) the L of the MOSFET-based gyrator-C AI along with the equivalent RLC circuit parameters (R_P, R_S) and (C_P) are expressed in terms of the transistor's transconductances and internal capacitances as shown in (10).

$$L = \frac{C_{gs2}}{g_{m1}g_{m2}},\ R_s = \frac{g_{ds1}}{g_{m1}g_{m2}},\ R_P = \frac{1}{g_{m1}},\ C_p = C_{gs1} \tag{10}$$

The input impedance (Z_{in}) of the gyrator-C AI can be expressed as the inverse of Y in terms of equivalent RLC circuit parameters L, R_P, $R_{S,}$ and (C_P) as shown in (11).

$$Z_{in} = \frac{1}{Y} = \left(\frac{R_S}{C_pL}\right)\frac{S\frac{L}{R_S}+1}{S^2+S\left(\frac{1}{R_PC_p}+\frac{R_S}{L}\right)+\left\{\frac{R_p+R_S}{R_pC_pL}\right\}=\{\omega_0^2\}} \tag{11}$$

From (11), the self-resonating frequency ($\omega 0$) of this MOSFET-based gyrator-C AI when R_P>>R_S is expressed as shown in (12).

$$\omega 0 = \sqrt{\frac{R_p+R_S}{R_pC_pL}} = \sqrt{\frac{1}{C_pL}} = \sqrt{\frac{g_{m1}g_{m2}}{C_{gs1}C_{gs2}}} \tag{12}$$

The inductive frequency range of this gyrator-C AI can be (ωz> ω> $\omega 0$) where ωz is a lower bounded frequency that can be expressed as shown in (13).

$$\omega z = \frac{R_S}{L} = \frac{g_{ds1}}{C_{gs2}} \tag{13}$$

This MOSFET-based gyrator-C AI's quality (Q) factor at ω= $\omega 0$ can be obtained from Z_{in} expression in terms of the transistor's transconductances and internal capacitances, as shown in (14).

$$\mathrm{Q}(\omega 0) = \frac{Im[Z_{in}]}{Re[Z_{in}]} \cong \frac{\omega_0 L}{R_S} = \frac{1}{g_{ds1}}\sqrt{\frac{g_{m1}g_{m2}C_{gs2}}{C_{gs1}}} \tag{14}$$

From the expressions of the L and Q factor of MOSFET-based gyrator-C AI, it can be noticed that varying the widths of the transistors (M_1 and M_2) varies their transconductances and internal gate capacitances at the same time, due to which it is difficult to tune the L and Q factor independently.

Based on this analysis, in this work, an AI is designed using the Weng-Kuo cascode topology [31] for achieving a 1 nH inductance value at 3.5 GHz centre frequency for replacing the passive lumped inductor in OMN of the proposed PA. The main reason for choosing this topology is its ability to tune the L and Q factor independently which can be achieved by adding a MOSFET (M_1) in cascode to the main MOSFET of the basic MOSFET-based gyrator-C AI structure as shown in Figure 10(a). With this configuration, independent tuning of L and Q factors is possible because g_{m6} is proportional to I_1+I_3 while g_{m1} is only proportional to I_1. In addition, this topology benefits from less chip area and low power consumption compared to the passive lumped or spiral inductor during its integration.

Similar to the basic gyrator -C AI's RLC equivalent circuit parameters, this AI's equivalent circuit parameters that are obtained from its Z_{in} expression can be represented in terms of transconductances and parasitic capacitances of MOSFETs 1.2 and 6 as shown in (15):

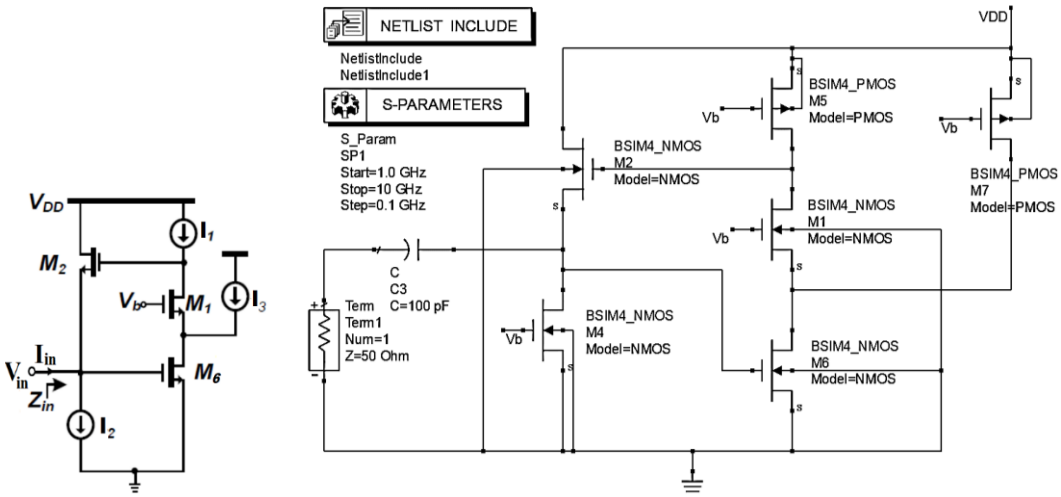
$$L = \frac{C_{gs2}}{g_{m6}g_{m2}}, R_s = \frac{g_{ds6}g_{ds1}}{g_{m6}g_{m2}g_{m1}}, R_P = \frac{1}{g_{ds2}+g_{m1}\approx g_{m1}}, C_p = C_{gs6} \quad (15)$$

the resonant frequency and corresponding Q-factor can be represented as shown in (16) and (17).

$$\omega 0 = \sqrt{\frac{g_{m6}g_{m2}}{C_{gs1}C_{gs2}}} \quad (16)$$

$$Q(\omega 0) = \frac{\omega_0 L}{R_S} = \frac{g_{m1}}{g_{ds6}g_{ds1}}\sqrt{\frac{g_{m6}g_{m2}C_{gs2}}{C_{gs1}}} \quad (17)$$

Therefore, an AI based on cascode topology as shown in Figure 10 is simulated with a gate bias (Vb)=1.5 V and a supply voltage (VDD)=3.3 V to obtain desired L and Q factor values, and the ideal current sources I_1, I_2 and I_3 in its topology as shown in Figure 10(a) are replaced with saturated MOSFETS M5, M4, and M7 as shown in Figure 10(b). The MOSFETs M_1, M_2, M_4, M_5, M_6, and M_7 W/L ratios of the AI are tuned and optimized for achieving a tunable inductance value of 1 nH≈956 pH (i.e., the passive lumped inductor's inductance value in OMN) at the 3.5 GHz centre frequency using S-parameter simulator.



(a) (b)

Figure 10. Cascode AI (a) topology and (b) schematic simulation in ADS

4. RESULTS AND DISCUSSION

The simulation results of proposed two-stage class J PAs are presented in the order of their design methodology steps. The proposed PA and the AI of its OMN are validated by evaluating their performance parameters. Finally, the integration feasibility and suitability of the proposed two-stage class-J PA for 5G wireless communication networks in smart grid's AMI are verified by performing its layout simulations with an active element-based design approach using the Silterra 0.13 μm process in MG EDA tool. The simulation results of all desired performance metrics of the proposed PA and the AI of its OMN are described as follows.

4.1. Stability

The simulation results of the stability analysis performed, as shown in Figure 4, reveal that the active device (i.e., GaN transistor) is unstable without any stabilization resistance as its stability factor (K) is <1. However, with the placement of a series resistance at the gate of the transistor, the stability factor analysis is represented in Figure 11. It is observed from Figure 11(a) and Figure 11(b) that the K becomes >1 and the stability measure is >0 over the desired frequency range (3-4) GHz which ensures the unconditional stability of the power and driver stage transistors.

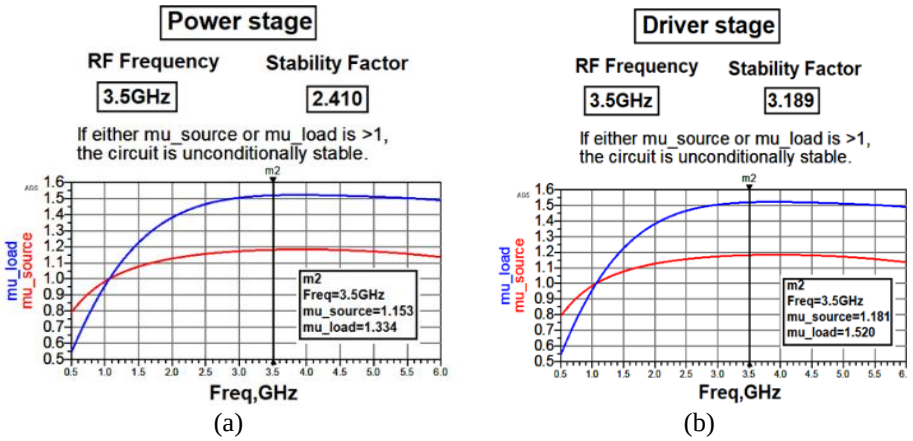


Figure 11. Stability factor analysis (a) power stage and (b) driver stage

4.2. Optimum input /source and output/load impedances from load pull

The simulator will measure the P_{out} and PAE from the load pull analysis and generate their contour plot for every swept point. Figure 12 shows the load pull simulation results where the optimum Z_S and Z_L of the power stage transistor obtained corresponding to maximum PAE are 6.322+j*14.053 and 16.212+j*4.793, respectively. Similarly, Figure 13 shows the optimum Z_S and Z_L of the driver stage transistor obtained corresponding to the maximum P_{out}/gain are 5.996+j*15.038 and 11.035+j*4.070, respectively. The values of Z_S and Z_L obtained from the simulation results of power and the driver stage's load-pull analysis corresponding to the maximum PAE and maximum power are shown in Table 1.

By presenting these optimum impedances at respective transistor terminals, the power and driver stages of the proposed two-stage PA are validated by computing their performance parameters using equations with the help of the "MeasEqn" component of the HB simulator in the ADS EDA tool respectively. From the validation of the power stage, it is observed that there is a harmonic boost in intrinsic drain voltage time domain signal (ts(X2.Q1.vdsi)) approximately up to 3 times (i.e., ≈84 V) of the supplied drain voltage of 28 V and a phase shift that reduces its overlap with half rectified drain current time domain signal (ts(-X2.Q1.idi)) as shown in Figure 14, which resembles the V_{DS} and I_D waveforms of class-J operation mode.

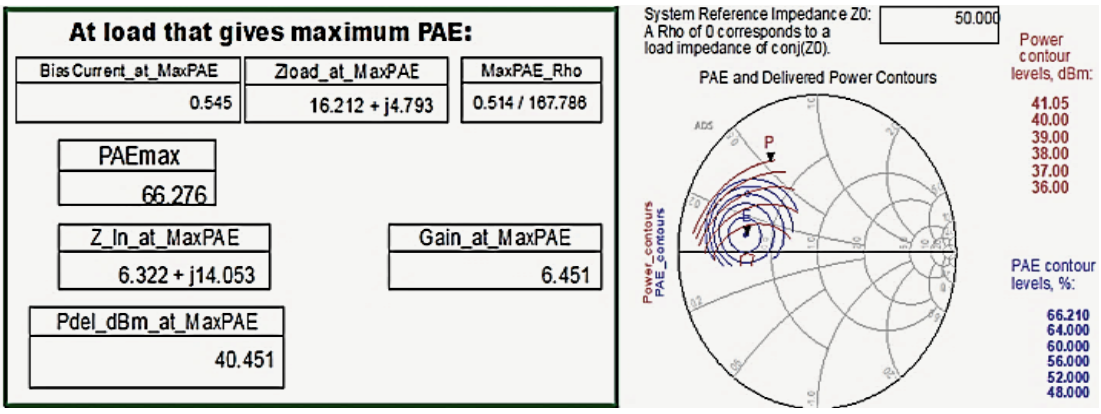


Figure 12. Optimum Z_S and Z_L of the power stage transistor w.r.t maximum PAE

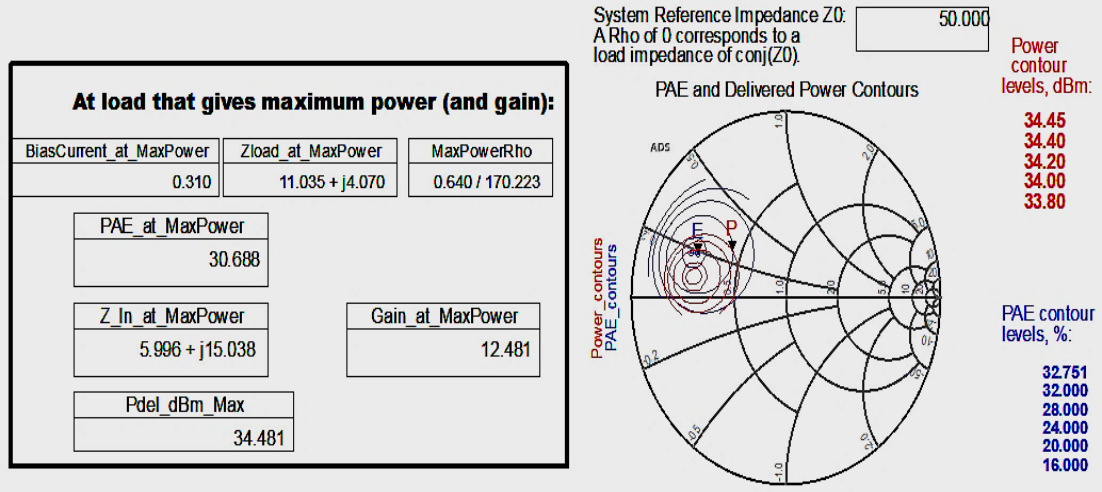


Figure 13. Optimum Z_S and Z_L of driver stage transistor w.r.t maximum power and gain

Table 1. Z_s and Z_L obtained from the load-pull analysis

Stage	Optimum impedance	Load pull analysis	Max PAE (%)	Max power (dBm)
Power	Source	6.32+j*14.0	@66	40.5
	Load	16.2+j*4.8		
Driver	Source	6.0+j*15.0	31	@34.5
	Load	11.0+j*4.0		

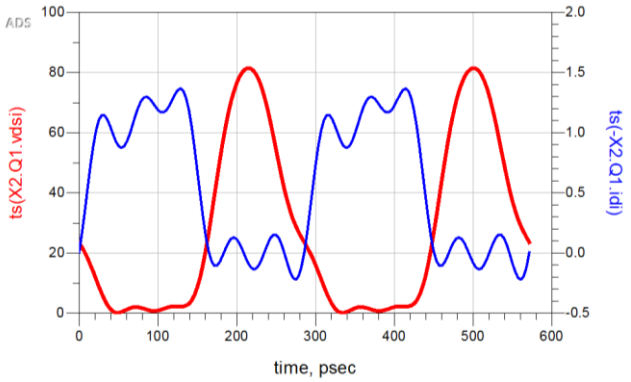


Figure 14. Intrinsic V_{DS} and I_D of power stage (class-J) transistor

4.3. Output power and efficiency

It is observed that by feeding the power stage (class-J) of the proposed PA with 34 dBm input power at 3.5 GHz centre frequency, its PAE, and D.E are estimated as 60.5% and 73.4%, and the P_{out} is estimated as 41.5 dBm with 7.5 dB power gain. Similarly, the driver stage delivers 34.9 dBm P_{out} with 12.9 dB power gain by feeding it with 22 dBm input power at 3.5 GHz centre frequency. Finally, by driving the class-J power stage with the class-AB driver stage using proper M.Ns design as shown in Figure 7, the proposed PA delivers 41.1 dBm P_{out} with 21.1 dB improved power gain, 54% D.E and 53% PAE using the reduced input power/ available source power (Pavs_dBm) of 20 dBm due to its two-stage structure. These performance parameters are tabulated as shown in Table 2.

Table 2. Performance parameters of two-stage PA

Stage	Pin (dBm)	LS_Gain (dB)	P_{out} (dBm)	PAE (%)	D.E (%)
Power (without M.Ns)	34	7.5	41.5	60.5	73.4
Driver (without M.Ns)	22	12.9	34.9	32	33
Two-stage (with M.Ns)	20	21.1	41.1	53	54

4.4. Performance over input power sweep

The variations of these performance parameters by sweeping the (Pavs_dBm) of the PA using the HB simulator are shown in Figure 15. These simulation results reveal that 54% D.E, 53% PAE as their maximum values, and 41 dBm P_{out} with 21 dB power gain were obtained for corresponding Pavs_dBm of 20 dBm. This improvement in the proposed two-stage PA's power gain is obtained at the cost of reducing its D.E and PAE. In general, the PAE and D.E of a GaN PA will not have the same values as they measure different aspects of the PA. However, the PAE and D.E of the proposed PA are close to each other because the load pull simulations of the proposed PA were performed to obtain optimum Z_L corresponding to maximum PAE, and it was initially designed using low-loss passive components and high-efficiency GaN transistor, resulting in minimal losses. The performance metrics of the proposed PA demonstrate its ability to achieve the desired P_{out} with improved power gain and linearity.

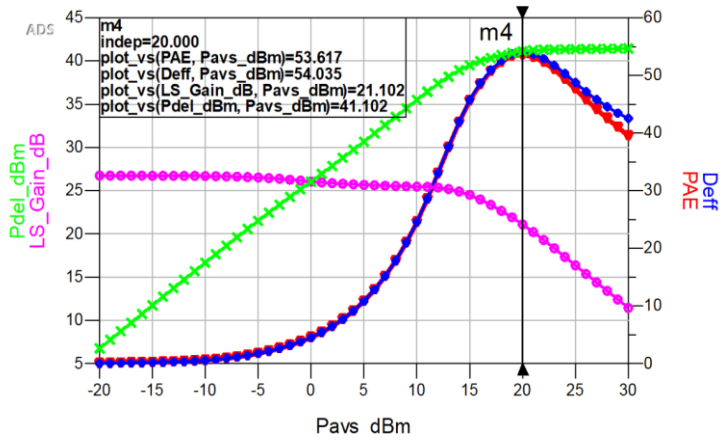


Figure 15. Two-stage PA's performance parameters w.r.t Pavs_dBm sweep

4.5. Bandwidth

Similarly, the variation of the proposed two-stage PA's performance parameters Vs RF frequency was measured using an HB simulator, and the respective simulation results reveal that D.E of 54%, PAE of 53% at 3.5 GHz centre frequency, and 41 dBm P_{out} with approximately 21 dB power gain is maintained across 400 MHz BW (i.e., 3.3 to 3.7 GHz) were obtained as shown in Figure 16. This enhanced BW demonstrates the proposed PA's ability to maintain its P_{out} and power gain across a wide frequency range and shows its suitability for next-generation 5G wireless networks of smart grid's AMI applications.

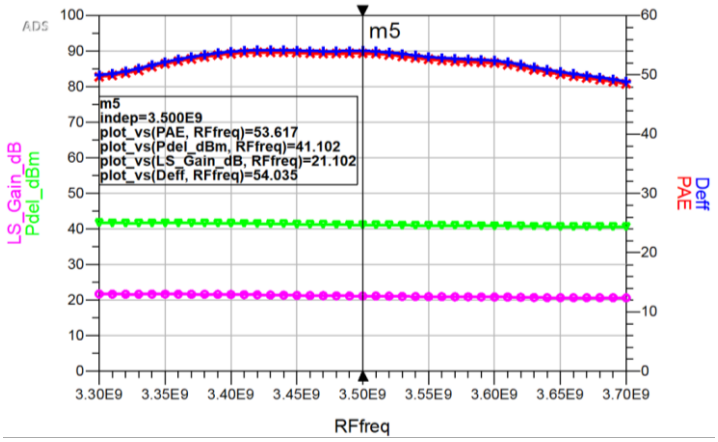


Figure 16. Two-stage PA's performance parameters w.r.t RF frequency

4.6. S-Parameters

The proper design of impedance-M.Ns of the optimized two-stage PA can be validated by measuring its S-parameters such as input, output reflection coefficients S (1,1), S (2,2), and small-signal gain S (2,1) using an S-parameter simulator of ADS EDA tool to ensure its improved interference resistance. It can be noticed that a small signal gain S (2,1) above 25 dB over 400 MHz BW (i.e., 3.3 to 3.7 MHz) with a maximum value of approximately 27 dB along with S (1,1), S (2,2)>-25 dB at 3.5 GHz centre frequency were obtained shown in Figure 17. These S-parameters ensure that the M.Ns are designed properly as the reflections are reduced which can reduce the impact of interference.

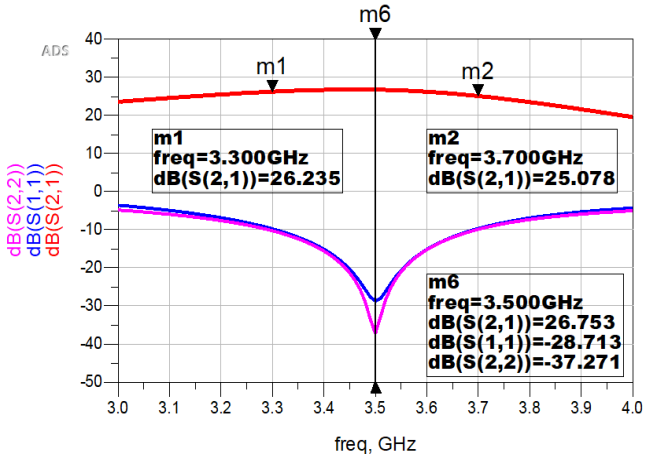


Figure 17. The proposed two-stage class AB/J PA's S-parameters

4.7. Issues of system interference resistance and error rate

Interference in a GaN PA refers to any unwanted signals that interfere with the proper operation of the PA, which can cause degradation in its performance. The various sources of interference, including other RF signals, electromagnetic interference (EMI), or thermal interference, can affect the performance and reliability of PA by introducing harmonic distortions into the output signal, leading the PAs to nonlinear behaviour. Therefore, improving the interference resistance while designing a PA is important to maintain its performance in the presence of external interference. In this work, the interference resistance of the proposed PA can be improved to mitigate the effects of interference by designing proper input/output impedance M.Ns, which can help to reduce reflections and distortions and improve the efficiency and linearity of the PA, which can help reduce the impact of interference.

On the other hand, the error rate of a PA refers to the frequency and severity of errors or distortions introduced into its output signal. The error rate can be measured in terms of bit error rate, adjacent channel power ratio, and error vector magnitude. The error rate of a GaN PA can be high due to various factors, such as input power levels, load impedance, operating frequency, and circuit design. In this work, the proposed PA's design is optimized to reduce distortions with proper impedance M.Ns that help achieve good linearity, reducing the error rate. Therefore, the improved interference resistance and reduced error rate of the proposed PA are assured by validating the M.Ns design through S-parameters and linearity measurements.

4.8. Linearity

In addition to the parameters such as DE, PAE, and BW of the PA, its linearity is also a crucial measure for performance evaluation. The linearity of a PA can be defined as a measure of how the PA produces an output that is a scaled version of the input signal without any distortion or nonlinear effects. The linearity of the PA may generally be evaluated using metrics like P1dB/P3dB (1 dB/3 dB compression point), third-order intercept point, AM-PM distortion, and adjacent channel power ratio, depending on its RF input signal and transistor technology used.

In this work, the proposed PA's linearity is evaluated using a 3 dB compression point as it is initially designed using a GaN transistor and fed by a continuous wave (CW)/1-tone signal as its RF input. The 3 dB compression point is defined as the point at which the gain of the PA begins to compress due to nonlinearity, and the output power no longer increases linearly with the input power. According to the simulation findings, the gain of the proposed PA is compressed by 3 dB (from 25.4 dB to 22.4 dB), as shown

in Figure 18. At this 3 dB compression point, the P_{out} value is 41 dBm, which is nearly as high as the saturated power (P_{sat}) value (i.e., 41.3 dB), which reveals that the proposed PA's linearity is good, reducing its error rate.

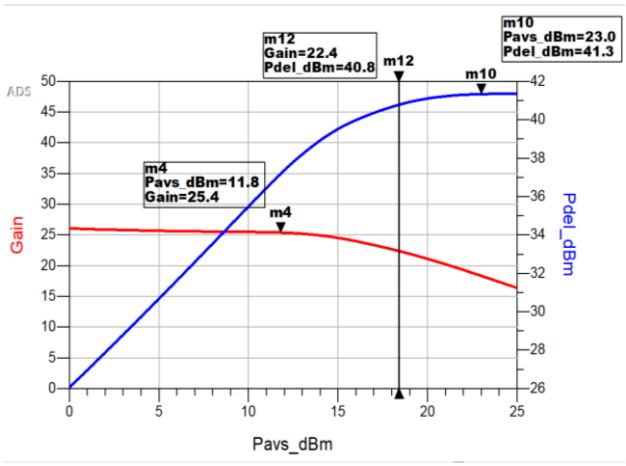


Figure 18. Linearity measurement using 3 dB compression point

4.9. Q factor and L of AI

After validation of lumped element-based two-stage PA's simulation results, the AI's schematic simulation was performed as shown in Figure 10(b), and by tuning the widths of MOSFETs in the AI an inductance value of 1 nH with a Q factor of 20 at 3.5 GHz was obtained, as shown in Figure 19. As this inductance value is almost equal to the value of the passive lumped inductor in the OMN of the proposed PA, it can be replaced with this AI to achieve tunability, reduced chip area, and less power consumption.

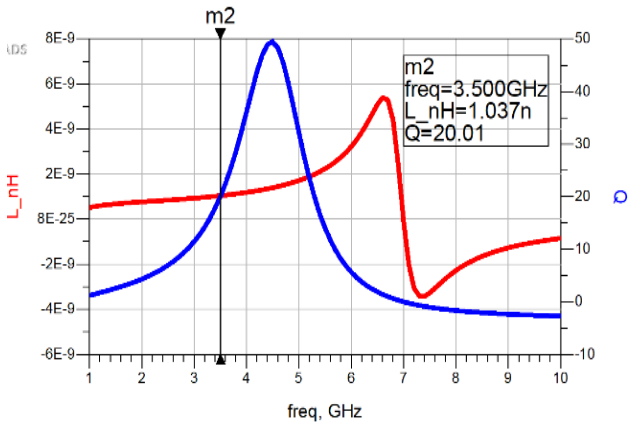


Figure 19. Q-factor and L of AI (vs) frequency

4.10. Proposed PA's layout design

Therefore, after validating the proposed two-stage PA's performance with lumped-element based M.Ns design, the layout design was performed to assess its integration feasibility and chip size. As the proposed PA of this work was initially designed using passive lumped elements, its final layout design is realized by replacing all of them with active elements such as the AI of OMN. The proposed PA's active element-based layout design was performed using the mentor graphics EDA tool. Since the load pull simulations cannot be performed using this tool, the R_{opt} values of the driver and power stages obtained using the ADS tool were taken as reference values. To get these reference R_{opt} values, the I_D of chosen Silterra Nmos transistors in the mentor graphics EDA tool were tuned by changing their aspect ratios.

Finally, by replacing all the elements in the proposed two-stage PA with Silterra 130 nm transistors and optimizing them as closely as possible, the chip size of its layout design shown in Figure 20 is estimated as (15.5×29.2) μm^2.

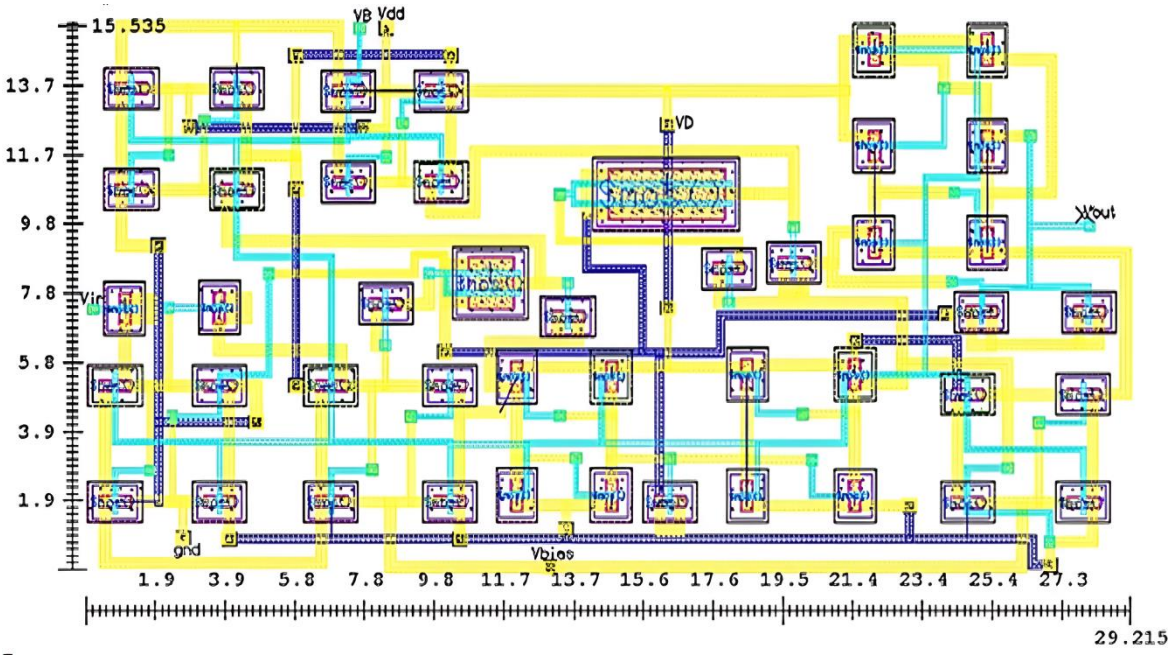


Figure 20. The proposed two-stage PA's active element-based core layout

4.11. Performance comparison

The proposed two-stage PA's performance parameters were compared with similar PAs in the literature, as shown in Table 3. The following are the noteworthy points by comparing the proposed PA's performance with recent similar PAs that were designed with different operating frequencies and technologies. A 5 GHz class-J PA design [22] suitable for WLAN 802.11ax applications using GaN technology delivers 55% maximum PAE and 38 dBm $P_{out,}$ whereas the proposed PA delivers 41 dBm of max P_{out} with 2-stage structure. However, this PA's power gain is comparatively higher than the proposed PA due to its 3-stage structure. A dynamic M.N-based class-J PA design [23] that operates at a 5G frequency band delivers a P_{sat} of 39.8 dBm and a maximum PAE of 50.6%. Our class-J PA delivers a maximum PAE of 53% with a max P_{out} of 41 dBm using the same GaN transistor with lower input power. However, the performance of PA can be further improved using an AI-based OMN structure.

A class-J PA with the 2-stage structure design using an active load modulation technique for the X-band presented in [24] eliminates the class-J2 PA's filter and doubler networks to improve its feasibility for integration. It delivers 50% PAE using an auxiliary circuit for phase-shifting that may require additional space. Whereas our proposed PA of this work delivers a PAE of 53% using a similar 2-stage structure without any auxiliary network for phase-shifting. A two-stage class-J PA design with a staked CMOS structure [25] delivers a max P_{out} of 20.2 dBm with 15 dB power gain and 29.7% PAE. Using a similar 2-stage structure, the PA of this work based on a GaN transistor delivers a max P_{out} of 41 dBm with 21 dB power gain and 53% PAE without any stacked structure due to its high-power handling capability. Using the Doherty structure, a broadband class-J PA presented in [26] achieved a saturated power output of 43–44.2 dBm and a small signal gain of 10–13 dB. In comparison, using a two-stage structure, our class-J PA provides a max P_{out} of 41 dBm with 21 dB power gain and a small signal gain of approximately 26 dB with the same number of transistors.

Moreover, the class-J PA designs in literature utilized transmission/microstrip lines or spiral inductors for realizing their M.Ns, which leads to large chip areas and high-power consumption. Compared to these existing class-J PA designs, the unique contribution of the proposed two-stage class-J PA is its active element-based layout design approach using AI for its OMN, which exhibits its feasibility for very large scale integration (VLSI) integration. In addition, the design methodology of proposed PA demonstrates its

potential for enhancing wireless communication capabilities in embedded, reconfigurable systems within the smart grid.

Table 3. Performance comparison

Ref./Parameters	[22] 2018	[23] 2020	[24] 2020	[25] 2021	[26] 2022	This work
Technology	GaN	GaN	GaAs	CMOS	GaN	GaN
Frequency [GHz]	5	3.7	10	9.5	3.5	3.5
BW [GHz]	4.9–5.9	3.3-4.2	9.1–10.8	8.7-11.8	3.0-3.7	3.3–3.7
Max P_{out} [dBm]	37.7	39.8	29	20	44.2	41
Max gain [dB]	31.7	-	12	15	13	21
Max PAE [%]	54.6	50.6	50	29.7	-	53
Max D.E [%]	-	-	71	-	74	54

5. CONCLUSION

This work presents a class-J PA with a two-stage structure, suitable for upcoming 5G wireless networks used in the smart grid's AMI applications. The proposed PA was designed with a 3.5 GHz operating frequency (i.e., sub-6 GHz 5G frequency) using lumped element-based M.Ns based on a two-stage PA design flow chart, and its simulations were performed using the ADS EDA tool. Its simulation results demonstrate that the proposed two-stage PA delivers 54% D.E, 53% PAE at 3.5 GHz centre frequency with 27 dB small signal gain and 41 dBm P_{out} with approximately 21 dB of improved power gain over a 400 MHz BW (i.e., 3.3 to 3.7 GHz).

Although the proposed two-stage PA with lumped element-based M.Ns exhibits good performance parameters, its overall size can be reduced to make it feasible for integration by replacing its passive lumped elements with active element designs. Therefore, as an initial step, an AI based on the Weng-Kuo cascode topology is designed and simulated to replace the passive lumped inductor in OMN of the proposed PA. In addition, by replacing its other passive lumped elements with active elements, the proposed PA layout's chip size is estimated as (15.5×29.2) μm^2, indicating its integration feasibility. However, there is scope for enhancing the proposed PA's performance with improved active-element-based designs to make it more appropriate for (sub-6 GHz) AMI/smart metering applications of 5G smart grid.

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