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FPGA in hardware description language based digital clock alarm system with 24-hr format

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ABSTRACT

Currently, digital clock adapts microprocessor or microcontroller system. Performance of speed and reconfigurability issue become a main concern in digital clocks. New additional feature may be introduced in digital clocks in the future. Field programmable gate array (FPGA) offer better performance of speed and reconfiguration features. Based on these advantages, it is essential to study or explore the digital clock with FPGA design. The objective in this study is to create a hardware description language (HDL)-based digital clock with alarm system and implement it onto the Altera DE2-115 board. Using Verilog HDL language in Quartus Prime 20.1 Lite Edition software, all submodule components is developed and being test benched using ModelSim-Altera Starter Edition 13.1 to ensure the correct functionality. Then all inputs and outputs will be assigned through pin assignment in the software. For verification purpose, it will be downloaded to the Altera DE2-115 board. In conclusion, the file has been successfully implemented to the board and the digital clock with alarm is fully functional as expected. This was proved by the alarm signal, time adjustment and display of the three-display mode which is clock, alarm, and input where each mode carries their own functions as expected.

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1. INTRODUCTION

An alarm clock is one of the devices which is very useful in human live. It solved a problem that everyone faces, which is determining the current time and also helping up to wake after sleep using alarm system. With this device, everyone can have a manageable and coordinated life.

Today, technology has progressed to the point where a system may be integrated onto a single chip, a process called as system on chip (SOC) [1], [2]. Likewise, this also applies to the digital clock. The system is currently comprised of a microprocessor [2], [3]. The problem related to the digital clock with the microprocessor is the performance of processing speed [4], [5] and reprogrammability issue [6], [7]. Following the trend of the period, numerous additional features may be incorporated in the future [8]. Therefore, it is essential to study the implementation of field programmable gate array (FPGA) in a digital clock [9]. Digital clocks use FPGA technology because it has a simpler circuit topology [10], quicker development cycle [11], and faster running speed [12]. FPGA is also used to solve the issue regarding on reprogrammability of the system [13]. FPGA can be used to solved complicated computational issues which requires increased speed and reprogrammability advantage [14]. It is explained that FPGA implementation is

superior to microcontroller or microprocessor since it is favourable in terms of performance and reconfigurable [15], making it easier to enhance the existing system [13].

The objective of this project is to create an hardware description language (HDL)-based digital clock with alarm system and implement it on an FPGA board in order to resolve the issue. To fulfil the objective, a digital clock with alarm system must be designed utilizing the verilog HDL programming language. The system's functionality will then be validated using ModelSim Altera Starter Edition for Quartus Prime 20.1 Lite Edition. It will then be implemented on an FPGA board for verification purposes. This study focuses on a 24-hour clock with an alarm system. This comprised coding, code analysis and synthesis, input and output pin assignments, compilation of the system, and download to the Altera DE2-115 FPGA board.

The main advantage of FPGA is its performance of speed. The high speed of an FPGA is a result of the system's I/O bandwidth to local memory, pipelining, and parallelism features [16], [17]. Parallel processing is one of the features that distinguishes FPGA from other processor types [18], [19]. FPGA is substantially superior to microcontrollers in terms of speed, I/O count, and performance [20]. Rodriguez-Andina *et al.* [21] stated that internal memory is essential for enhancing processing performance and optimizing I/O pin utilization. In addition, internal memory blocks offer the benefit of constructing complex functions, such as counters and multipliers. While digital clocks can be built using a variety of technologies, FPGAs offer major benefits such as a greater number of I/O ports [17]. It is desirable to explore digital clocks using FPGA due to their reduced system usage, increased system reliability, and increased working speed [12], [22] likewise, due to the advantages of a simpler circuit construction and faster operation, explained it is essential to analyze the digital clock using FPGA.

As compared to application-specific integrated circuits (ASICs), FPGAs have simpler design cycle in which means the design tools take care of a major function by themselves, such as placement, routing, and timing in reference to specifications that need to be set [23]. Apart from that, although the product has been finalised, built, and delivered, it may be easily updated, adapted, and reprogrammable. FPGAs are ideal for time-critical systems [24] and is the right solution if the application requires constant bug fixes, feature, design changes, and software flexibility. Table 1 summarizes performance of FPGAs to microcontrollers and ASICs across various aspects.

Like any other microcontrollers, FPGA also facing reprogrammable issues in which one of the solutions presented in this paper is to simulate the developed Verilog coding using ModelSim-Altera Starter Edition 13.1 software. The output is presented in timing waveforms. From these generated output waveforms, it can be compared with the expected output.

Table 1. Comparison of FPGA to another microcontroller and ASIC [23], [25], [26]

Aspect	Microcontroller	FPGA	ASIC
Flexibility during development	High	High	High
Flexibility after development	High	High	Low
Performance	Low	Medium	High
Power consumption	High	Medium	Low
Development cost	Low	Medium	High

2. RESEARCH METHOD

Figure 1 depicts the design of the top module of a digital alarm clock. There are 14 inputs including 50 MHz clock and 8 outputs. The input ports were listed as shown in the following diagram. The inputs for 'Reset' are used to reset all operations to zero. Consequently, the clock time, alarm time, input time, and alarm time switch to zero. While 'clock_50 MHz' is generated from a 50 MHz clock source. The frequency was subsequently decreased to 1 Hz to match the duration of 1 s during clock operation. Load data time (LD_time) is the switch that loads the input time into the clock. While 'LD_alarm' loaded input time into the alarm time. The 'Increment button' is utilized to assign values to inputs. As it is pressed, the time will be increased by 1 unit, depending on which switch is active at the time: switch Hin_1, which corresponds to the most significant hour, or switch Hin_0, which relates to the least significant hour. This was also applied to minutes. The 'ctime' switch is used to display the current time. 'atime' is used to display alarm time, whereas 'stime' displays input time. The 'AL_ON' switch activates the alarm system, while the 'STOP_al' switch deactivates it.

Figure 2 shows the overall components of submodule used for this study. It consists the submodules of clock reducer, time input, clock function, clock output, current time, and alarm function. All submodules were tested with their own testbench coding to ensure the functionality of each submodule. In clock reducer, the input of this module is 50 MHz clock and reset. It was then reduced to 1 Hz clock which equivalent to 1 s for operation in time input, clock function, and alarm function. In this module, it uses counter to count for 1 s clock production. If the counter is equal to 25,000,000, the 1 s clock will change in state from high to low.

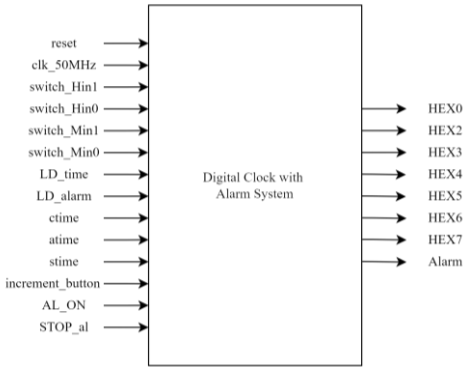

Figure 1. Top module of a digital clock alarm system

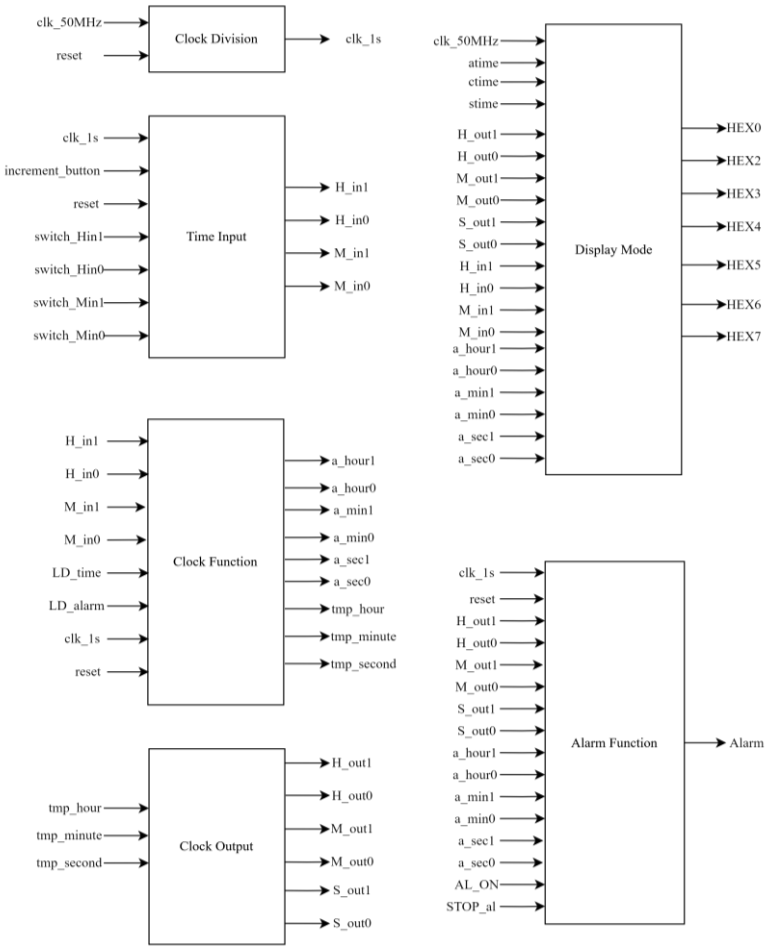

Figure 2. Submodule for digital alarm clock system

The reason why 25,000,000 count is used as the clock consists of 2 states, high and low. Each will be representing 0.5 s. To make 1 s clock, each state must have the count of 25,000,000 before changing to another state. If the counter reaches its target, it will reset back to zero. In time input, the user need to insert their desired time for clock time or alarm time using 4 switches which H_in1, H_in0, M_in1, and M in0. These switches representing the hour and the minutes, most and least significant digit. Each push of increment_button will increase the input value by 1. The value will reset if it exceeds the maximum pre-set value of clock time. If reset switch is turned on, all input will reset to 0. In clock function, this is where the input from user will be loaded either to clock time or alarm time. If LD time is switched on, the input will be loaded to the clock time. While LD_alarm will load the input into alarm time. This module also where the

clock time operates through counters through seconds, hour and minutes. In clock output, the internal clock time know as temporary (tmp) will be converted to 6 types of output for clock time display. It includes most significant and least significant of hours, minutes and seconds. In current time, it utilized 3 types of input which is clock time, alarm time, and setting time. The users can choose to see which type of display they want to see using 3 switches. The switches are 'ctime' which displays current clock time, 'atime' for displaying the alarm time and 'stime' for input time. And all of the input will be assigned to 7 different seven-segment displays. The arrangement of seven-segment display is 7'b (6 5 4 3 2 1 0). Seven segment display is active low meaning than logic low will light up the character of display. While logic high will turn off the character. In alarm function, it will compare the clock time and the alarm time. If both are similar and the switch AL_ON is on, the alarm will be turned on. In this case, the red LED will represent the alarm. If AL_ON is not on, the Alarm will not be turned on. To stop the alarm, user must switch STOP AL_ON. The flowchart of a digital clock with alarm system is depicted in Figure 3. This digital clock has three display modes. The user can choose between the clock, alarm, and set times. If the user selects reset switch, all time modes are reset to 0. If the user does not activate any of the three display switches, the seven-segment display will be blank. With input time mode, the user may also provide input to edit the clock time and alarm time. There are four switches to choose which portion of time is to be modified. Two are the maximum and minimum hours, while the other two are the maximum and minimum minutes. If the user presses the increment button, the value will grow by one. If the value of H_in1 is more than 2, for instance, it will be reset to zero. And it will continue if the button is still pressed. This will facilitate the user's input. If the user activates the LD time switch, the input will be set to clock time. The input will be loaded at alarm time for LD alarm. If AL_ON is enabled, the Alarm will be triggered if the clock time coincides with the alarm time.

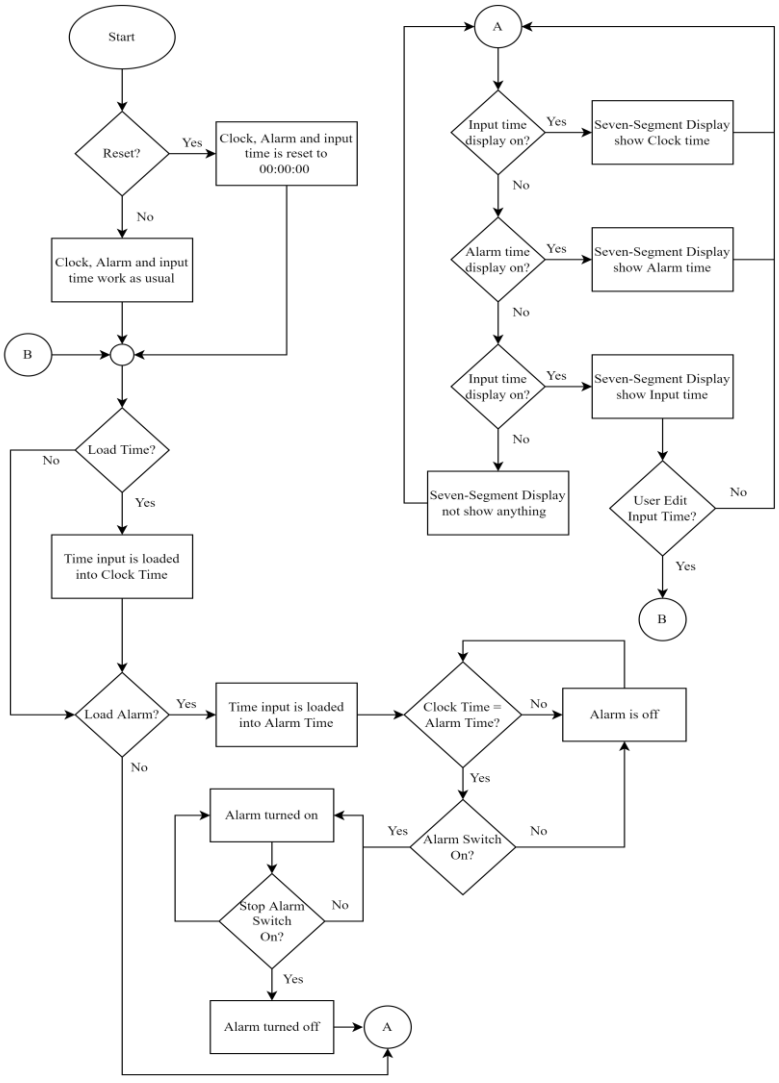

Figure 3. Flowchart of digital clock alarm system

3. RESULTS AND DISCUSSION

In this section, it is divided into 2 categories: software simulation and hardware implementation. In the part of software simulation, ModelSim-Altera Starter Edition 13.1 had been used. Whereby for hardware implementation, Cyclone IV of Altera DE2-115 development and education board had been utilized for verification.

3.1. Software simulation

Figures 4 and 5 reflect the timing diagram for the top module of a digital alarm clock. When 'stime' is enabled, the seven-segment displays the time input. In this instance, switch Min0 is activated. If the 'increment button' was pressed, the input will be added to Min_0 by 1. Then, LD alarm is enabled, which loads the input with the alarm time. The current alarm time is 0001 hours. Seven-segment display output HEX0-HEX7 displays three types of display modes. It consists of 7'bit registers, with each of LED of a seven-segment display utilizing a bit of register. 7'b describes the configuration of seven-segment display (6 5 4 3 2 1 0). Seven-segment displays are low active type, therefore 0 input will illuminate the display while 1 will turn it off.

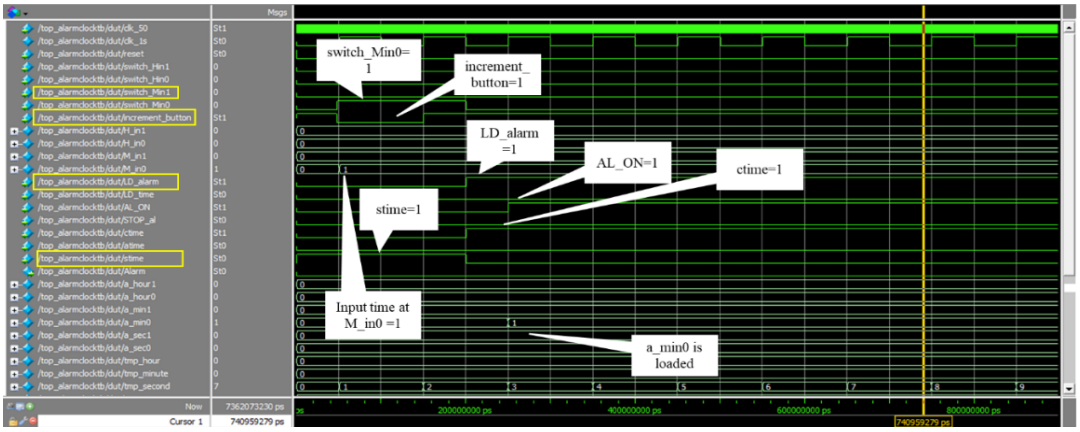

Figure 4. Timing diagram of time input for alarm time

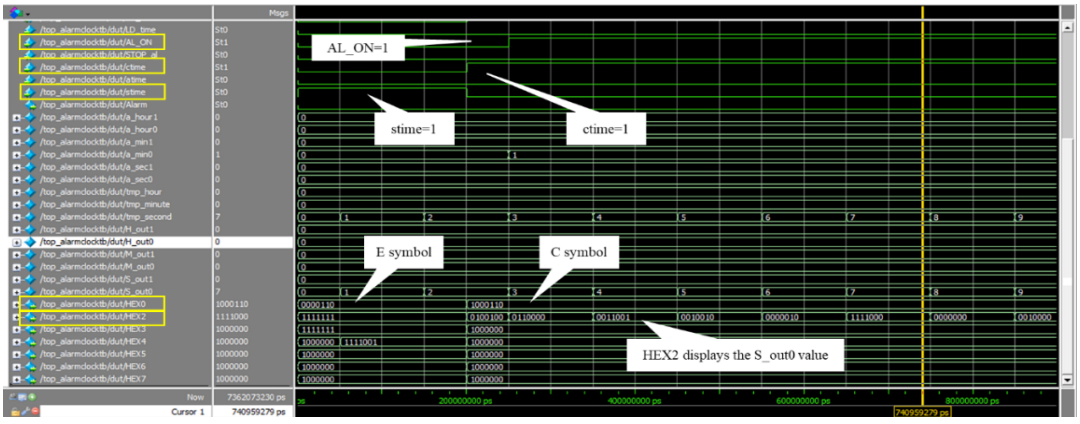

Figure 5. Timing diagram of display mode change

3.2. Hardware implementation

In this project, the digital clock with alarm system accepts input from 12 switches, a 50 MHz clock, and one push button. While the output is 7 unit of seven-segment display and a red LED. Figures 6, 7, and 8 show the implementation of digital clock with alarm system. It shows the types of display modes that can be chosen by user via switches. The input and the output have been assigned through Pin Planner in Quartus Prime 20.1 Lite Edition software. In clock time, HEX0 will display ‘C’ symbol which represents clock. In alarm time, HEX0 will display ‘A’ symbol which represents alarm and HEX0 will display ‘E’ symbol which represents entry or in input time.

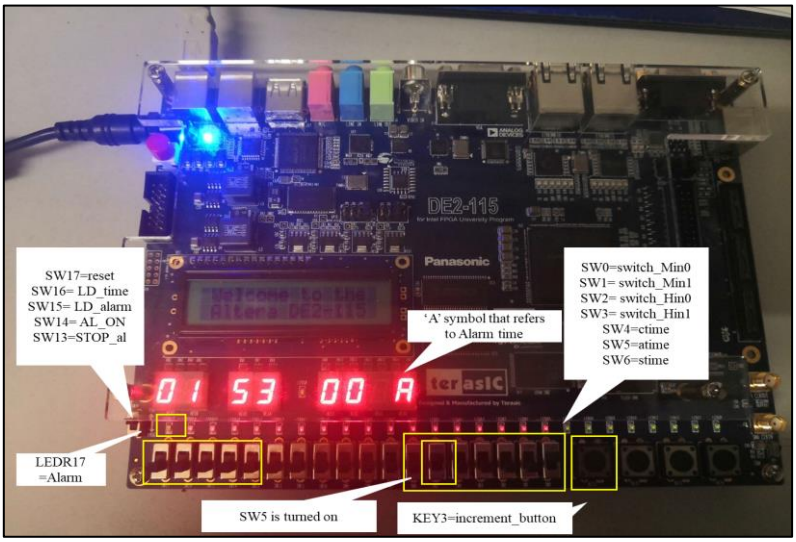

Figure 6. Display mode of alarm time on Altera DE2-115

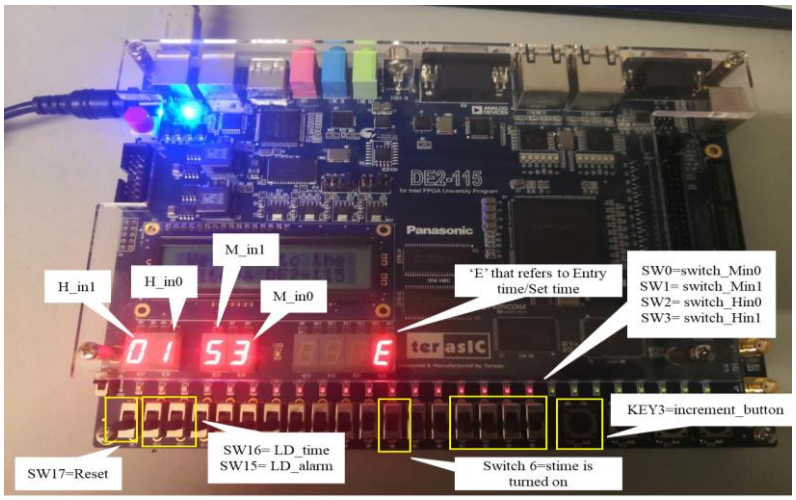

Figure 7. Display mode of input time on Altera DE2-115

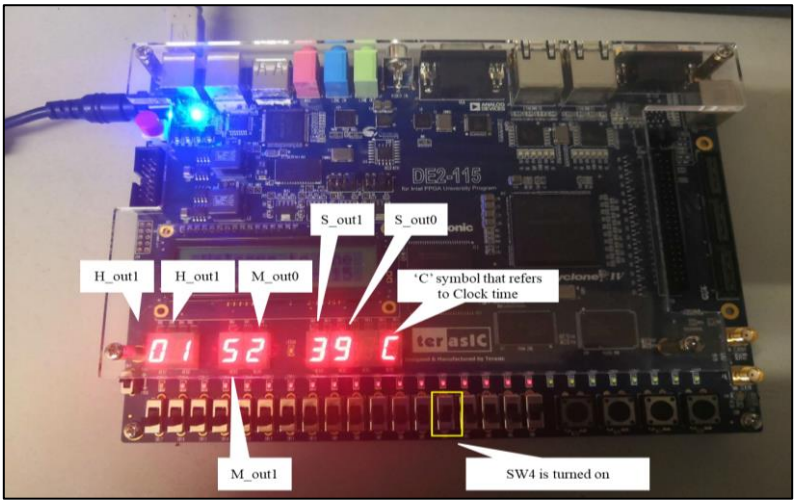

Figure 8. Display mode of clock time on Altera DE2-115

4. CONCLUSION

In conclusion, the digital clock with alarm system has been successfully implemented into Altera DE2-115 board. It consists of switches and button as input while seven-segment display and red LED as output. This digital clock has 3 types of display which is clock, alarm, and input time. Therefore, this study will improve the current technology of digital clock where with usage of microcontroller or microprocessor having disadvantages in term of performance and reprogrammability issues.

REFERENCES

[1] A. Koreki *et al.*, "Are analogue or digital clocks friendlier for people living with dementia?," *Dementia and Geriatric Cognitive Disorders Extra*, vol. 11, no. 3, pp. 207–212, Sep. 2021, doi: 10.1159/000518350.

[2] F. Al-Turjman, H. Zahmatkesh, and L. Mostarda, "Quantifying uncertainty in internet of medical things and big-data services using intelligence and deep learning," *IEEE Access*, vol. 7, pp. 115749–115759, 2019, doi: 10.1109/ACCESS.2019.2931637.

[3] T. T. Ogunseye, G. B. Egbeyale, A. K. Bello, and A. S. Ajani, "Design and construction of a microcontroller based electronic moving message display," *Open Journal of Applied Sciences*, vol. 12, no. 04, pp. 434–454, 2022, doi: 10.4236/ojapps.2022.124030.

[4] A. Malinowski and H. Yu, "Comparison of embedded system design for industrial applications," *IEEE Transactions on Industrial Informatics*, vol. 7, no. 2, pp. 244–254, May 2011, doi: 10.1109/TII.2011.2124466.

[5] A. Zemmouri *et al.*, "Proposal of a reliable embedded circuit to control a stepper motor using microblaze soft-core processor," *International Journal of Reconfigurable and Embedded Systems (IJRES)*, vol. 11, no. 3, pp. 215–225, Nov. 2022, doi: 10.11591/ijres.v11.i3.pp215-225.

[6] Ş. Răzvan and S. Csaba, "Software redundancy implementation strategy in reconfigurable hardware framework," in *Proceedings of 2019 8th International Conference on Modern Power Systems, MPS 2019*, IEEE, May 2019, pp. 1–6, doi: 10.1109/MPS.2019.8759719.

[7] N. Bleier, C. Lee, F. Rodriguez, A. Sou, S. White, and R. Kumar, "FlexiCores: low footprint, high yield, field reprogrammable flexible microprocessors," in *Proceedings - International Symposium on Computer Architecture*, New York, NY, USA: ACM, Jun. 2022, pp. 831–846, doi: 10.1145/3470496.3527410.

[8] C. A. Sepulveda, J. A. Munoz, J. R. Espinoza, M. E. Figueroa, and C. R. Baier, "FPGA v/s DSP performance comparison for a VSC-based STATCOM control application," *IEEE Transactions on Industrial Informatics*, vol. 9, no. 3, pp. 1351–1360, Aug. 2013, doi: 10.1109/TII.2012.2222419.

[9] R. Muley, B. Patil, and R. Henry, "Design and implementation of digital clock with stopwatch on FPGA," in *Proceedings of the 2017 International Conference on Intelligent Computing and Control Systems, ICICCS 2017*, IEEE, Jun. 2017, pp. 1033–1036, doi: 10.1109/ICCONS.2017.8250622.

[10] Z. Z. Aminuddin, I. H. Hamzah, A. A. A. Samat, M. Idris, A. F. A. Rahim, and Z. H. C. Soh, "An FPGA application of home security code using verilog," *International Journal of Reconfigurable and Embedded Systems (IJRES)*, vol. 11, no. 3, pp. 205–214, Nov. 2022, doi: 10.11591/ijres.v11.i3.pp205-214.

[11] I. H. Hamzah, M. S. Z. Suhaimi, A. A. Malik, and A. F. A. Rahim, "Design and implementation of HDL remote controller for smart home system," *Indonesian Journal of Electrical Engineering and Computer Science (IJEECS)*, vol. 20, no. 1, pp. 117–124, Oct. 2020, doi: 10.11591/ijeecs.v20.i1.pp117-124.

[12] J. Yang, H. Y. Li, and L. Liu, "Design and implementation of the infrared remote-controlled digital clock based on FPGA," *Applied Mechanics and Materials*, vol. 738–739, pp. 1266–1269, Mar. 2015, doi: 10.4028/www.scientific.net/amm.738-739.1266.

[13] N. K. Vuthuri, V. Mahewar, G. Yeddluri, E. S. Movva, and V. Ch, "A novel 7-segment digital clock implementation on FPGA," in *Proceedings - International Conference on Trends in Electronics and Informatics, ICEI 2017*, IEEE, May 2017, pp. 465–468, doi: 10.1109/ICOEI.2017.8300970.

[14] S. Ravi, A. M. Zungeru, B. Mtengi, and J. Chuma, "An enhanced digital stopwatch for academic purposes," in *ACM International Conference Proceeding Series*, New York, NY, USA: ACM, Sep. 2019, pp. 92–98, doi: 10.1145/3362752.3362756.

[15] A. Devrari and A. Kumar, "Turbo encoder and decoder chip design and FPGA device analysis for communication system," *International Journal of Reconfigurable and Embedded Systems (IJRES)*, vol. 12, no. 2, pp. 174–185, Jul. 2023, doi: 10.11591/ijres.v12.i2.pp174-185.

[16] I. Chiuchisan, "A new FPGA-based real-time configurable system for medical image processing," in *2013 E-Health and Bioengineering Conference, EHB 2013*, IEEE, Nov. 2013, pp. 1–4, doi: 10.1109/EHB.2013.6707301.

[17] J. H. Zhu, A. Wu, and J. F. Zhu, "Research and design of digital clock based on FPGA," *Advanced Materials Research*, vol. 187, pp. 741–745, Feb. 2011, doi: 10.4028/www.scientific.net/AMR.187.741.

[18] P. Shrestha, B. Subedi, M. Girard, C. Parikh, and N. Kandalaft, "Wireless communication between FPGA and microcontroller," in *2020 10th Annual Computing and Communication Workshop and Conference, CCWC 2020*, IEEE, Jan. 2020, pp. 402–405, doi: 10.1109/CCWC47524.2020.9031196.

[19] J. A. Prathap and S. Ramesh, "A novel reduced instruction set computer-communication processor design using field programmable gate array," *International Journal of Reconfigurable and Embedded Systems (IJRES)*, vol. 12, no. 2, pp. 165–173, Jul. 2023, doi: 10.11591/ijres.v12.i2.pp165-173.

[20] M. F. M. Sabri, M. H. Husin, W. A. W. Z. Abidin, K. M. Tay, and H. M. Basri, "Design of FPGA-based traffic light controller system," in *Proceedings - 2011 IEEE International Conference on Computer Science and Automation Engineering, CSAE 2011*, IEEE, Jun. 2011, pp. 114–118, doi: 10.1109/CSAE.2011.5952814.

[21] J. J. Rodriguez-Andina, M. J. Moure, and M. D. Valdes, "Features, design tools, and application domains of FPGAs," *IEEE Transactions on Industrial Electronics*, vol. 54, no. 4, pp. 1810–1823, Aug. 2007, doi: 10.1109/TIE.2007.898279.

[22] Z. Ge, Y. Peng, Y. Zhang, S. Zhang, and Z. Yang, "Design of intelligent digital clock based on FPGA," in *Proceedings of the 2019 International Conference on Wireless Communication, Network and Multimedia Engineering (WCNME 2019)*, Paris, France: Atlantis Press, 2019, doi: 10.2991/wcnme-19.2019.47.

[23] A. Amara, F. Amiel, T. Ea, "FPGA vs. ASIC for low power applications," *Microelectronics Journal*, vol. 37, no. 8, pp. 669-677, Aug. 2006, doi: 10.1016/j.mejo.2005.11.003..

[24] K. Vipin, S. Shreejith, S. A. Fahmy and A. Easwaran, "Mapping time-critical safety-critical cyber physical systems to hybrid FPGAs," *2014 IEEE International Conference on Cyber-Physical Systems, Networks, and Applications*, Aug. 2014, pp. 31-36, doi:10.1109/CPSNA.2014.14.

[25] G. Dinelli, G. Meoni, E. Rapuano, and L. Fanucci, "Advantages and limitations of fully on-chip CNN FPGA-based hardware accelerator," in *Proceedings-IEEE International Symposium on Circuits and Systems*, IEEE, Oct. 2020, pp. 1–5, doi: 10.1109/iscas45731.2020.9180867.
[26] T. Kahl and S. Dieckerhoff, "Comparison of FPGA- and microcontroller-based control of a high-dynamic power electronic converter," *2017 IEEE 18th Workshop on Control and Modeling for Power Electronics COMPEL*, Jul. 2017, pp. 1-6, doi:10.1109/COMPEL.2017.8013288.

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