International Journal of Reconfigurable and Embedded Systems (IJRES)
Vol. 13, No. 2, July 2024, pp. 307~314
ISSN: 2089-4864, DOI: 10.11591/ijres.v13.i2.pp307-314

Noise coupling reduction using temperature enhanced device for future integrated circuit integration applications

Malagonda Siva Kumar, Jayavelu Mohanraj
Department of Electronics and Communication Engineering, School of Electrical and Communications,
Vel Tech Rangarajan Dr. Sagunthala R&D Institute of Science and Technology, Chennai, India

Article Info

Article history:

Received Apr 12, 2023
Revised Sep 13, 2023
Accepted Sep 21, 2023

Keywords:

Drain induced barrier lowering
Field effect transistor
Nanosheet
Nanosheet field effect transistor
Subthreshold swing

ABSTRACT

Information technology-to-internet of things may have succeeded because of fast silicon chip capability expansion. Moore's law, which reduces device size, boosted integrated circuit (IC) performance. Delay rises with high-density connection parasitic capacitance. Interconnect delays have surpassed transistor delays and slowed progress. An alternative is required now to reduce connection latency. The third dimension is used in popular 3D IC technology IC technology requires through silicon via (TSV) for signal integrity and heat mitigation. Noise coupling hinders electrical communication between signal-carrying TSVs (aggressive TSVs) and ground TSVs (victim TSVs), a 3D IC bottleneck. TSVs must be dielectrically insulated from Si substrates to avoid electrical signal interference. Additionally, first-order modelling will confirm the suggestions. This article proposes using the nanosheet field effect transistor (NSFET) to overcome 3D IC noise coupling and complementary metal oxide semiconductor (CMOS) technology nodes. After discussing the electronic industry and sub nm, several basic metrics and criteria for developing electronic components are presented. The first technique uses Perylene-N's exceptional noise-cancelling characteristics. Second technique uses electrical TSV (ETSV), thermal TSV (TTSV), and heat source models to measure noise coupling on numerous ICs. The third proposes many noise-reducing materials. The suggested structures outperform traditional approaches.

Corresponding Author:

Malagonda Siva Kumar
Department of Electronics and Communication Engineering, School of Electrical and Communications
Vel Tech Rangarajan Dr. Sagunthala R&D Institute of Science and Technology
Avadi, Chennai-600061, Tamil Nadu, India
E-mail: sivakumar.jntuacep@gmail.com

1. INTRODUCTION

Emerging technology known as three-dimensional integrated circuits (3D IC) has the potential to solve the problems associated with two-dimensional (2D) IC integration. Vertical bonding [1]–[6] and through silicon vias (TSVs) can be used to electrically link several thin IC chips to create 3D IC integration. Several semiconductor companies currently rely heavily on TSVs for 3D IC integration. There are two primary types of TSVs: those that transmit an electric signal (ETSV) and those that transmit heat (TTSV). Despite its numerous advantages, noise coupling is a major consideration for the critical design circuits of a 3D IC. Most disruptions to TSVs' electrical signals are caused by noise coupling between TSVs conveying the signals. The use of guard rings around the TSVs and in the TSVs themselves has been shown to reduce noise coupling by a small amount, according to a few studies [7]–[9]. Although the guard ring construction is rather excellent, more structure is needed to enhance noise coupling. Additionally, in order to enhance the

noise coupling, several researchers have used layered liner structures and various liner materials [10], [11]. Through ETSV, we have introduced Perylene-N as a more advantageous dielectric material in our current study.In this design, noise coupling between TSV-to-substrate and TSV-to-TSV is of great importance. Similar to the coupling between interconnections, the volume and direction of the signals propagating in both the victim and the aggressive TSVs rely on the coupling between TSVs. The same problem is focused on for both capacitive and inductive coupling inside TSV arrays. The primary objectives involve a variety of manufacturing and design aspects to reduce the noise linked from aggressive TSV to victim TSV. This research proposes numerous methods for enhancing noise isolation in 3D IC circuits [12]–[15].

2. NOISE COUPLING MODELS IN 3D IC

Global interconnects have developed into a significant roadblock in modern very large scale integration (VLSI) designs. The signal quality worsens as a result of the lengthy interconnects and parasitic impedances. Repeaters, an essential circuit, are needed to mitigate the issue the global connection is having. The 3D structure will provide the best solution for this challenge of global interconnect by enabling intimate vertical integration. TSVs are short vertical links that connect components on neighboring layers in 3D IC designs. These TSVs help fix issues with global connectivity by allowing devices to be tightly connected in the vertical dimension. The main benefit of using 3D ICs is their lower form factor as compared to 2D architectures. A 2D IC of size A has a form factor proportional to A, but an n-layer 3D IC of the same area A has a form factor proportional to A/n. This capability lets tiny products use 3D IC designs. This research examines a unique nanosheet tunnel field effect transistor (TFET) with varying doping concentrations for low power and high switching applications. We use the same method to minimize 3D IC integration noise coupling. The method was previously used to a single 3D IC Si substrate block. In ongoing research, dielectric materials are being developed as an outer layer of TSVs for a single IC block that requires four. The implications of adding dielectric materials to each TSV's model to minimize noise coupling are investigated. Figures 1 and 2 show a single IC structure [16]–[20].

The width of a 3D IC is determined by the distance between the aggressive TSV and the victim TSV. According to the international technology roadmap for semiconductors (ITRS), the expected range for pitch between two TSVs (the shortest distance between the centers of both surrounding TSVs) is 2–8 meters. According to Table 1, a TSV has a thickness of 0.15 um, a height of 8 um, and an area of 4 um.

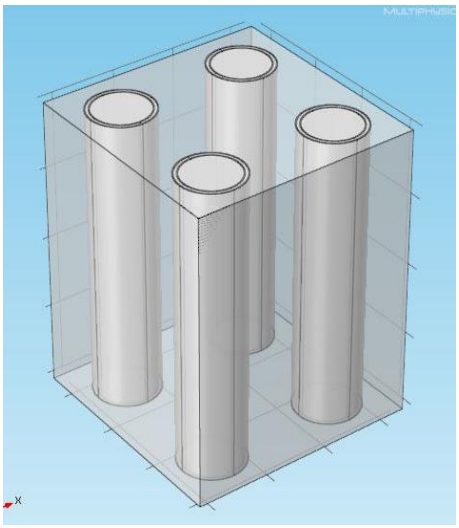

Figure 1. Model of single block of 3D IC structure

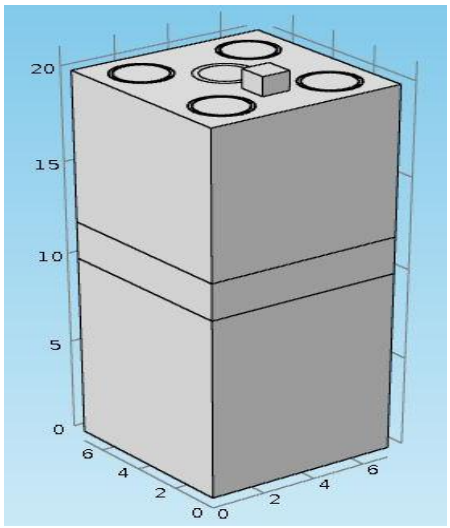

Figure 2. Model of multiple blocks of 3D IC structure

Table 1. Dimensions of TSV as per ITRS roadmap

Dimensions of TSV	Value
TSV's diameter	2 um
Thickness of liner	0.15 um
TSV's height	8 um
Distance between two TSV's	4 um
Pitch between TSV to TSV	2 um

3. METHOD

The Due to the stacking of nano-sheets, the structure of the nanosheet field effect transistor (NSFET) is much more complicated than that of the metal oxide semiconductor field effect transistor (MOSFET). A superlattice with alternating Si and SiGe layers must be constructed as an alternative to a single channel. The next step is to remove the SiGe layer deliberately. Metal gate and gate dielectric (often a combination of SiO_2, Si_3N_4, and a high-K dielectric like Hafnium Oxide (HfO_2)) are used to fully surround the NS, filling the void between the Si channels. It is far more difficult to provide designers a selection of threshold voltages (multi-Vt) for nanosheet (NS) devices than it is for FinFET or MOSFET device designs. Low Vt devices are often utilized due to their outstanding performance, whereas high Vt devices are preferred due to their low power consumption. In order to meet designer goals for the optimal speed-to-power ratio, industrial procedures may produce up to four separate kinds of Vt. For instance, Samsung [20] reports that with 10 nm technology, the same FinFET device was released in super low Vt (sLVT), low Vt (LVT), regular Vt (RVT), and high Vt (HVT) versions, with Vt fluctuating between the two by 200 mV due to differences in the thickness of metal layers in the gate stack. In Narendar and Mishra [21], the metal gate boundary control strategy for multi-Vt NSFET devices is discussed. In our simulated NSFET, we used NS with thicknesses between 7 nm and 20 nm. In Figure 3, a 3D schematic of the proposed nanosheet tunnel FET is shown. Figure 3, which depicts a cross-sectional view of a NSFET, was produced using technology computer-aided design (TCAD).

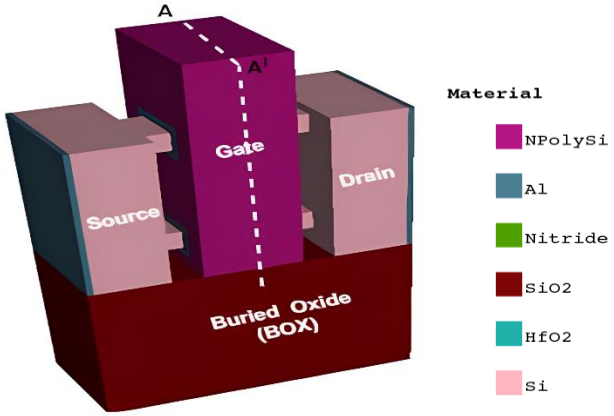

Figure 3. 3D schematic view of the proposed NSFET

4. RESULTS AND DISCUSSION

A novel dielectric material with a low dielectric constant (Perylene-N) be utilized for noise isolation in future IC integration. Due to poor electrical signaling between the signal carrier and the victim, TSVs have the greatest drawback. Growing noise coupling occurs between silicon substrates and TSVs Perylene-N, a dielectric material, is used as a consequence to minimize noise while using less energy and taking up less space. For several structures, such as single-liner and stacked-liner constructions, as well as THz analyses, the Perylene-N material is contrasted with traditional SiO_2 material shown in Figure 4.

Perylene-N and SiO_2 are employed as single liner and stacked layers of liner structures surrounding the TSV shown in Figure 5. Many excellent mechanism designs were developed at around the same time that the traditional MOS structure met its scaling limit. Device performance is diminished as a consequence of short channel effects and drain induced barrier lowering (DIBL) introduced during MOSFET scaling. Until recently, it has been inconceivable to factor channels thinner than 6 nm into the 3D quantum transport equations. The density gradient model is commonly used in quantum transport equations [22]. A NSFET device is distinguished by its band gap narrowing (BGN) model and its doping-dependent mobility. The Shockley-read-hall (SRH) gene and the idea of Auger recombination have both been the subject of much study. Using CVT and ballistic mobility models, we were able to simulate gate lengths below 10 nm.

We undertake 3D simulations with a set/reset voltage range of +/-10 V to ascertain whether the reliability and performance of our proposed NSFET designs are feasible. The experimental setup results shown in Figure 6 are used to perform an initial calibration of the proposed NS device. The calibration verifies that the calculated drain current (ID) agrees with the experimental data.

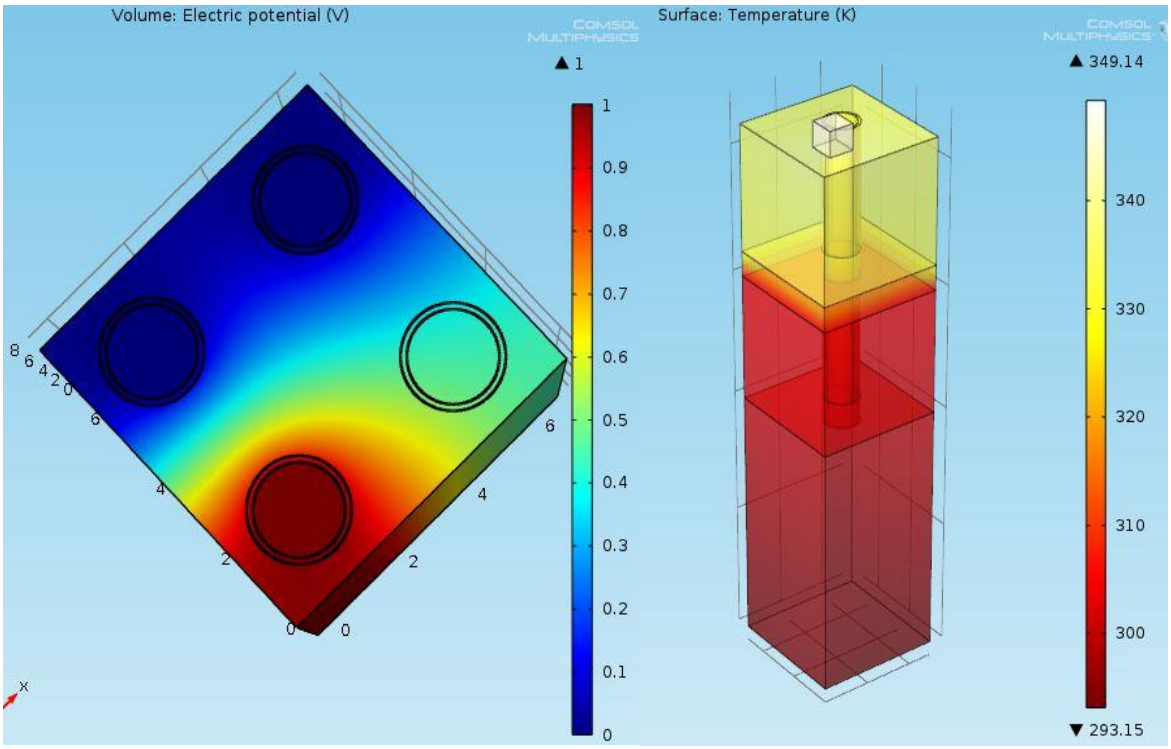

Figure 4. Electrical and thermal models are in 3D view

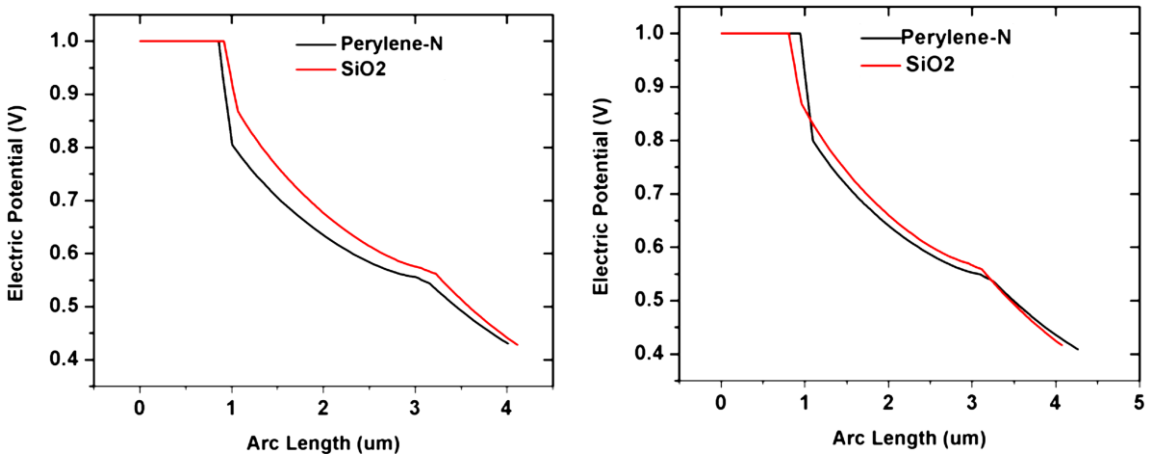

Figure 5. Differences in applied potential between TSVs made of dielectric materials

Figure 6 demonstrates that the physical properties of the TCAD device correlate well with the experimental data used to illustrate NSFETs. It provides abundant evidence that the proposed model is quite similar to the observed one. The gate voltage (VGS) was adjusted from 0 V to 1.6 V to comply with ITRS standards. The framework for the gadget was created using a simulator built on the TCAD platform. The NSFET has dimensions of 12 nm for its gate length (LG), fin width (FW), channel height (H), and buried oxide layer (OL). Two times 12 nm is 24 nm, and that's how tall the whole fin is. To avoid nanoscale junction formation, the device is maintained at a constant doping concentration of 2×1018 /cm^3. We also look at operating the proposed NSFET at temperatures between 225 and 375 °C. The DIBL and subthreshold swing (SS) are used to measure how well a device performs in the subthreshold range. The DIBL and SS are calculated using the given formulas [23]. The simulated device's SS and DIBL are calculated based on the following factors. The temperature dependence of the SS is seen in Figure 7. High-temperature simulations of the SS were performed.

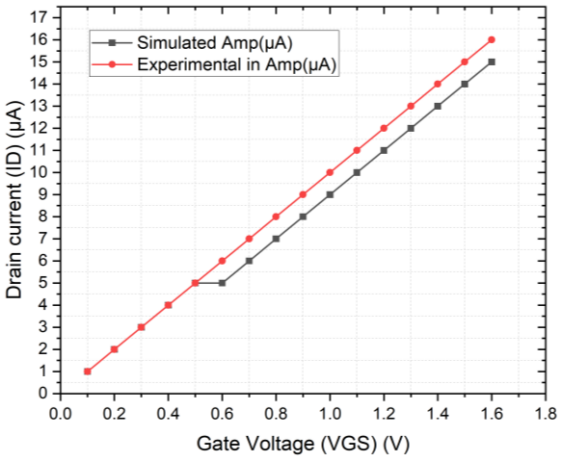

Figure 6. Calibration of TCAD device with experimental data utilized to demonstrate NSFET

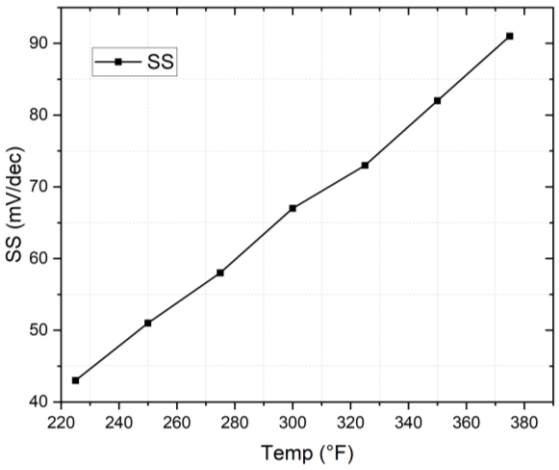

Figure 7. Subthreshold NSFET characteristics with temperature variation

It is obvious that when the temperature rises, the subthreshold swing (mV/dec) increases. Figure 7 shows the proposed NsFET's drain-induced barrier lowering at various temperatures. The suggested structure offers excellent control over the DIBL as temperature increases, as is extremely obvious from the DIBL plot. Finally, when the temperature rises more, there is not much of an increase in the DIBL curve. It implies that the suggested gadget performs better even at greater temperatures.

The performance of the gadget was further investigated by analyzing I_{ON} and I_{OFF} at various temperatures. The suggested NSFET's I_{ON} is shown in Figure 8, at a higher temperature. The suggested device's on current is in the microampere region, which blatantly indicates the simulated device has greater switching control. Figure 9, illustrates how I_{ON} grows as the temperature rises and then decreases as the temperature rises. Figure 9, depicts the I_{OFF} of the simulated device at temperatures ranging from 225 °C to 375 °C. The suggested device's off current is in the region of Pico Amperes, demonstrating the device's excellent performance even at higher temperatures.

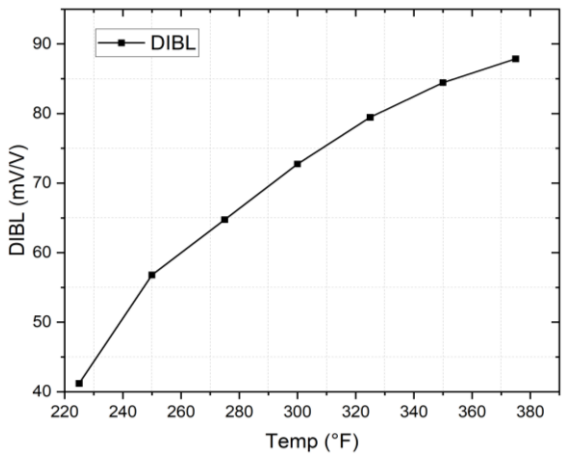

Figure 8. DIBL plot of proposed NSFET with varying temperature

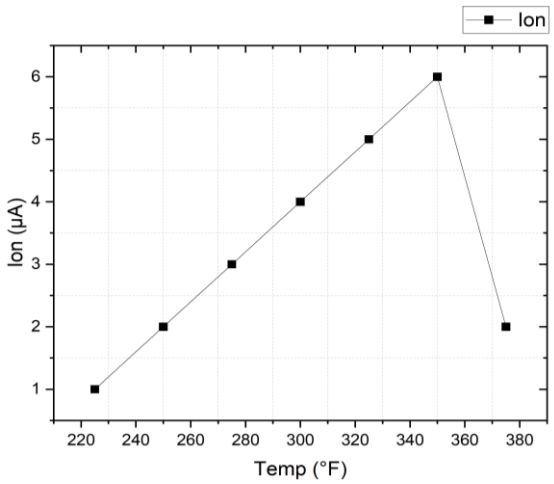

Figure 9. I_{ON} of the proposed NSFET at varying temperature

Figure 10 shows the proposed NSFET's I_{ON}/I_{OFF} calculated and shown. We found that the device runs between 225 °C and 375 °C and has an I_{ON}/I_{OFF} ratio of above 107. The gm is crucial while designing operational and transconductance amplifiers. The gm shows the amplifier's DC gain, bandwidth, and noise efficiency. The formula from [24]–[26] was used to calculate and simulate the NSFET's transconductance.

Change the drain voltage (VDS) from 0.1 V to 1.6 V to imitate the device's transconductance. Figure 9 shows that drain voltage increases transconductance for the recommended NSFET.

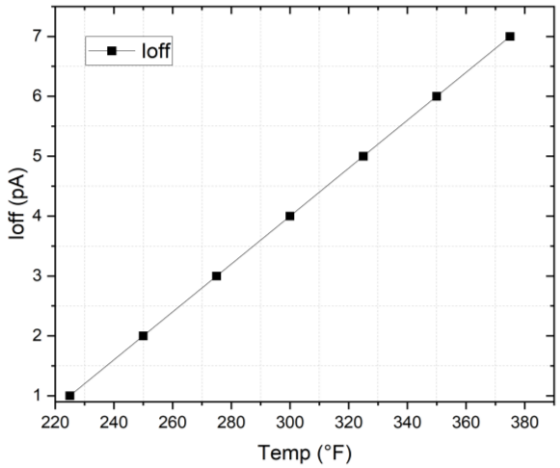

Figure 10. I_{OFF} of the proposed NSFET at varying temperature

In order to determine a device's intrinsic gain, the output conductance (gd) is a crucial figure of merit. With a minor change in drain current and a small change in drain to source voltage, output conductance was estimated shown in the Figure 11. The output conductance curve was generated using a range of drain to source voltages, from 0.1 V to 1.6 V, as illustrated in Figure 12. A little rise in output conductance with rising VDS strongly confirms the suggested NSFET's driving potential. The outcomes are ideal for both high switching-rate and low power applications.

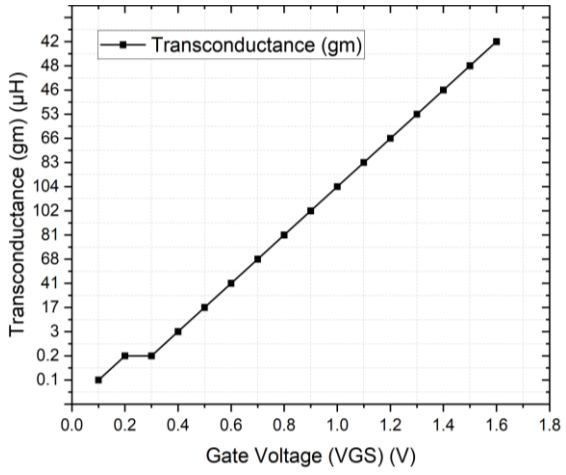

Figure 11. Transconductance (gm) plot with varying drain to source voltage of the proposed NSFET

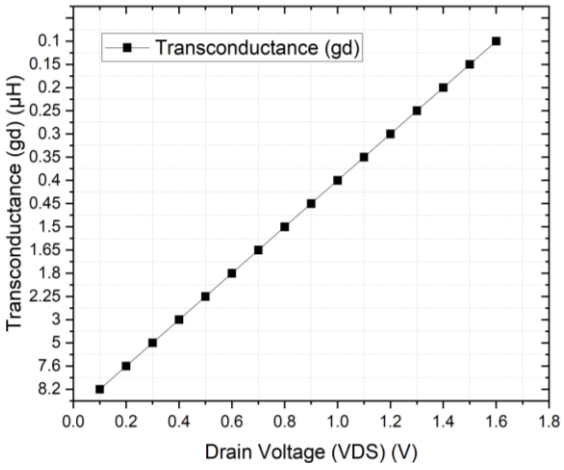

Figure 12. Output conductance (gd) plot with varying drain to source voltage of the proposed NSFET

5. CONCLUSION

New integration strategies have been developed to decrease network delay. One of the greatest methods for CMOS applications is 3D integration technology, which enables many layers of devices to be stacked with high-thickness, interconnects between them. A big benefit of 3D IC is its capacity to perform heterogeneous integration in addition to everything else. The problem of noise coupling in 3D IC is quite serious. In order to lessen the issues with noise coupling, several researchers have created and tested

alternative materials for TSVs and substrates. This work proposes the application of the novel NSFET for the changeable CMOS technology node and the 3D IC noise coupling problem. Design requirements and basics are covered after a brief introduction of the electronic market and the route to the sub-nm world. Three approaches are suggested: the first uses Perylene-N as a dielectric material to reduce noise when compared to other dielectric materials; the second employs three distinct models to test noise coupling on numerous ICs, such as ETSV, TTSV, and heat source; and the third employs various core materials to isolate noise. The suggested structures provide superior results to traditional methods.

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BIOGRAPHIES OF AUTHORS

Malagonda Siva Kumar received his B.Tech. degree in the branch of electronics and communication engineering from JNTU Anantapuram, Andhra Pradesh, India in 2007. He Completed M.Tech. from JNTU Anantapuram, Andhrapradesh, India in 2011. He is pursuing Ph.D. in Department of Electronics and Communication Engineering, Vel Tech Rangarajan Dr. Sagunthala R&D Institute of Science and Technology, Avadi, Chennai-600061, India. He can be contacted at email: sivakumar.jntuacep@gmail.com.

Dr. Jayavelu Mohanraj received the B.Tech. degree in telecommunication engineering from the Vellore Institute of Technology (VIT), Vellore, India, in 2008, the master's degree in VLSI design from Vel Tech Technical University, Avadi, Chennai, in 2012, and the Ph.D. degree from VIT in 2018. He is currently an associate professor with the Department of Electronics and Communication Engineering, Vel Tech Rangarajan Dr. Sagunthala Research and Development Institute of Science and Technology, Chennai. He has authored or coauthored over 20 papers in different international journals and conferences. His fields of interest include ultrafast fiber laser, nanomaterial-based saturable absorbers, and sensors. He can be contacted at email: jmohanraj@veltech.edu.in.