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An efficient high performance reconfigurable canonical sign digit architecture for software defined radio

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ABSTRACT

Software defined radios (SDRs) are highly motivated for wireless device modelling due to their flexibility and scalability over alternative wireless design options. The evolutionary structure of finite impulse response (FIR) filters was designed for a proposed reconfigurable canonical sign digit (CSD) approach. Considering the complex trade-off, this is accomplished with many FIR taps, which is a challenging assignment. On the baseband processing side, design is given with parameterization-controlled FIR filter tap selection. Optimal processing models to overcome the reconfigurable design issues associated with the SDR system for a multi-standard wireless communication system root cosine filter standard are often used to implement multiple FIR channelization topologies, each of which is tied to a particular in-phase and quadrature (IQ) symbol. Additionally, it demonstrates the viability of using a multi-modulation baseband modulator in the SDR system for next-generation wireless communication systems to maximise adaptability with the least amount of computational complexity overhead. The proposed multiplier-less FIR filter-based reconfigurable baseband modulator, according to the experimental results, offers a 6% complexity reduction and a 47% improvement in performance efficiency over the current SDR system.

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1. INTRODUCTION

Wireless communication has become increasingly popular, but existing devices are not enough to meet the needs of users. Furthermore, it is impossible and cost inefficient to use new devices models for each wireless standard introduces [1]. Software defined radio (SDR), is a method of wireless communication. This technique relies on wireless protocols specified in software rather than hardware. This means that the underlying hardware may be used indefinitely while new features and functions are added or updated through reprogramming. This allows for the realisation of wireless devices that can operate on many frequencies simultaneously. SDR should have a reasonably low cost in terms of its hardware and a relatively low rate of energy consumption if its application ranges are to be expanded [2]. When it comes to the implementation of SDR in hardware platforms, digital signal processors (DSPs) and field-programmable gate arrays (FPGAs) are two main ways that are often employed. The DSP-based architecture provides more flexibility while simultaneously improving both energy and area efficiency. Nevertheless, the DSP model is unable to fulfil the throughput rate requirements demanded by the growing wireless communication system. In addition, the inability to reconfigure further hinders its

performance. On the other hand, modelling that is based on FPGAs enables dynamic reconfiguration, which may accommodate a broad variety of standards and maintains all of the potential metrics of techniques that are based on DSPs. In addition, recent advances in FPGA technology enable the development of a high-performance SDR system [3]. The graphics processing unit (GPU) is sometimes used too, thanks to its parallel processing capabilities. Because of its versatility and adaptability, SDR is used for multi-standard wireless applications. The SDR's digital channelizer is its most crucial component. The digital channelizer is responsible for the down conversion of digital signals, the conversion of sampling rates, and the filtering of channels. A group of channel filters makes up the bulk of the SDR's digital channelizer [4].

The newest methods for wireless communication systems raise the quality of service (QoS) while supporting various protocols, including global system for mobile communications (GSM), universal mobile telecommunication system (UMTS), and wideband code division multiple access (WCDMA), among others, with better data rates. It also encompasses numerous wireless data transport methods and digital broadcasting models, such as digital audio and digital video broadcasting (DVB) (wireless local area network (WLAN), WiFi). However, its range of applications was constrained by flexibility concerns and the existence of analogue components [5]. To address this issue, next-generation wireless communication systems [6], [7] provide a single terminal solution based on highly adaptable digital hardware that can carry out numerous tasks using reconfigurable units.

In this scenario, SDR technology [8] always aims to more flexibly perform many functions over a single terminal device while also supporting various wireless protocols. Flexibility in digital systems is only possible through dynamic reconfiguration of the other digital blocks in accordance with the design specifications. The dynamic reconfiguration for real-time applications should be established in a short amount of time. For the purpose of sending and receiving baseband data at an intermediate frequency, digital SDR [9] computes signal processing using programmable devices. SDR systems can use software-enabled capabilities to replace every piece of hardware in conventional radio systems, including mixers, modulators, demodulators, and any other relevant modules [10]. This will make it possible for a single piece of hardware to support a variety of radio modes, including amplitude modulation amplitude modulation (AM), frequency modulation (FM), single sideband (SSB), and double sideband (DSB) [11]. In addition, SDR systems use multiple digital channels to communicate with digital devices such as computers and peripherals. There are several advantages to using the SDR system over other wireless technologies. All current infrastructure, including base stations and different standards, may now be supported by the SDR system component. The following requirements can be met by configuring these programmable devices with DSPs and FPGAs during the hardware implementation of SDR communication protocols [12]. Using DSPs and FPGAs, the SDR system supports channel dependent frequency modulation in software for conventional and multiband systems. For wireless device modeling in communication systems, hardware based methods have become more popular in recent years. An inherent potential metric of a programmable device is used to create the overall system architecture in the SDR system evaluation process. Using a programmable device, such as an FPGA, for a system implementation is often expensive and thus not preferable. For the SDR system, the essential functions of a wireless communication system may be accomplished on a single hardware platform by combining various compute units.

2. RELATED WORK

Because of its statistical and physical properties, the SDR finite impulse response (FIR) filter may be used in a broad variety of communication receivers for noise reduction, voice detection, and the elimination of interference caused by adjacent channels. With digital filter banks on the receiver, distinct SDR channels from a broad spectrum may be isolated and utilized separately and simultaneously. Even though high sampling rates are desirable for SDR channels, power consumption, and performance issues must be taken into account to enable portable receivers, and these may result in an FIR filter with a rather limited number of taps. Narrow band subcarriers are derived from a signal's channel bandwidth using a bank of FIR filters so that each subcarrier frequency is directly related to the input signal. FIR filters are extensively employed in several signal processing and communication applications due to their precise linear phase and high stability under specific circumstances. Digital filters with a tunable passband are designed using approximate spectral parameters and transformed [13].

Odugu *et al.* [14] implemented the 2-D FIR filter designs by proposing a memory-based look-up table (LUT) multiplication mechanism. Here, distribute arithmetic (DA) multipliers are used to materialise a filter bank comprised of block-based symmetry FIR filters. Only coefficients that are even numbers or odd numbers are considered to store in LUT in order to minimise LUT size. To maximise the very large scale integration (VLSI) design metrics of FIR filter banks, we combine the concepts of symmetry in the coefficients, parallel processing, and DA. 1-D filters have access to the same capabilities. Horvath and Bakki [15] developed SDR based orthogonal frequency-division multiplexing (OFDM) to realize the potential metrics of SDR, such as reconfigurability and

flexibility. Here multi modulation selection of baseband unit allows aware channel mapping for improved QoS. The sensitiveness of higher-order quadrature amplitude modulation (QAM) in smaller SNR regions is very high compared to M-ary phase-shift keying (MPSK) to minimize error rate performance. The problems related to peak-to-average power ratio (PAPR) are also reduced using appropriate channel coding and clipping models. Furthermore, finally a configurable digital filter is incorporated to reducing the distortion caused by the clipping method.

Suzuki *et al.* [16] proposes a combinational driven bit shift canonical sign digit (CSD) to implement CSD in FIR filter design. Compact representation utilising CSD of produced FIR coefficients considerably reduces the overall number of registers used. To convert the 2's complement number to CSD, they introduced a unique real-time transformation mechanism in [17]. Additionally, the performance characteristics of the architecture employing radix eight multipliers are evaluated. The findings showed that multiplier-based design is much superior, whereas CSD has a smaller complexity overhead and gives greater energy efficiency. Thomas and Indu [18] proposes a digital upconverter (DUC) with a highly programmable pulse shaping filter was created to support several industry standards. This optimization is done in two ways: first, the number of processes needed per input sample is lowered. Then, the number of adder components is reduced by using bitwise binary common sub expressions (BCS) based elimination. A multiplier-adder circuit (MAC) was constructed by employing decomposed LUTs in all stages of the netlist in [19] to get the optimal result. Lowering connection length may further improve route propagation by reducing the total activity of signal transitions associated with each filter tap. Reconfigurable mode was suggested in [20] using a hardware-based look-up table (HLUT). The number of adders and memory elements utilised in the FIR structure may be reduced significantly due to hardware sharing across the many internal blocks.

The memoryless distributed arithmetic proposed in [21] for hardware efficient decision feedback equalizer (DFE) implementation. This memoryless DA model mitigates the problems of higher order filters in DFE architectures, like increased hardware complexity and latency. With an enhanced 4:2 compressor adder, the hardware utilization rate is maximized during the accumulation process new in-situ strategies for reducing timing errors were devised in [22] to address the effects of dynamic changes in the DA. An extension block for the sign and precision gate size are the two main components. The least significant bit (LSB) calculation has an impact on the route latency. With some moderate timing faults and acceptable accuracy losses, this is a good example.

3. SOFTWARE DEFINED RADIO

It is important for solutions to be able to give prospective needs for these models in the design of any SDR system for wireless applications. Channel coding [23], data modulation [24], channel estimation [25], and symbol equalisation [26], are all part of this digital base band processing. Most radio system operations were originally realised using analogue circuitry until digital signal processing technology was introduced. Research has shifted to focus on using SDR as highly flexible digital communication in light of recent improvements in the digital system. In particular, Figure 1 SDR design is used when designing wireless devices for mobile communication due to its ability to work under tighter energy parameters and smaller footprint requirements. Communication systems that use SDR technology must be backwards-compatible with older protocols and forward-compatible with new protocols via reconfigurable methods.

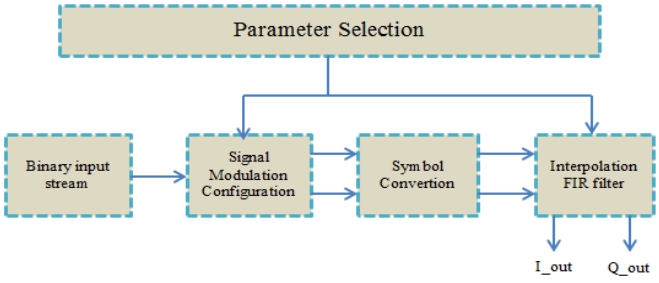


Figure 1. SDR configurable architecture

4. SDR FIR FILTER DESIGN

Wireless systems are particularly vulnerable to interference deterioration, necessitating the use of digital filtering to counteract this. Inter-symbol interference may be solved by using an root raised cosine (RRC) pulse shaping filter [27] in the intermediate frequency (IF) stage of most wireless communication systems. Each modulated signal's spectral breadth is restricted by the RRC filter. There are various benefits of

using filters in wireless communication: i) to prevent inter-symbol interference (ISI) by adjusting the pulse spectra of each sent message; ii) a low pass frequency dispersive channel may be used to enhance data transmission reliability; and iii) in order to reduce the bandwidth requirements and reduce co-channel interference (CCI).

Digital FIR structures for the implementation of the RRC filter use computationally complicated arithmetic units with energy-inefficient data propagation. In order to make the RRC compatible with wireless standards, it is necessary to simplify the FIR filter design on the hardware side. When integrated into the SDR system, the prototype RRC filter should fulfill the system's power and compactness requirements. RRC filter design complexity may be reduced by using a novel technique that uses a circuit structure shown Figure 2 (a digital FIR structure) to alleviate this issue.

4.1. RRC FIR interpolation filter

Interpolation factors, roll-off value, and order are all elements that affect the frequency response of the RRC FIR interpolation filter when FIR coefficients are extracted. In order to accommodate a broad variety of typical digital implementations of FIR filters, a bank of FIR coefficients with greater flexibility and high performance is required, design specification of filter for various wireless standards WCDMA, UMTS, and DVB, as shown in Table 1. The design of reconfigurable FIR filters for SDR systems has been the subject of many studies [28].

Hardware optimization for SDR applications necessitates the articulation of the FIR structure. Figure 2 depicts a simple real-time wireless filter. The majority of SDR systems suggested for wireless applications should be able to handle a wide range of different standards at high speeds. A changeable RRC filter design with proper arithmetic models may do this. Because of the number of taps and related filter coefficients that are created from the impulse response, RRC's spectral properties are already pre-determined.

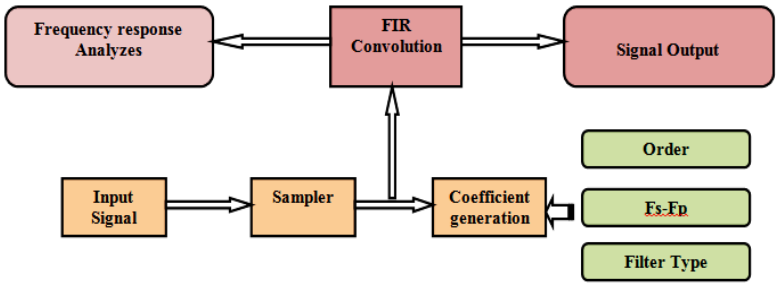


Figure 2. FIR architecture

Table 1. Design specification of filter for various wireless standards

Roll off factor is 0.22	WCDMA	UMTS	DVB
Sampling frequency	5 MHz	30.72 MHz	165 MHz
FIR order	25	49	37

4.2. Pulse shaping filter

Based on how the pulse is shaped, the symbol is calculated, the samples are shown, and a narrow band pulse is made for transmission. The biggest problem with any digital modulation method is interference, which slows down the whole system and makes it harder for the receiver to find the symbol. A SDR part of a communication system used an RRC pulse shaping filter at the IF stage to change the shape of the spectrum. This eliminated the broader modulated signal caused by intersymbol interference. The (1) illustrates the connection between the root raised cosine impulse response and the roll-off factor.

$$h(\mathrm{t}) = \frac{4\alpha T/\pi}{T^2-16\alpha^2t^2}\cos\left[\pi T\frac{(1+\alpha)}{T}\right] + \frac{T^2/\pi T}{T^2-16\alpha^2t^2}\cos\left[\pi T\frac{(1-\alpha)}{T}\right] \quad (1)$$

Where α denotes a roll-off factor, with the dynamic range of $0<\alpha\leq 1$, and T denotes the symbol duration.

The filter bandwidth (BW) is directly proportional to the roll-off factor (α) as shown in (2).

$$\mathrm{BW}=\frac{(1+\alpha)}{\mathrm{T}} \quad (2)$$

Raised root cosine filters with different roll-off factors are most commonly used for communication standards. The wireless communication system used roll-off factors between 0.1 to 0.5 based on bandwidth restrictions and a modest distortion rate. Here we consider a roll-off factor value of 0.33 for generating pulse shaped in-phase and quadrature (IQ) baseband modulated symbols. Typical digital implementations of the RRC FIR filter require N number of multiply and accumulate units, leading to computational complexity. Irrespective of the applications and various types of architecture used for RRC filter implementation, reconfigurability, and hardware optimization are essential and need to be established for SDR applications. The Table 2 shows the RRC filter design specifications.

Table 2. RRC filter design specification

Design parameter	Value
Response type	Raised-cosine
Filter type	Direct from-FIR filter
Magnitude specification	Square-root
Windowing technique	Rectangular window
FIR order	4, 8, 16 taps
Stop band frequency (Fs)	15.3 MHz
Carrier frequency (Fc)	1.6 MHz
Roll-off factor (α)	0.22

4.3. Root raised cosine filter

The raised cosine pulse takes on the shape of a sine pulse, which can be implemented completely in the digital domain to reduce bandwidth consumption and inter block interferences, which is accomplished through a root raised cosine filter. Table 3 shows the raised root cosine filter design specification. The Fourier transform of the root raised cosine pulse generates a square frequency spectrum, which provides a brick wall like spectrum to communication channels. In the present work, various taps of the RRC FIR filter with appropriate roll off factors are designed in the MATLAB filter design analyzer (FDA) tool as illustrated in Figure 3 and FIR coefficients are extracted from each set of system components. The implementation of the RRC filter is carried out using a CSD based approach, where the multiplication is achieved by controlled bit shifting. By default, the FDA tool generates the coefficients in fractional numbers for the given specifications and chosen impulse response as shown in Figure 3.

Table 3. CSD recoding unit

Binary	CSD
000	0000
001	0001
010	0010
011	0010-1
100	0100
101	0101
110	10-10
111	100-1

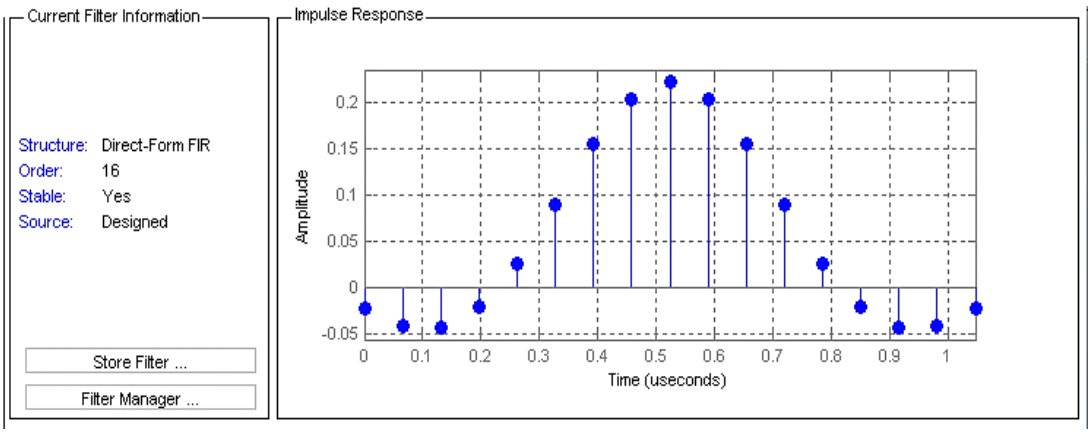
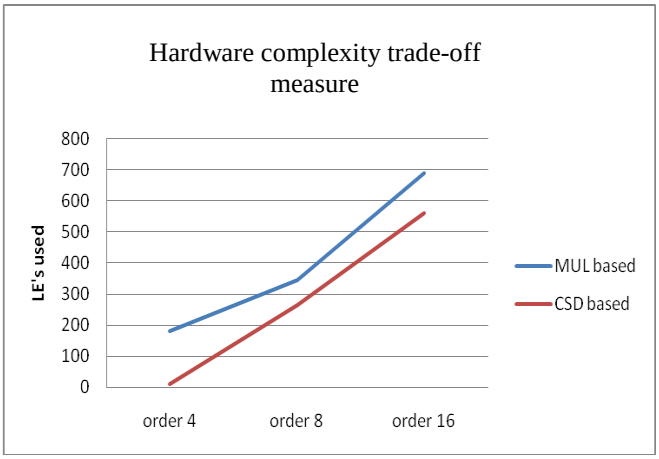


Figure 3. RRC impulse response visualization

5. CSD MODEL

5.1. CSD FIR filter performance evaluations

The suggested FIR is evaluated using a broad variety of FIR orders to prove the trade-off measure in the CSD performance validation centre FIR filter design, as shown in Table 3. Figure 4 shown all multiplier components were replaced by the proposed FIR MAC with a CSD orientation Figure 4(a) and Figure 4(b) illustrate its better performance in reducing complexity overhead and route latency.



(a)

(b)

Figure 4. Performance comparison of CSD FIR unit (a) hardware complexity analysis and (b) performance path delay analysis

As demonstrated in (3), a filter's CSD coefficients are represented by a small number of signed digits:

$$CSD = \sum_{i=0}^{M} d_i 2^{-p_i} \quad (3)$$

where pi ϵ {0, 1, …, N} and di denotes the signed digit {-1, 0, 1}. CSD based FIR MAC includes the advantages of both parallel processing as well as path delay reduction during FIR tap computations and outperforms conventional multiplier based approaches, as shown in Table 4.

Table 4. Performance trade off comparison analyses of proposed CSD FIR design

Length of FIR	MAC computation with conventional FIR		DA computation with proposed FIR	
	LE's (Area)	Max (f)	LE's (Area)	Max (f)
4 tap	182	130.72 MHz	111	162.13 MHz
8 tap	346	100.22 MHz	265	84.1 MHz
16 tap	688	68.5 MHz	559	52.1 MHz

6. CONCLUSION

FIR filters designs that function well. An increase in the number of taps reveals that the intended CSD driven FIR data rate may be increased. In order to achieve maximum device efficiency, or LEs, the clock frequency was decreased substantially. It's possible to minimize propagation route delay while still increasing performance thanks to the simplified hardware. FIR filter designs that are optimum and adjustable support the dynamics of the SDR system in addition to the completely digitalized frequency synthesizer model and boost the flexibility of future generation communication systems.

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