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Role of tuning techniques in advancing the performance of negative capacitance field effecting based full adder

Ravuri Daniel[1], Bode Prasad[2], Abhay Chaturvedi[3], Chinthaguntla Balaswamy[4], Dorababu Sudarsa[5], Nallathambi Vinodhkumar[6], Ramakrishna Reddy Eamani[6], Ambarapu Sudhakar[7], Bodapati Venkata Rajanna[7]

[1]Department of Computer Science and Engineering, Prasad V. Potluri Siddhartha Institute of Technology, Vijayawada, India
[2]Department of Information Technology, Vignan's Institute of Information Technology (A), Visakhapatnam, India
[3]Department of Electronics and Communication Engineering, GLA University, Mathura, India
[4]Department of Electronics and Communication Engineering, Seshadri Rao Gudlavalleru Engineering College, Gudlavalleru, India
[5]Department of Computer science and Engineering, Koneru Lakshmaiah Education Foundation, Vijayawada, India
[6]Department of Electronics and Communication Engineering,
Vel Tech Rangarajan Dr. Sagunthala R&D Institute of Science and Technology, Chennai, India
[7]Department of Electrical and Electronics Engineering, MLR Institute of Technology, Hyderabad, India

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ABSTRACT

The increasing demand for faster, robust, and efficient device development of enabling technology to mass production of industrial research in circuit design deals with challenges like size, efficiency, power, and scalability. This paper, presents a design and analysis of low power high speed full adder using negative capacitance field effecting transistors. A comprehensive study is performed with adiabatic logic and reversable logic. The performance of full adder is studied with metal oxide field effect transistor (MOSFET) and negative capacitance field effecting (NCFET). The NCFET based full adder offers a low power and high speed compared with conventional MOSFET. The complete design and analysis are performed using cadence virtuoso. The adiabatic logic offering low delay of 0.023 ns and reversable logic is offering low power of 7.19 mw.

Corresponding Author:

Ravuri Daniel
Department of Computer Science and Engineering, Prasad V. Potluri Siddhartha Institute of Technology
Chalasani Nagar, Kanuru, Vijayawada, Andhra Pradesh 520007, India
Email: danielravuri@gmail.com

1. INTRODUCTION

The modern embedded systems and signal processing processors demand low power and high speed full adder [1]. Many researchers have developed versions of complete adders using XOR/XNOR gates and complementary metal-oxide semiconductor (CMOS) inverters [2]. The transistor technology and logic utilised to create the complete adder will decide the performance [3]. Transistor scaling is vital to building low-power integrated circuit (IC). Transistors technologies as high-electron-mobility transistor (HEMT), heterojunction bipolar transistor (HBT), metal oxide semiconductor field effect transistor (MOSFET), and negative capacitance field effect transistor (NCFET) [4], [5] facilitate scaling to lower levels [6]. Other than typical full adder design techniques (using XOR/XNOR (or) CMOS inverters), there are some popular digital logics accessible, i.e., efficient charge recovery logic (ECRL), adiabatic logic, dual rail circuits (DRC), and reversible logic [7], [8]. In this paper, we give an examination of the design of a full adder using several transistor technologies and different forms of logic to boost the ability in the elements of delay and power. When compared with the typical XOR operations of full adder cells, adiabatic logic [9], [10] and reversable logic-

based full adder cells offer outstanding performance. This paper is organized as follows. Section 2 presents the related work. In section 3, problem statement and the proposed method is described. In section 4, design and analysis is presented. In section 5, described results and analysis. Finally, the main conclusion and future directions are parented in section 6.

2. RELATED WORK

Consumer electronics and medical devices use ultra-low-power circuitry. Low-power technology powers CMOS scaling. Digital signal processing uses complex techniques like convolution, which requires efficient arithmetic circuits. As arithmetic circuits become more complicated, power consumption becomes more critical. This complicates arithmetic circuits, making energy usage more important. Cell phones, PDAs, and laptops are in high demand because arithmetic circuits use a low-power full adder [11]. Table 1 show that the ECRL, DRC, secured quasi-adiabatic logic (SQAL), and one-dimensional capacitor (ODC) have been proposed and studied to understand future energy-efficient high-end computing systems.

Table 1. Full adder design state of art

Ref.	Transistor technology	Logic	Number of transistors		Description
			P-Type	N-Type	
[12]	MOSFET	Hybrid CMOS	10	10	This research suggests triplet design to improve transmission gate (TG) and hybrid CMOS full adder designs in chain and tree topologies. TG and hybrid CMOS full adder can employ this approach.
[13]	Quantum-dot cellular automata (QCA)	--	--	--	Digital logic and arithmetic use the full adder circuit. This study examines QCA-enhanced full adder. This full adder features fewer cells and a shorter latency.
[14]	MOSFET	Gate diffusion input (GDI)	8	8	Addition is the foundation of arithmetic. This work builds three low-power full adders with full-swing AND, OR, and XOR gates to overcome GDI logic's threshold voltage problem.
[15]	MOSFET	MOS current-mode logic	7	7	This work presents a reversible logic full adder for MOS current mode logic (MCML) circuits. Six-input logic gates power the conventional MCML full adder.
[16]	HEMT	Reversible logic-	12	12	Reversible circuits cannot fan-out, but extra gates can. Feynman, TSG, and Peres gates are explained here.
[17]	MOSFET-	XOR-MUX-	--	--	Digital technology, especially signal processing, has advanced significantly. Software-defined radio devices must be compact, low power, high-performing, and fast.
[18]	MOSFET	Adiabatic logic-	24	24	"Adiabatic" thermodynamic processes do not exchange energy with the outside world; hence no power or energy is lost. This logic decreases power dissipation when switching. It recycles energy from the load capacitance for the following action.
[19]	Fin field-effect transistor (FinFET)	CMOS-36	11	11	Many computational circuits use full adders. This study uses graphene-dielectric-metal waveguide tuning to create a compact, efficient electro-optical full adder.

In arithmetic, addition is a fundamental operation, addition-based operations like subtraction, and multiplication. The full adder is an essential module of the binary adder. Improving the performance of 1-bit full-adder is a top priority that has drawn a lot of research resources [20], [21]. Full adder develops high-performance, low-power systems. Scientists have long prioritised full adder MOSFET threshold voltage.

$$V_{th} = V_{t0} + \gamma\left(\sqrt{|2\phi_F| + |V_{sb}|} - \sqrt{|2\phi_F|}\right) \quad (1)$$

Table 2 shows that channel length (L), channel width (W), and gate and drain voltage MOSFET characteristics determine drain current.

Table 2. MOSFET properties

Parameter	Value
Gate width	120 nm
Gate length	45 nm
Supply voltage	1 V
Threshold voltage	0.7 V

$$I_D = \frac{W}{L}\mu_{n,eff}C_{ox}\left[(V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2\right] \quad (2)$$

The Boltzmann tyranny limits typical MOSFET subthreshold swing to 60 mV/decade at normal temperature, making it difficult to lower supply voltage and power usage [22]. NCFETs may benefit from future IC nodes [23]. Because of its integrated ferroelectric layer in the gate stacks, an NCFET has a larger switching current ratio [24]–[26] and a steeper subthreshold swing than a MOSFET. In devices and circuits, it improves performance while using less power. The ferroelectric material's non-stable NCE requires careful CFE-to-underlying MOSFET capacitance matching for NCFET performance [27]. NCFET transistors use a ferroelectric (FE) layer in the transistor gate stack to function at lower VDDs while retaining switching speed [28], [29]. The NCFET's threshold voltage, drain current, and device parameters are provided in (3), (4), and Table 3.

$$V_F = \rho\frac{dQ_F}{dt} + (\alpha Q_F + \beta Q_F^3) \quad (3)$$

The drain current of the NCFET is:

$$I_d = WQ_i(x_o)V_{x0}F_{sat} \quad (4)$$

Table 3. NCFET properties

Parameter	Value
Gate width	120 nm
Gate length	45 nm
Supply voltage	1 V
Threshold voltage	0.7 V

3. PROBLEM STATEMENT AND DESIGN METHOD

Portable battery-operated systems are moving towards better speeds, smaller on-chip regions, and lower power consumption [30]–[33]. Convolution, correlation, filtering, and other efficient arithmetic operations are used in modern microprocessors and digital signal processor (DSP). These operations depend on full adders. Power consumption can be reduced by reducing arithmetic operation energy. Low supply voltage and low-frequency input pulses delay and degrade an arithmetic system's circuits, reducing power consumption. Static and dynamic logic design CMOS full adder cells. Static full adder cells are simpler to develop, more dependable, and consume less power. Several logic topologies created full adder cells. Some topologies perform better than others. Table 4 describes recent real issues. Developing such systems requires full adder cell design with low power consumption and fast speed. Figure 1 illustrates the problem statement using a flowchart.

Table 4. Problem statement

Research challenge	Description
Low power	The selection of optimal transistor technology and reduction of leakage currents helps to reduce the circuit power supply.
High speed	The selection of design logic helps to achieve the design of high speed full adder.

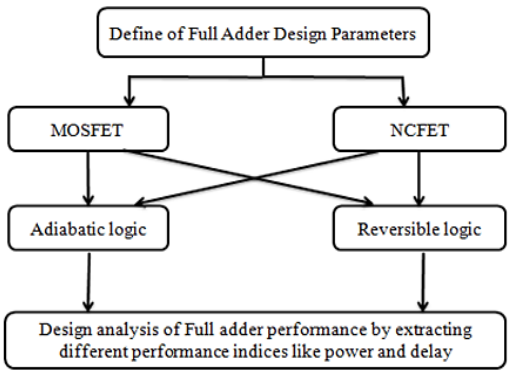

Figure 1. Detailed method

4. DESIGN AND ANALYSIS

4.1. Adiabatic logic

Adiabatic logic controls current flow and reduces energy loss from switching and the capacitor. It's done by recycling circuit energy. This approach recycles energy and slows charge transmission. Vds (nMOS or pMOS) are hard to zero, wasting energy during recovery. Adiabatic circuits enhance silicon area Figure 2. Thus, energy-efficient operation has grown popular. Adiabatic circuits have dissipated less energy than CMOS circuits for over two decades. The inability to consistently construct the power clock in Figure 3 has slowed energy-efficient adiabatic systems' progress. MOSFET and Table 5 function adiabatic logic-based complete adder. Figures 4 and 5 illustrate the NCFET-based adiabatic logic-based complete adder's design and transient response.

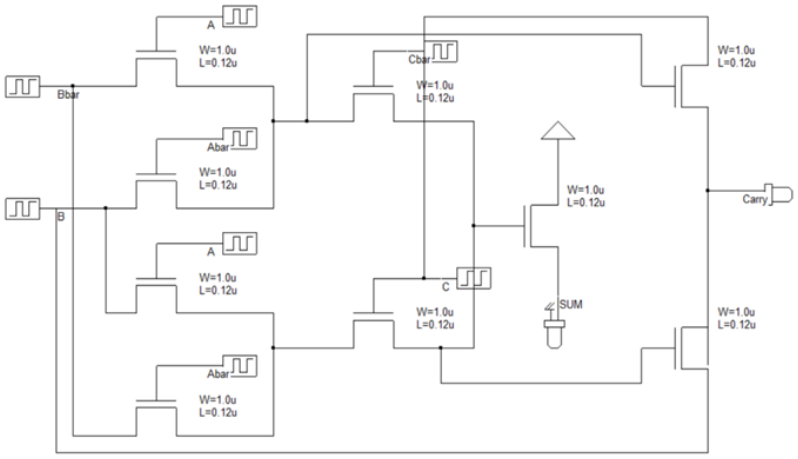

Figure 2. Adiabatic logic based full adder using MOSFET

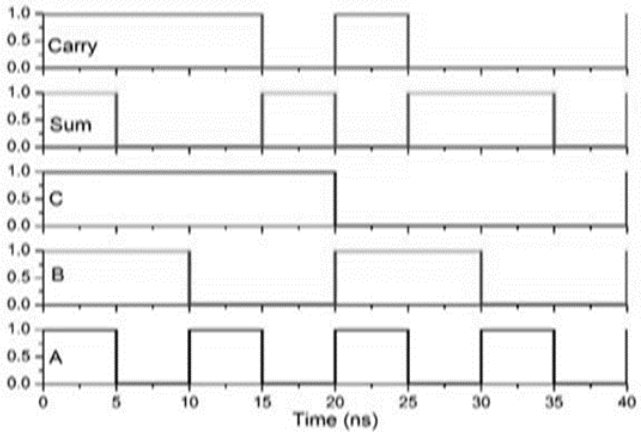

Figure 3. Adiabatic logic based full adder using MOSFET transient response

Table 5. Adiabatic logic based full adder condition analysis

A	B	C	Transistor (Q)									Sum	Carry
			1	2	3	4	5	6	7	8	9		
0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	1	1	0	0	1	1	1	1	0
0	1	0	0	1	1	0	0	1	1	0	0	1	0
0	1	1	0	1	1	1	0	1	1	1	1	0	1
1	0	0	1	0	0	0	1	0	0	0	0	1	0
1	0	1	1	1	0	1	1	1	0	1	1	0	1
1	1	0	1	1	1	0	1	1	1	0	0	0	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1

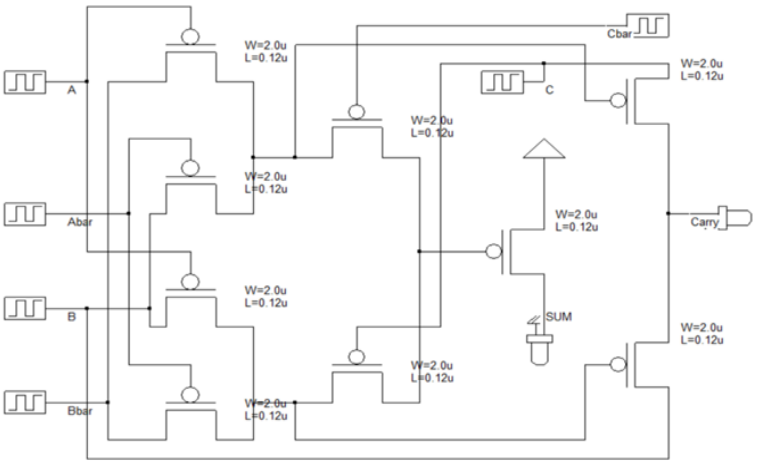

Figure 4. Adiabatic logic based full adder using NCFET

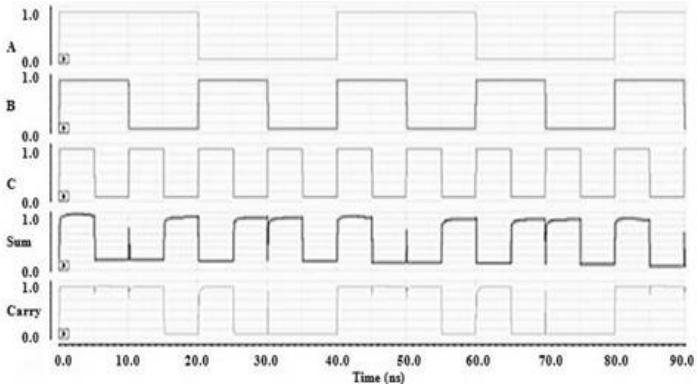

Figure 5. Adiabatic logic based full adder using NCFET transient response

4.2. Reversable logic

The proposed reversible logic based full adder using MOSFET as shown in Figure 6. In this circuit, there are three inputs (A, B, and Cin) representing the two binary numbers to be added and the carry input, and two outputs (Sum and Cout) representing the sum and carry-out of the addition. A reversible full adder using NCFETs as shown in Figure 7 can be implemented using a combination of reversible gates, such as the Toffoli gate or Fredkin gate. These gates can be constructed using NCFETs, but the actual circuit design and fabrication would require specialized expertise and tools. Figure 8 shows transient response of a NCFET refers to how the transistor behaves during the time it takes to transition from one state to another in response to a change in its input or initial conditions.

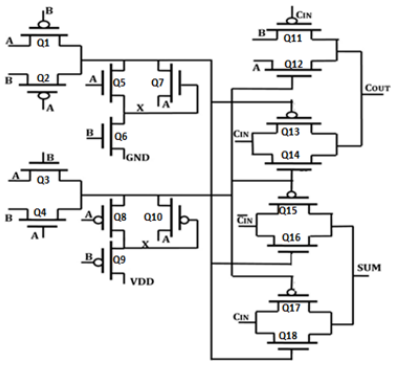

Figure 6. Full adder using reversible logic by MOSFET

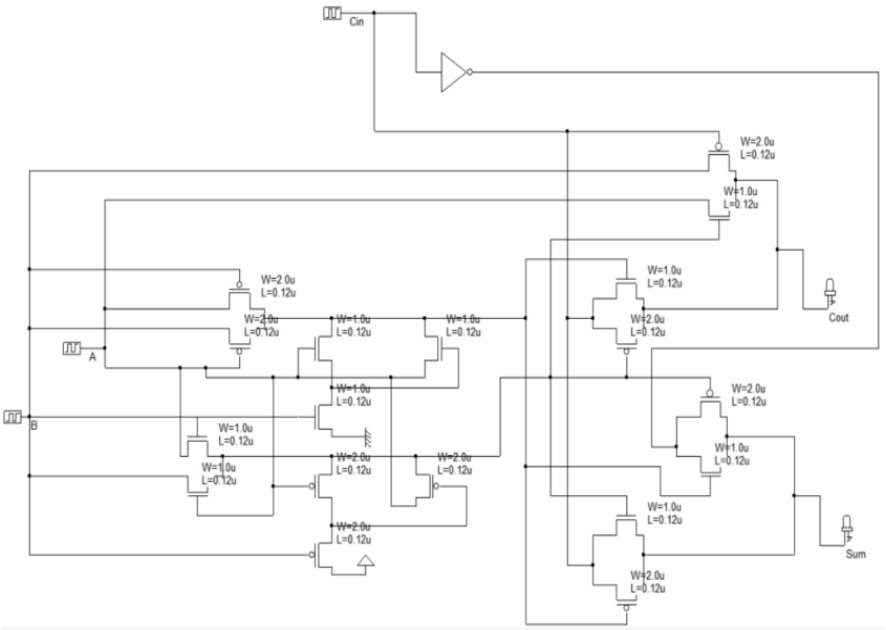

Figure 7. Reversable logic based full adderusing NCFET

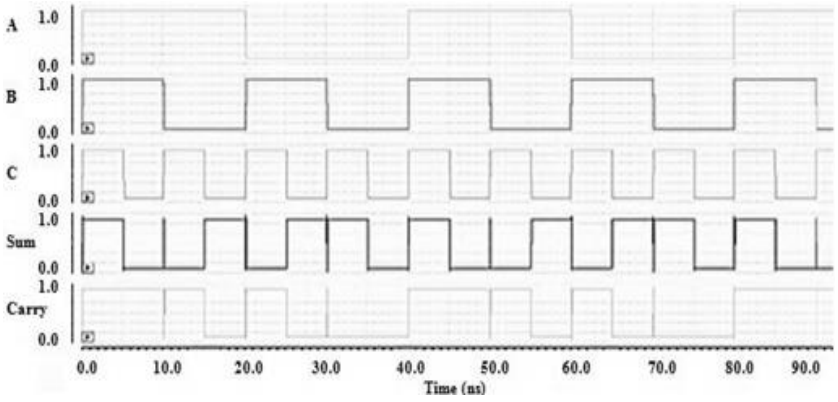

Figure 8. Full adder using reversible logic by NCFET transient response

5. RESULTS AND DISCUSSION

In order to design and analyses the simulation of the described full adder circuits, the CADANCE software was used. A MOSFET and an NCFET are used to evaluate the overall adder's performance. MOSFET and NCFET model files used for simulation and design NCFETs perform well in delay and power compared to conventional MOSFETs, as shown in Tables 6 and 7. Respectively of the comprehensive study on adiabatic and reversible logic using 45 nm technology by both MOSFET- and NCFET-based full adder.

Table 6. Comprehensive study on adiabatic and reversable logic

Logic	Adiabatic logic		Reversable logic	
	MOSFET	NCFET	MOSFET	NCFET
Transistor technology	45 nm	45 nm	45 nm	45 nm
Threshold voltage	0.7	0.7	0.7	0.7
Supply voltage	1	1	1	1
No. of transistor	8	8	18	18
Power dissipation	548 mw	552 mw	22.6 mw	7.19 mw
Delay	5.069 ns	0.023 ns	15.08 ns	1.68 ns

Table 7. Work comparison with literature

Parameters	Mamaghani *et al.* [32]	Pan and Naeemi [33]	Proposed method	
Transistor technology	FinFET	Tunneling FET	NCFET	NCFET
Gate length	27 nm	45 nm	45 nm	45 nm
Supply voltage	1.75 V	2.5 V	1 V	1 V
Threshold voltage	0.7	0.7	0.7	0.7
Logic	Magnetic	CoMET	Adiabatic logic	Reversable logic
No. of transistors	28	21	8	18
Power dissipation	746 mw	889.3 mw	552 mw	7.19 mw
Delay	8 ns	54 ns	0.023 ns	1.68 ns

Figure 9 shows the power consumption of the proposed logic 1 (552 mW) and logic 2 (7.19 mW) are stands out as the most energy-efficient among existing methods. Figure 10 shows delay of the logic 1 (1.68 ns) and logic 2 (0.023 ns) are exceptionally low delay than the existing methods. The primary takeaways from the performance analysis are that the adiabatic logic-based full adder has a fast processing speed, whereas the reversible logic-based full adder has low overall power consumption.

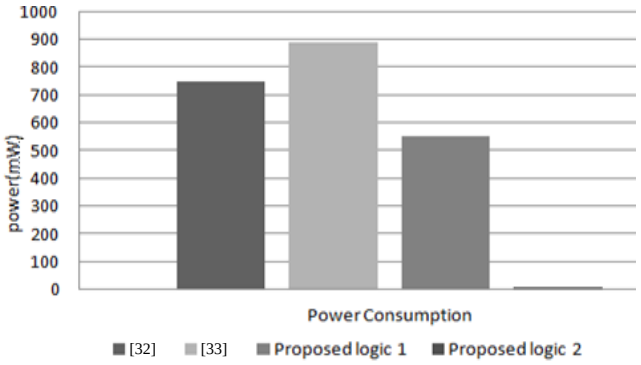

Figure 9. Power comparison with existing system

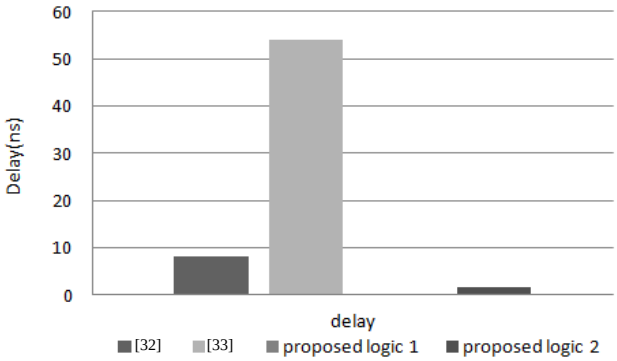

Figure 10. Delay comparison with existing system

6. CONCLUSION

NCFETs outperform MOSFETs. Reversible and adiabatic logic evaluated NCFET based complete adder performance. The performance investigation found that the adiabatic logic-based full adder is fast and the reversible logic-based one is low-power. Low-power, high-speed embedded system IC design prefers the given full adder. The choice of NCFET-based full adder, one designed using adiabatic logic and the other using reversible logic, appears to be well-suited for the needs of low-power, high-speed embedded system ICs. NCFET technology's novelty presents fabrication problems that must be overcome to seamlessly incorporate it into semiconductor processes, requiring further research for scalability and cost-effectiveness. Adiabatic and reversible logic architectures have larger circuit sizes than CMOS-based designs, which may limit space-constrained applications. These constraints highlight the need for continual research and innovation to overcome them and maximize NCFET technology's potential.

NCFET-based full adder designs have several promising futures. First, more reliable and cost-effective fabrication methods are essential to this technology's applicability for mass production. Hybrid logic architectures that combine adiabatic and reversible logic may balance power efficiency and speed, reducing area overhead. To ensure performance under varied environmental circumstances, research should also improve temperature resilience. Integration of NCFET-based designs with legacy systems should also be a priority to ease the transition. Finally, customizing complete adder designs for low-power, high-speed embedded system applications can improve performance and energy efficiency. These future efforts aim to maximize NCFET-based designs' practical uses.

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BIOGRAPHIES OF AUTHORS

Dr. Ravuri Daniel working as associate professor in the Department of Computer Science and Engineering, Prasad V. Potluri Siddhartha Institute of Technology, Vijayawad, India. He has industrial, national, and international teaching experience. Awarded Ph.D. from Jawaharlal Nehru Technological University Kakinada (JNTU Kakinada), M.Tech. from Andhra University, and B.Tech. from Jawaharlal Nehru Technological University. His area of research in the field of computer networks, wireless sensor networks, internet of things, data analytics, AI, and embedded systems. Presently, he is exploring innovative applications in IoT with data analytics. He's an ISTE lifer. He can be contacted at email: danielravuri@gmail.com.

Dr. Bode Prasad received his master's degree from Koneru Lakshmaiah Engineering College in Guntur, India, and obtained his Ph.D. degree from Andhra University College of Engineering, Visakhapatnam, India in the year 2015. He currently holds the position of Professor in the Department of Information Technology at Vignan's Institute of Information Technology (A) in Visakhapatnam, India. His research interests span a wide range of topics, including computer networks, mobile ad-hoc networks, cloud computing, wireless networks, machine learning, data science, artificial intelligence, human action analysis, and sign language machine translation. He can be contacted at email: arjunprasad.bode@gmail.com.

Dr. Abhay Chaturvedi is working as associate professor in the Department of Electronics and Communication Engineering, GLA University, Mathura, U.P. He has about twenty years of teaching/research experience. He received B.E. in electronics and communication engineering and M.E. in microwave communication and radar engineering from Dr. B.R. Ambedkar University, Agra, U.P. He received Ph.D. in communication engineering from Rajasthan Technical University, Kota, Raj. He is life member of IETE New Delhi, ISTE New Delhi, ISCA Kolkata and SSI Thiruvananthapuram. He can be contacted at email: abhaychat@gmail.com.

Dr. Chinthaguntla Balaswamy got a 1998 B.E. in electronics and communication engineering from S.R.K.R. Engineering College, Bhimavaram. Malnad College of Engineering, Hassan, awarded him an M.Tech. in electronics and communication engineering in 2001. In 2010, Jawaharlal Nehru Technological University, Anantapur, awarded him a Ph.D. He taught engineering colleges for 21 years. He mentored three computer communication and networking Ph.D. He teaches and advises R&D at Sheshadri Rao Gudlavalleru Engineering College. Computer networking, embedded systems, and VLSI interest him. He can be contacted at email: balaswamy@gecgudlavallerumic.in.

Mr. Dorababu Sudarsa M.Tech. in information technology from Sathyabama University, Chennai, 2009. JNT University, Hyderabad, awarded him a B.Tech. in computer science and information technology in 2002. He received the Best Teaching Faculty Award from Koneru Lakshmaiah University, Vadeswaram, Guntur, India, and Audi Sankara College of Engineering and Technology, Gudur, India. He taught 18 years total. Cloud computing, data mining and warehousing, data science, and IoT interest him. 15 international publications and conferences published him. He's an ISTE lifer. He can be contacted at email: dorababu.sudarsa@gmail.com.

Dr. Nallathambi Vinodhkumar B.E. in electronics and communication engineering, M.E. in computer and communication, and Ph.D. in nanoelectronics from Anna University, Chennai, in 2007, 2010, and 2017. He was a one-year post-doctoral fellow at Chang Gung University's Centre for Reliability Sciences and Technology. He is an ECE associate professor at Vel Tech Rangarajan Dr. Sagunthala R&D Institute of Science and Technology, Chennai. IEEE and Electron Devices Society members. 27 journal and conference publications. He studies low-power VLSI, nanodevices, and radiation impacts in CMOS devices and circuits. He can be contacted at email: vinodhkumar.cc@gmail.com.

Ramakrishna Reddy Eamani B.Tech. in electronics and communication engineering from Jawaharlal Nehru Technological University, Hyderabad, 2008; M.E. in VLSI design from Anna University, Coimbatore, 2010. He is an associate professor at the Department of Electronics and Communication Engineering in Usha Rama College of Engineering and Technology-Autonomous affiliated to Jawaharlal Nehru Technological University, Kakinada, and a Ph.D. candidate at Vel Tech Rangarajan Dr. Sagunthala R&D Institute of Science and Technology, Avadi, Chennai, Tamil Nadu, India. He studies DIP/DSP low-power and low-complexity VLSI architectures. He can be contacted at email: erkrishnareddy.phd@gmail.com.

Dr. Ambarapu Sudhakar since 2019 as professor and head of the Electrical and Electronics Engineering Department at MLR Institute of Technology, Hyderabad, Telangana, India. He taught engineering colleges for 17 years. He likes electric drives, and clever controllers. He has several patents and research articles in indexed journals. Research earned him the 2016 INDUS Research Excellence Award. He wrote a textbook and offered expert webinars and conferences. He organised state and national conferences with Indian government subsidies. He can be contacted at email: sudhakar.a@mlrinstitutions.ac.in.

Dr. Bodapati Venkata Rajanna received B.Tech. degree in electrical and electronics engineering from Chirala Engineering College, JNTU, Kakinada, India, in 2010, M.Tech. degree in power electronics and drives from Koneru Lakshmaiah Education Foundation, Guntur, India, in 2015 and Ph.D. in electrical and electronics engineering at Koneru Lakshmaiah Education Foundation, Guntur, India, in 2021. Currently, he is working as an associate professor at MLR Institute of Technology, Hyderabad. His current research includes, dynamic modeling of batteries for renewable energy storage, electric vehicles and portable electronics applications, renewable energy sources integration with battery energy storage systems (BESS), Smart metering and smart grids, micro-grids, automatic meter reading (AMR) devices. He can be contacted at email: rajannabv2012@gmail.com