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FPGA-based fault analysis for 7-level switched ladder multi-level inverter using decision tree algorithm

Nithya Ramalingam, Anitha Thiagarajan
Department of Electronics and Instrumentations, Faculty of Engineering, Annamalai University, Chidambaram, India

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ABSTRACT

The proposed method involves the fault analysis of the inverter switches present in the multi-level inverter (MLI) circuitry. The decision tree machine learning algorithm is incorporated for the fault analysis of the inverter switches. The multi-level inverter utilized in this work is a 7-level switched ladder multi-level inverter. There is 4 number of switches in the design of a 7-level inverter driven by the non-carrier digital pulse width modulation signals. The non-carried-based digital pulse-width modulator (DPWM) generation is generated using the event angle for the 7-level of the switched ladder inverter. The proposed method investigates the stuck-at-fault occurrences of the 4 switches in the inverter by manipulating the decision tree parameters such as entropy, information gain, and decision tree. Based on the decision tree, the very high-speed integrated circuit hardware description language (VHDL) code is developed by making use of the behavioral modeling and validated for the power, area in the Xilinx Vivado tool. The real-time feasibility is verified for the proposed method by synthesizing the developed VHDL code in the field programmable gate array (FPGA) device.

Corresponding Author:

Nithya Ramalingam
Department of Electronics and Instrumentations, Faculty of Engineering, Annamalai University
Annamalai Nagar, Chidambaram, Tamil Nadu 608002, India
Email: nithyaramalingam1989@gmail.com

1. INTRODUCTION

The multi-level inverter is a power converter that converts DC to AC voltage and is used in many industrial applications. Conventionally, the multi-level inverter (MLI) circuits were driven by the static DC source with its performance based on the topology, driving sources, switch types, pulse width modulation (PWM) generation, and control algorithm. In real-time, the advent of renewable resources provided the opportunity to prominently use power inverters. Though the power inverters were used, the fault occurrence in the circuitry is a major issue that affects the performance of the power applications. To overcome these faulty circuits, several soft computing techniques and bio-inspired algorithms were utilized, but the accuracy of the fault identification was low and demanded enhancement for real applications.

Artificial intelligence techniques such as deep learning and machine learning algorithms are used in recent times to precisely detect faults in power systems. The fault analysis for photovoltaic (PV) systems can be achieved by using the machine learning algorithm [1]. Machine learning algorithms are used to find the faults of switching devices in the PV system with fewer computations [2], [3]. To fasten the error detection in the PV system, deep learning can be considered that includes the equilibrium optimizer algorithm and long short-term memory (LSTM) in real-time implementation [4]. The decision tree is suitable for the fault analysis of the non-linear behavior of the PV modules [5].

Ensemble learning is utilized for the feature extraction and phase selection for grid-connected PV systems [6]. The performance of the grid-connected PV systems is enhanced by developing the ensemble learning-based fault identification algorithm considering the dynamic nature of the solar panel [7]. The full processing system that consists of a photovoltaic power station can identify the fault occurrence on the run using machine learning algorithms [8]. The output voltage timing waveforms of the closed-loop PV grid-connected inverters are monitored for faults in working conditions using the insulated gate bipolar transistor (IGBT) open-circuit fault diagnosis [9].

To optimize the open circuit faults in the inverter topology design, machine learning techniques are tried rather than extracting the fault harmonic of the switch [10]. By utilizing the supervised machine learning algorithm, the fault occurrence can be identified using the k-nearest neighbors (KNN) algorithm, and prediction for the next step in the inverter input voltage can be achieved through the LSTM algorithm [11]. The power system parameters are forecasted by artificial intelligence to eradicate the sudden flow of current, power failure, and current leakage in industrial drives [12]. The line location and variable impedance faults happening in the transmission line connected inverter-generator can be diagnosed using the machine learning-based technique [13]. The faulty phases are extracted by the Pearson correlation coefficient-based technique for the micro-grid fed inverter based generator [14]. The classification and regression tree (CART) method can be utilized for the fault location of a single-phase grounding in real-time power converters [15]. The DC faults can be analyzed using the teager-kaiser energy operator algorithm which has low computation time and complexity [16].

The fault detection in power electronics systems is fused with short-time fourier transform to examine the three-phase inverters [17]. The switching faults are tested for tolerance to affirm the durability of the multi-level inverter [18]. The fault identification is performed with the cascaded H-bridge multilevel inverter (CHMLI) circuit using the deep convolutional neural network through imaging [19]. The 7-level multi-level inverter is diagnosed for faults using the cuckoo search algorithm with radial basis function is advantageous for prediction [20]. The AC/DC interleaved boost converter is checked for output ripple faults using the artificial neural network (ANN) model [21]. The open-circuit faults of IGBT can be located using the accuracy-weighted random forest algorithm [22].

To implement the fault analysis method, several digital controllers are available, but the field programmable gate array (FPGA) is used for the real-time control of the power inverters. The very high speed integrated circuit hardware description language (VHDL) code is developed for the digital pulse-width modulator (DPWM) generation and its control of the DC-DC voltage regulator and implemented in the FPGA for real-time validation [23] The FPGA-based control for the PV-fed DC-DC-AC converter gives accuracy and low total harmonic distortion (THD)% in the implementation of 81-level MLI [24]. The FPGA-based neuro-genetic algorithm for backward propagation of neural networks can be used for fault detection in induction motor drives [25]. This paper deals with the analysis of the fault that occurs in the switches of the switched ladder type MLI circuit using the decision tree algorithm implemented in the FPGA device. The next section discusses the working of the proposed algorithm in detail.

2. PROPOSED METHOD: DECISION TREE-BASED FAULT ANALYSIS FOR MLI

The proposed method identifies the fault in the level-7 switched ladder multi-level inverter using the decision tree machine learning algorithm. Level 7 consists of 3 levels each in a positive and negative cycle and a zero level in the AC output. The switched ladder inverter uses the trinary pattern for the inputs of the DC voltages. For the level-7 starter lightning and ignition (SLI), the switching voltages are 1 V, 3 V, -1 V, and -3 V which constitute the four switches namely SW1, SW3, SWb1, and SWb3 respectively. The switch patterns are generated for the four switches based on the 12 switching angles that are generated by the half height-switching angle method (HH-SAM) algorithm. The four switch patterns for the 7-level SLM are given in Table 1. The topology of the 7-level switch ladder multilevel inverter (SLMLI) utilized for this work is depicted in Figure 1. The voltage pattern is given in trinary form for each ladder stage of the inverter. The proposed 7-level SLMLI utilizes only 8 switches to attain the required output of the MLI circuit. Also, there is no need for carriers for the generation of PWM signals as compared to the cascaded based reversing voltage inverter circuit [26]. Though the reverse voltage inverter uses 10 switches for the 15-levels, the proposed Switched Ladder Trinary Multi-Level Inverter (SLTMLI) uses only 8 switches and is more precise in the generation of the 15-levels [27].

The four switch patterns are represented by the decimal equivalent considering the SW1 as the most significant bit (MSB) and SWb3 as the least significant bit (LSB). Thus the switches SW1, SW3, SWb1, and SWb3 are manipulated for the used states namely 0, 1, 2, 4, 6, 8, and 9. The remaining equivalent values such as 3, 5, 7, 10, 11, 12, 13, 14, and 15 are destinated as unused states. The data set for identifying the switching table is developed as per the used and unused states. The used states are considered to be valid with the

decision of "YES" designated as 'Y' and the unused states are taken as invalid with the decision of "NO" designated as 'N'. The decision tree algorithm is utilized in this work to identify the switching faults of the 7-level switched ladder multi-level inverter (SLM). The entropy is manipulated for the switches of the SLM from SW1 to SWb3. The formulation for the entropy for the SW1 is given by (1).

$$SW1 = -\frac{13}{22}log_2\left(\frac{13}{22}\right) - \frac{9}{22}log_2\left(\frac{9}{22}\right) \quad (1)$$

Similarly, the entropy for the number of "1s" and number of "0s" in the SW1 is depicted in (2) and (3) respectively.

$$SW1_{(1)} = -\frac{4}{10}log_2\left(\frac{4}{10}\right) - \frac{6}{10}log_2\left(\frac{6}{10}\right) \quad (2)$$

$$SW1_{(0)} = -\frac{9}{12}log_2\left(\frac{9}{12}\right) - \frac{3}{12}log_2\left(\frac{3}{12}\right) \quad (3)$$

The gain of the SW1 is given by (4).

$$Gain = Entropy\ of\ SW1 - \frac{10}{22}(Entropy\ of\ \text{"1s" in SW1}) - \frac{10}{22}(Entropy\ of\ \text{"0s" in SW1}) \quad (4)$$

The calculation of entropy and gain for the SW3 are evaluated as depicted in (5).

$$SW3 = -\frac{13}{22}log_2\left(\frac{13}{22}\right) - \frac{9}{22}log_2\left(\frac{9}{22}\right) \quad (5)$$

Similarly, the entropy for the number of "1s" and number of "0s" in the SW3 is depicted in (6) and (7) respectively.

$$SW3_{(1)} = -\frac{3}{9}log_2\left(\frac{3}{9}\right) - \frac{6}{9}log_2\left(\frac{6}{9}\right) \quad (6)$$

$$SW3_{(0)} = -\frac{10}{13}log_2\left(\frac{10}{13}\right) - \frac{3}{13}log_2\left(\frac{3}{13}\right) \quad (7)$$

The gain of the SW3 is given by (8).

$$Gain = Entropy\ of\ SW3 - \frac{9}{22}(Entropy\ of\ \text{"1s" in SW3}) - \frac{13}{22}(Entropy\ of\ \text{"0s" in SW3}) \quad (8)$$

Table 1. Switching pattern for the fault identification in the 7-level SLM

Levels	SW1	SW3	SWB1	SWB3	Decision	Equivalent
0	0	0	0	0	Y	0
1	1	0	0	0	Y	8
2	0	1	1	0	Y	6
3	0	1	0	0	Y	4
2	0	1	1	0	Y	6
1	1	0	0	0	Y	8
0	0	0	0	0	Y	0
-1	0	0	1	0	Y	2
-2	1	0	0	1	Y	9
-3	0	0	0	1	Y	1
-2	1	0	0	1	Y	9
-1	0	0	1	0	Y	2
0	0	0	0	0	Y	0
Unused states	0	0	1	1	N	3
	0	1	0	1	N	5
	0	1	1	1	N	7
	1	0	1	0	N	10
	1	0	1	1	N	11
	1	1	0	0	N	12
	1	1	0	1	N	13
	1	1	1	0	N	14
	1	1	1	1	N	15

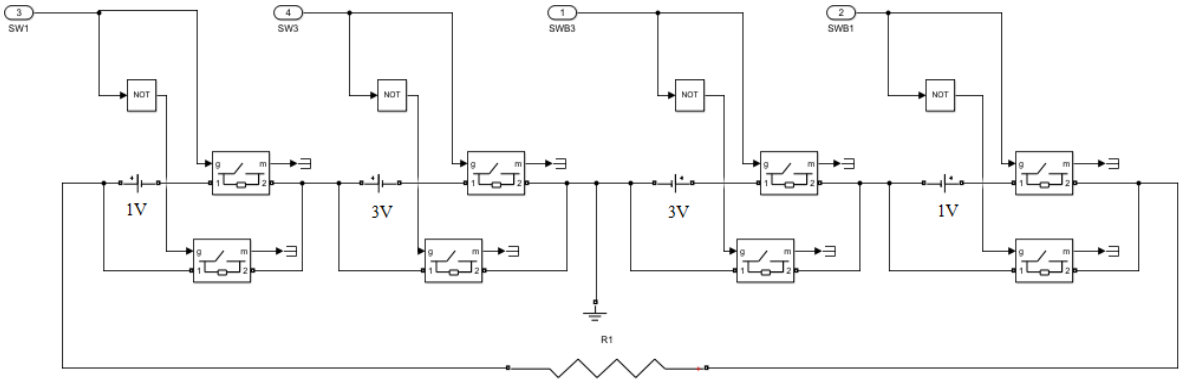

Figure 1. Circuit topology for the proposed 7-level switched ladder multi-level inverter

Due to the symmetricity of the switch patterns, the number of 1's and 0's for the negative switches are the same which leads to the same value of the entropy and gain as in positive switches. Thus the negative switches are not considered for the evaluation in the decision tree algorithm. Table 2 consolidates the entropy and gain for the two switches SW1 and SW3. The gain of SW3 is 0.13976 and higher than SW1 with 0.09217. Now comparing the two switches, the SW3 is the root node for the decision tree of the proposed fault identification in 7-level SLM. The flowchart for the proposed method is depicted in Figure 2. The VHDL code is used to develop the proposed decision tree algorithm for the identification of the faults in the 7-level SLM.

Table 2. Entropy and gain calculation for the switches using the decision tree algorithm

Sl.No	Parameters	SW1	SW3
1	Entropy total	0.97603	0.97603
2	The entropy of only 1's	0.97095	0.91849
3	The entropy of only 0's	0.81128	0.77934
4	Gain	0.09217	0.13976

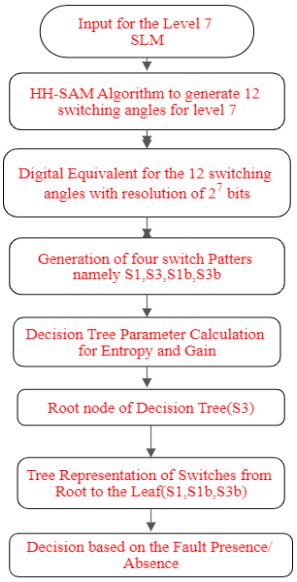

Figure 2. Flowchart for the proposed decision tree algorithm based fault analysis of 7-level SLM

3. RESULTS AND DISCUSSION

The proposed fault analysis of switches in the ladder MLI is evaluated using the decision tree algorithm using the VHDL code. The decision tree parameters namely entropy and gains are manipulated for

deriving the splitting tree. Initially, the positive side switches are considered for the decision tree and the gain value is maximum for the SW3 as compared to the remaining switches, thus, the SW3 is considered the root node for the tree. With the SW3 as the root node, there are 13 combinations for fault free decision and 9 combinations for faulty decision as depicted by (13,9). The decision tree (DT) checks for the value of SW3 and based on the value of either "0" or "1", the next node SW1 is evaluated with 3 positive decisions and 6 negative decisions as given (3,6) for SW3=0. For SW3=1, the SW1 node is evaluated for (10,3). Similarly, the next nodes of SWB3 are evaluated as (3,2) with SW3=1 and SW1=1. For SW3=0 and SW1=X, the nodes of SWB3 and SWB1 are utilized for the decision of fault and fault free switches in the inverter. Figure 3 shows the complete decision tree for the proposed fault analysis for the switching combination of the multilevel inverter.

The VHDL code is developed for the derived decision tree using the nested-if-else loop in behavioral style. The simulation for the developed VHDL is verified using the ModelSim compiler as shown in Figure 4. The Xilinx Vivado tool is used for the validation of the synthesizable code of the proposed switching fault analysis. The register transfer level (RTL) schematic for the proposed method is given in Figure 5. The proposed method is evaluated for power consumption using the Xilinx Vivado tool as given in Figure 6. Figure 7 depicts the AC output for the 7-level switched ladder trinary multi-level inverter with the THD% value. The dynamic power manipulated for the proposed switching fault analysis is 1.134 W and the static power is 0.095 W. The device utilization chart for the proposed method using the Xilinx Vivado tool is given in Table 3. Table 4 depicts the comparison of the proposed method with THD% and proves to be low at 12.52% compared to multi-carrier sinusoidal pulse width modulation (MCSPWM) and multi-carrier space vector pulse width modulation (MCSVPWM) in [28] and since no carrier is used, the modulation index (M) is not assigned.

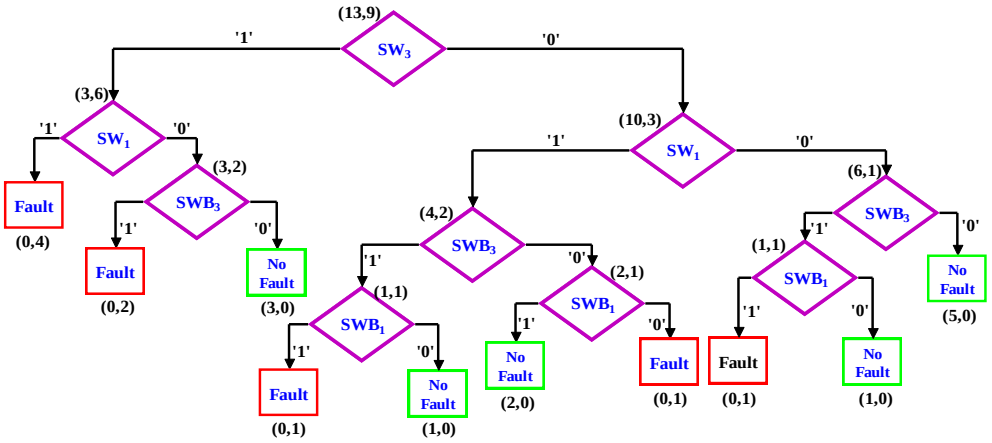

Figure 3. Decision tree for the proposed switching fault identification in SLM

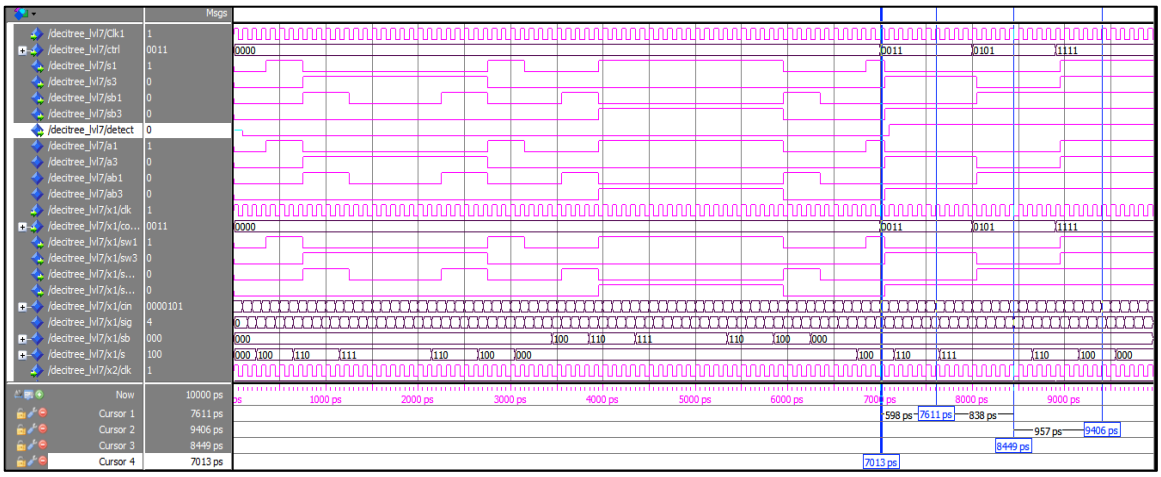

Figure 4. Simulation output for the proposed decision tree based switching fault identification in SLM

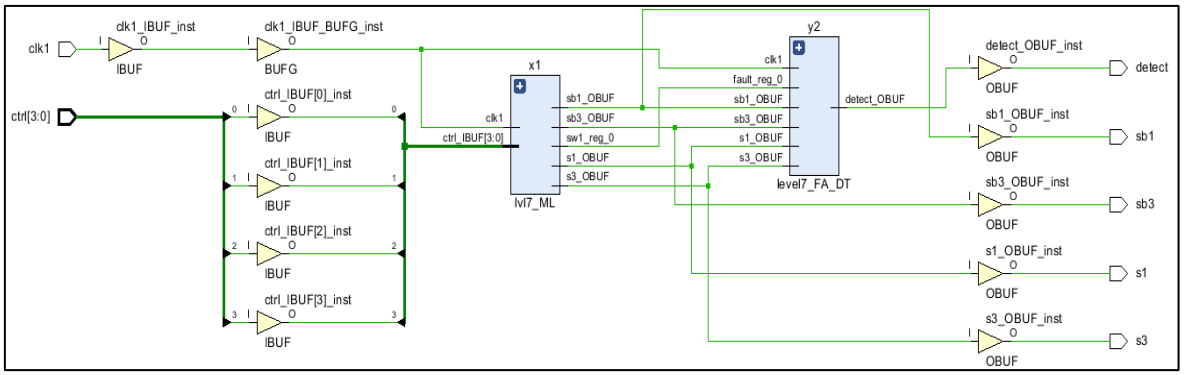

Figure 5. RTL schematic for the proposed decision tree based switching fault identification in SLM

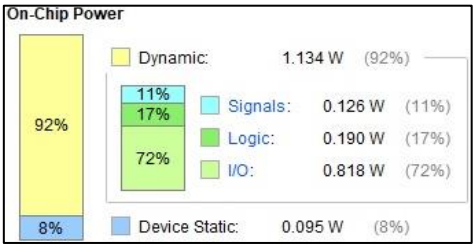

Figure 6. Power dissipation for the proposed decision tree based switching fault identification in SLM

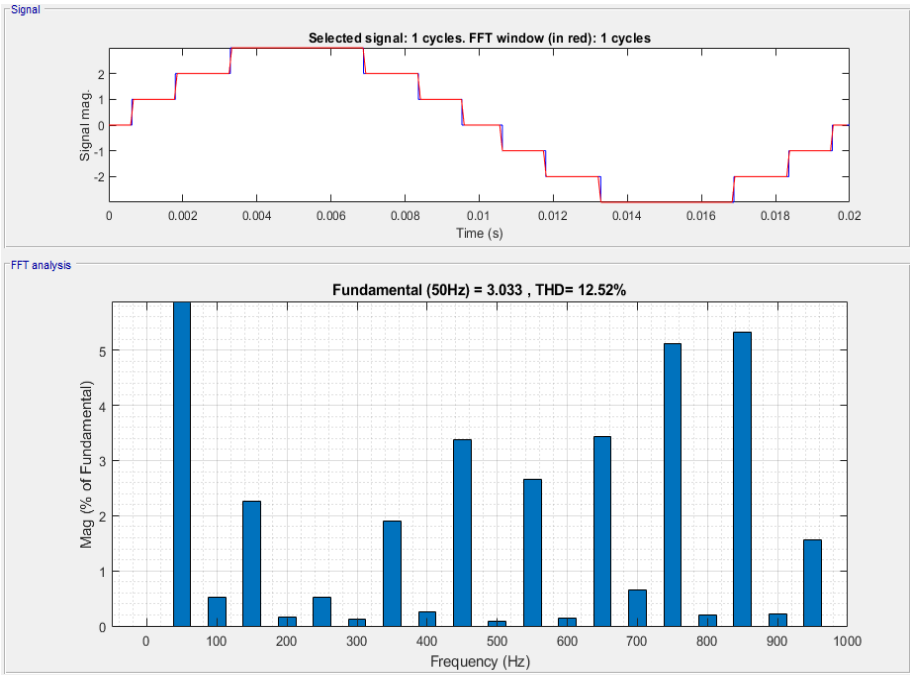

Figure 7. THD% evaluation for the proposed 7-level SLTLI using the MATLAB Simulink tool

Table 3. Device utilization for the proposed decision tree-based switching fault identification in SLM

Resource	Utilization	Available	Utilization (%)
Look up table (LUT)	25	63,400	0.04
Flip-flops (FF)	8	126,800	0.01
Input/output (IO)	10	170	5.88
Clock buffer (BUFG)	1	32	3.13

Table 4. Comparison of THD% for the 7-level MLI AC OUTPUT

Methods	THD% for the simulation AC output		
	MCSPWM [28]	MCSVPWM [28]	Proposed
7-level with M=0.8	24.33	21.84	12.52
7-level with M=0.7	25.31	24.27	

4. CONCLUSION

The proposed switching fault analysis using the decision tree algorithm is validated using VHDL code. The developed VHDL code identifies the stuck-at faults of the inverter switches using the decision tree algorithm. The parametric evaluation for the proposed method seems to be satisfactory and feasible for the real-time fault analysis of the multi-level inverter. The proposed algorithm can be utilized for identifying faults in the switches of the higher resolution inverter level design and can direct towards the use of neural network-based fault identification in multi-level inverter switches.

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BIOGRAPHIES OF AUTHORS

Nithya Ramalingam was born in 1989 in Cuddalore, Tamil Nadu. She obtained B.E. [Electronics and Communication] degree from Anna University in the year 2010 and M.Tech. [Embedded Systems] degree from Sathyabama University in the year 2012. She has put in 6 years of service in teaching. She is currently a research scholar in the Department of Electronics and Instrumentation Engineering at Annamalai University, Chidambaram, Tamil Nadu, India. Her research interest includes VLSI design, development of digital control for converters, FPGA implementation of control algorithms, renewable energy sources-based power converters for real applications. She can be contacted at email: nithyaramalingam1989@gmail.com.

Anitha Thiagarajan received her B.E., M.E., and Ph.D. degrees in Electronics and Instrumentation Engineering from the Annamalai University, Chidambaram, India in 1998, 2005, and 2017 respectively. She is currently working as Associate Professor at the Department of Electronics and Instrumentation Engineering, Annamalai University, India since 1999. Her current research interests include power electronic converters, renewable energy systems, process control, and embedded systems. She published more than thirty papers in international journals and has more than ten years of research experience in power electronics. She can be contacted at email: rgm_anitha@rediffmail.com.