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Design and memory optimization of hybrid gate diffusion input numerical controlled oscillator

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ABSTRACT

The numerically controlled oscillator (NCO) is one of the digital oscillator signal generators. It can generate the clocked, synchronous, discrete waveform, and generally sinusoidal. Often NCOs care utilized in the combinations of digital to analog converter (DAC) at the outputs for creating direct digital synthesizer (DDS). The network on chips (NOCs) are utilized in various communication systems that are fully digital or mixed signals such as synthesis of arbitrary wave, precise control for sonar systems or phased array radar, digital down/up converters, all the digital phase locked loops (PLLs) for cellular and personal communication system (PCS) base stations and drivers for acoustic or optical transmissions and multilevel phase shift keying/frequency shift keying (PSK/FSK) modulators or demodulators (modem). The basic architecture of NCO will be enhanced and improved with less hardware for facilitating complete system level support to various sorts of modulation with minimum FPGA resources. In this paper design and memory optimization of hybrid gate diffusion input (GDI) numerically controlled oscillator based on field programmable gate array (FPGA) is implemented. compared with NCO based 8-bit microchip, memory optimization of hybrid GDI numerically controlled oscillator based on FPGA gives effective outcome in terms of delay, metal-oxide-semiconductor field-effect transistors (MOSFET's) and nodes.

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1. INTRODUCTION

Since its inception the communication fields have been noticed many enhancements. Some of the reasons behind it are the requirements of good design, efficiency of power and area [1]. In communication devices the most important block is numerically controlled oscillator (NCO). The NCO is one of the computerized signal generators which can generate discrete-time, synchronous (timed) and discrete esteemed waveform representational basically sinusoidal.

Usually the NCOs can be used as the part of conjunction with digital to analog converter (DAC) at the output side for makingdirect digital synthesizer (DDS). The NCO provides a certain focal point over various types of oscillators regarding security, quality of unwavering, exactness and quality. The NCO can be used as

the segment of corresponding frameworks include computerized up/down converters which are utilized inadvanced PLLs, programming radio frameworks and 3G remote, multi-level phase shift keying/frequency shift keying (PSK/FSK)demodulators or modulators (modem)and drivers for the transmission of acoustics or optic [2]–[4].

The NCO is an electronic architecture to incorporate the scope of frequencies from changing time base. Unlike a simple recurrence synthesizer based on stage bolted circle, the NCO fits to combine the extensive varieties of exact recurrence proportions [5]–[8]. In addition, the NCOs are known as DDS, is an intensive technique used as the part of radio recurrence signals era to use in utilizations assortment from radio collectors for signs generators and certain more.

The basic NCO uses time space sufficiency tests for sinusoidal waveform creation and its recurrence can be controlled through the computerized control word in solitary time clock cycle. The output recurrence of NCOs may alter right away with no procurement and lock delay times are associated with classical phase locked loop (PLL) synthesizers. The yield recurrence of NCO is observed by the info check/entire number quality. Fundamentally inside the NCO center is comprised with stage gatherer and a stage to plentifulness converter (PAC) [9]–[12].Two or more look up tables (LUTs), that can store the samples of cosine and sine waveforms are used by the larger portion of PACs and the stage to-sufficiency transformation is finished by some related rationale.

The DDS is one of the most popular and widely utilized synthesizers in digital systems include digital communication where they can be utilized for sinusoidal sequences generation. In most of the implementation the DDS will be in voltage-controlled oscillator (VCO) form or in digital world it is named as NCO. Here, "control" means changing the oscillator output frequency by a control input [13]–[17].

The LUT-based NCOs are used majority as they are analyzed first. The simplest NCOs including phase accumulator, certain output bits of which can drive the address inputs of read only memory (ROM) filled with sinusoidal samples is as shown in Figure 1. If the input of accumulator is changed then the frequency of output will be controlled. The frequency finer controller is allowed by the phase truncation bits. In many cases where field programmable gate arrays (FPGAs) are employed, NCO tables are actually random-access memory (RAMs) whose contents are altered in operating conditions providing great flexibility. Therefore LUT based network on chips (NOCs) are well suited in digital designs with FPGAs [18]–[21].

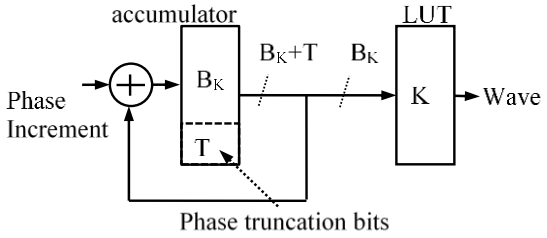

Figure 1. Basic table based NCO

However, the LUT based NOCs tending for consumption of more power for more memory and the memory circuits may draw power even when they are not accessed. Therefore, authors aimed to reduce/compress memory size while preserving the quality of output signal. The studies ranging from the employment of certain trigonometric identities for linear/nonlinear interpolation between the sample points stored in the ROM.

One of the most used quality measures for generated sinusoidal is spurious free dynamic range (SFDR) that can give the amplitude differences between targeted frequency component and further strongest component over the frequency spectrum. This SFDR offers an idea over generated signal spectral purity and the higher will be better. In quadrature NOCs same quality measures are utilized i.e., sine and cosine signal at output [22].

The NCO sometimes called a local oscillator which generates digital samples of two sine waves precisely offset by 90 degrees during phase creation of cosine as well as sine signals. This can use the sine/cosine LUTs and a digital phase accumulator (i.e., adder). The clock of analog to digital converter (ADC) is passing through the local oscillator. The local oscillator generates the digital samples with the sample rate which can exactly equal to the clock frequency of ADC sample i.e. fs. As the data rates from the two mixer input sources would be at the sampling rate of ADC i.e., fs and the output samples of complex mixer are at fs. The local oscillator sine and cosine input will create an In-phase and quadrature (I and Q) output which would be vital to maintain the phase information of an input signal.

The decimating low pass filter (LPF) may accept the input samples from the output of mixer at full sampling frequency (fs) of ADC. It may use the digital signal processing (DSP) for the implementation offinite impulse response (FIR) filter transfer function. This filter allows the passage of all signals from 0 Hz to a programmable bandwidth or cutoff frequency and rejects the signals which can have frequency above cutoff [23]. Digital filter is one of the most complex filters that will process I and Q signals from mixer. The conventional NCO is shown in Figure 2.

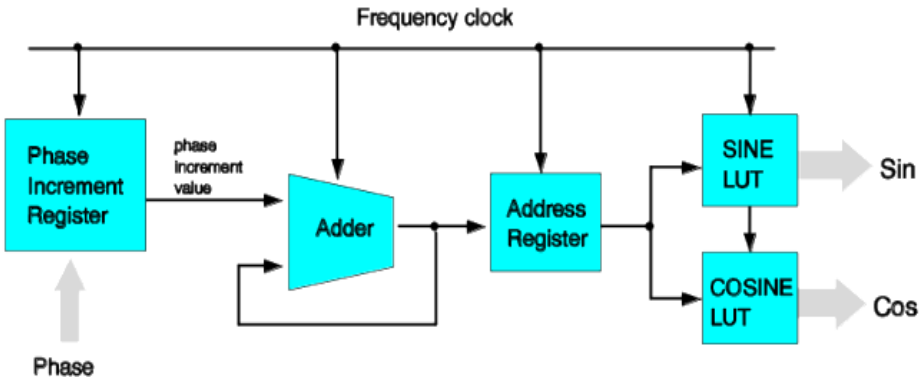

Figure 2. Conventional NCO

2. NUMERICALLY CONTROLLED OSCILLATOR FOR MICROCHIP 8-BIT MCU

Thenumerically controlled oscillator (NCOx) module shown in Figure 3 is a timer and it utilizes an accumulator overflow for output signal generation. The overflow of accumulator can be controlled with the adjustable increment value instead of post-scaler increment or single clock pulse. This may offer an advantage on simpler time driven counter where division resolution won't change with limited postscaler/prescaler divider values [24]. The NCOx module is mostly useful for the applications which may need fine resolution and frequency accuracy at a fixed duty cycle (FDC). Features of the NCOx include:

- 16-bit increment function
- Multiple clock input sources
- FDC mode
- Interrupt capability
- Output polarity control
- Output pulse width control
- Pulse Frequency (PF) mode

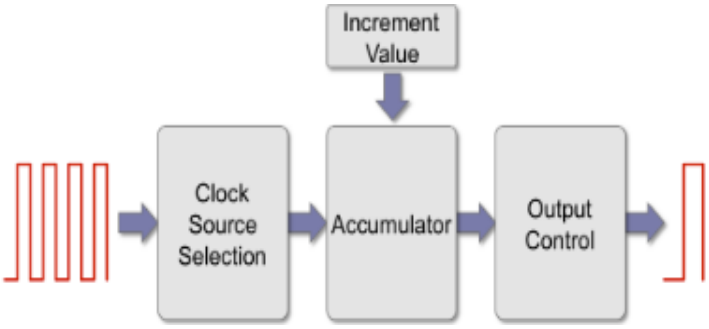

Figure 3. Numerically controlled oscillator for microchip 8-bit MCU

The NCOx is operated by adding the fixed value repeatedly to the accumulator. The additions will appear at input clock rate. The accumulator is overflowed with the carry periodically that is the raw output of NCOx. This will effectively reduce the input clock by a ratio of added value to the maximum value of accumulator.

Further the output of NCOx is modified by toggling a flip-flop or stretching the pulse. Then modified NCOx output can be internally distributed to peripherals and optionally output to I/O pin. An interrupt is generated by the overflow of accumulator. The period of NCOx is varying in discrete steps for average frequency creation. Based in the abilities of receiving circuit (i.e., external resonant converter circuitry) this output averages the output of NCOx for reducing uncertainty [25].

The NCO module overflow is expressed as:

$$\text{Accumulator Overflow Rate} = \frac{\text{Accumulator Overflow Value}}{\text{Input Clock Frequency} \times \text{Increment Value}}$$

the NCO module may provide the output signal in any of two modes namely: i) fixed duty cycle and ii) pulse frequency modulation.

The FDC mode will toggle the output on every flow of accumulator. If the clock and adder values do not change then this results 50% duty cycle as output. The PF modulation triggers the pulse on every overflow of accumulator to the period set by 3 bits in numerically controlled oscillator (NCO) register. The accumulator is a 20-bit register and it can have maximum value of 1,048,575. The accumulators write and read access is available by the registers:

- NCOxACCL
- NCOxACCH
- NCOxACCU

The NCOx adder is a full adder that will operate independently from a system clock. This can add the increment values to accumulator over every clock pulse of NCO. This adder will take the value from accumulator and it is added to increment value and the obtained result is stored in the accumulator. The value of accumulator is roll over and the value beyond 1,048,575 is stored as initial value in the accumulator. When a zero is written to the accumulator then it is reset. Normally this can be done in Interrupt Service Routine (ISR) when it is enabled over NCOx module [25]. The increment value will be stored in two 8-bit registers made as a 16-bit increment value. The upper 8 bits might be stored in NCOxINCH register and lower 8-bits will be stored in NCOxINCL register.

- NCOxINCL
- NCOxINCH

These registers are writeable as well as readable. These increment registers would be double-buffered for allowing to the value changes to be done and no need to disable the NCOx module. if the module is disabled then the buffer loads will be immediate. Writing the values into the NCOxINCH register is essential since the buffer would be synchronously loaded with the operations of NCOx module after the write is performed on NCOxINCL register. The available clock sources to NCOx are:

- HFINTOSC
- CLKIN pin
- LCxOUT
- FOSC

Configure the NxCKS<2:0> bits in NCOxCLK register for NCOx module clock source selection. However, the NCO output has various options which might be set in NCOCON register. The output will enable or disable ((NxOE bit) and even invert (NxPOL bit) while clearing or setting the bits in NCOCON register. In addition, the output is monitored in software by reading the NxOUT bit state in NCOCON register.The output of NCO triggers the internal interrupt if the accumulator is overflowed. This will be handled with 3 bits (NCOxIE, GIE and PEIE). This can allow the NCO for controlling the actions of software via ISR in application code and also result a signal to the I/O pin.GIE referred as Global Interrupt Enable bit, NCOxIE is referred as NCO Interrupt Enable bit. Multiple NCO modules will be there. Here “x” indicates NCO number and PEIE is Peripheral Interrupt Enable bit. The NCOxIF bit is an Interrupt Indicator Flag. In software, this is monitored for observing that interrupt is occurred or not. This is required to be cleared in ISR or in software routine which can read the bit.

3. MEMORY OPTIMIZATION OF HYBRID GDI NUMERICAL CONTROLLED OSCILLATOR

One of the most important parts of digital down conversion is NCO. The NCO is most widely utilized in software radio systems as well as in radar wireless transceiver systems. Here the NCO major function is producing two path sine and cosine data samples with discrete time, variable frequency and mutually orthogonal. The main advantage of NCO is quick response and high frequency precision. The LUT and polynomial expansion are the traditional implementation methods of NCO. The LUT method data accuracy depends on the LUT size of ROM. The memory size and phase accuracy precision are the

exponential relationships that will enlarge the consumption of resources and reduce the system processing speed.

As known that NCO is one of the most utilized digital oscillators that generate signals like clocked, discrete and synchronous waveforms. The NOCs are more often utilized in combinations with the DAC at the outputs for creating DDS. The NCO is utilized in various communication systems that are fully digital or mixed signal such as synthesis of arbitrary waveform, phased array radar and precise control.

Figure 4 shows the schematic ofmemory optimization of hybrid GDI NCO. In this 16 metal-oxide-semiconductor field-effect transistors (MOSFET's) are utilized to design. 2 MOSFET's geometries are utilized. Basically, Total nodes are classified into two types of boundary nodes and independent nodes.1.70 seconds is taken to execute the entire seconds. 0.14 seconds is taken for parsing and 0.03 seconds is taken for setup the design. 12 total nodes are utilized, 5 boundary nodes and 7 independent nodes are utilized. Compared with NCO based 8-bit microchip design, memory optimization of hybrid GDI based NCO gives effective outcome in terms of delay, MOSFET's and nodes. The output waveform is shown in Figure 5.

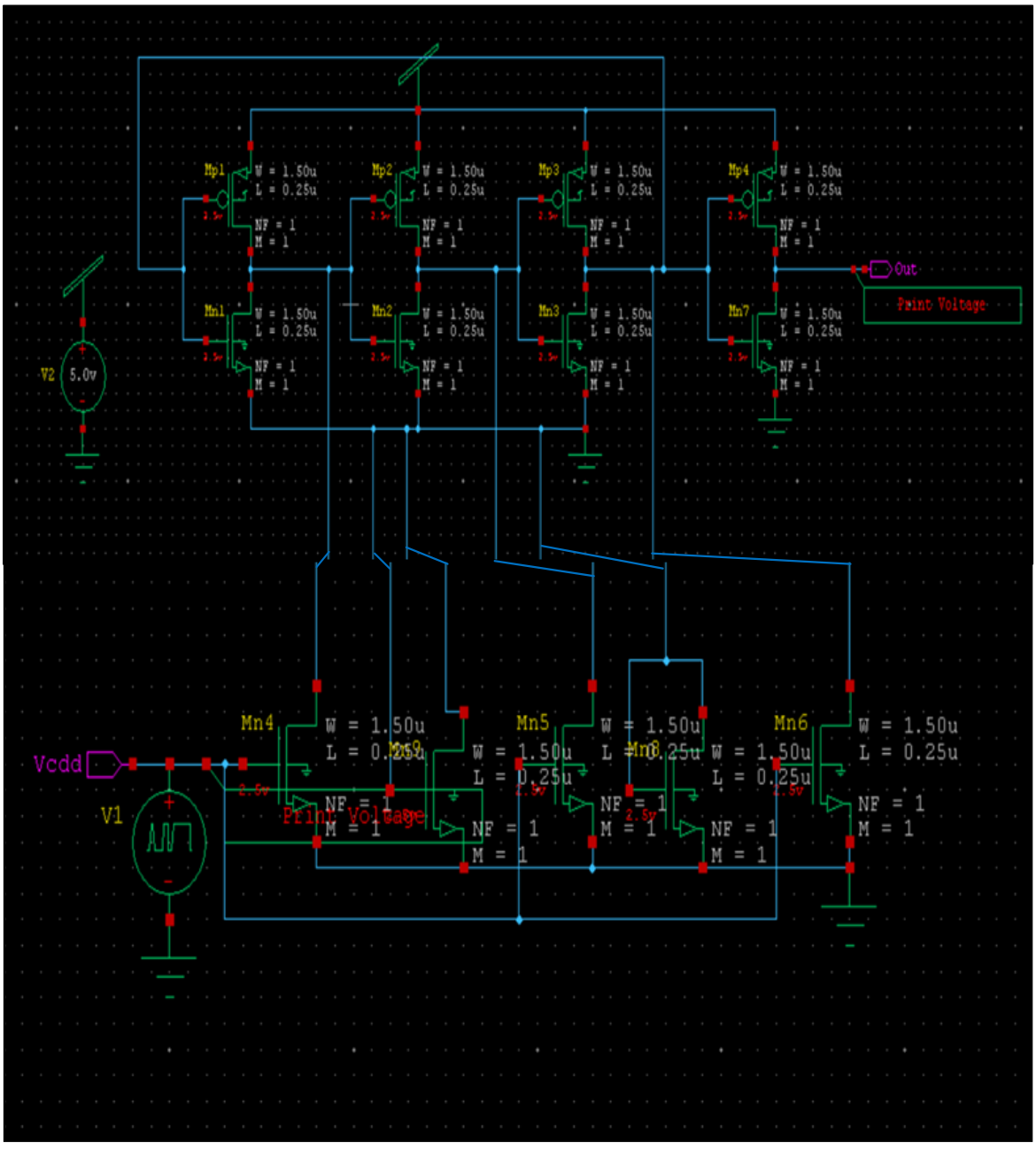

Figure 4. Schematic design

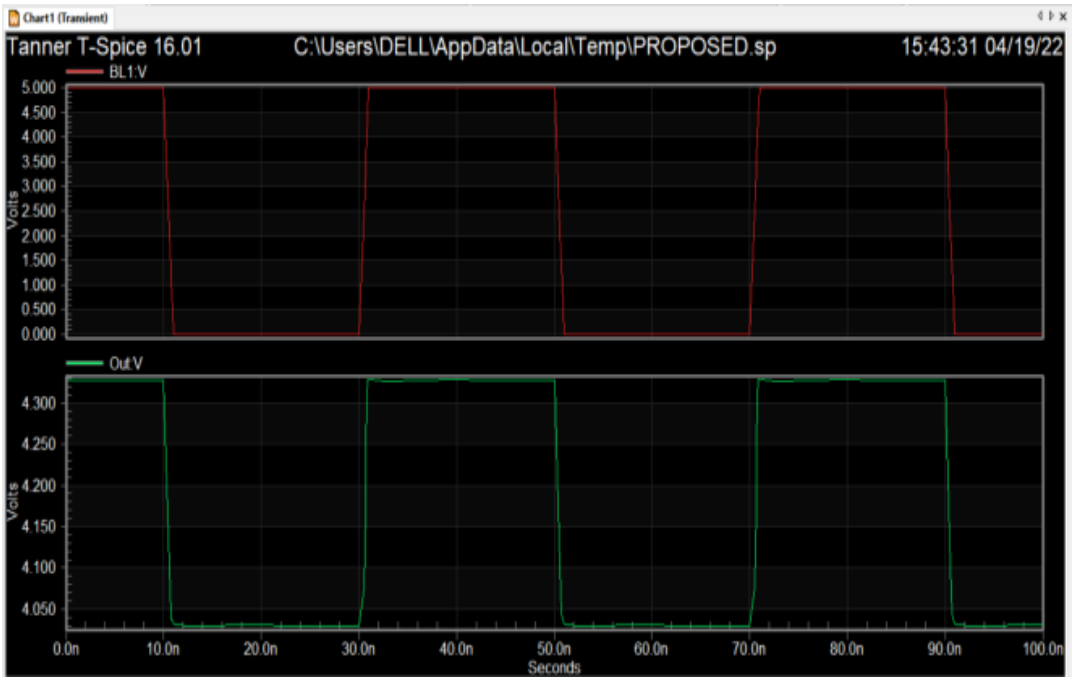

Figure 5. Output waveform

4. RESULTS AND DISCUSSION

Table 1 shows the comparison table. In this 16 MOSFET's are utilized to design. 12 total nodes are utilized, 5 boundary nodes and 7 independent nodes are utilized. 2 MOSFET's geometries are utilized. 1.70 seconds is taken to execute the entire seconds. 0.14 seconds is taken for parsing and 0.03 seconds is taken for setup the design. Figure 6 shows the comparison of nodes for memory optimization of hybrid GDI NCO and NCO based 8-bitmicrochip. Compared with NCO based 8-bitmicrochip, Memory optimization of hybrid GDI NCO uses less number of nodes.

Table 1. Comparison table

S. No	Parameters	NCO based 8-bitmicrochip	Memory optimization of hybrid GDI NCO
1	MOSFET's	32	16
2	MOSFET's geometries	5	2
2	Voltage sources	8	4
3	Total nodes	26	12
4	Boundary nodes	14	5
5	Independent nodes	12	7
6	Total delay	2.51 Seconds	1.70 Seconds
7	Parsing delay	0.43Seconds	0.14 Seconds
8	Setup delay	0.06 Seconds	0.03 Seconds

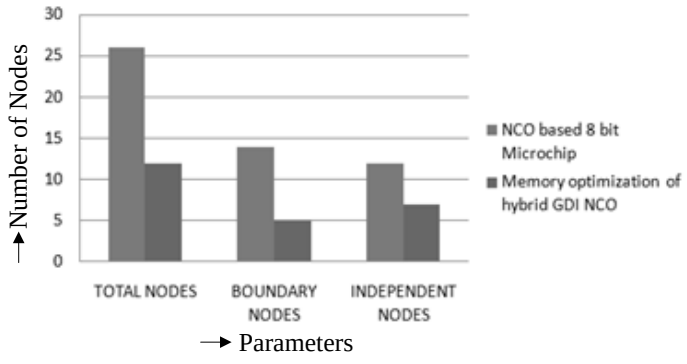

Figure 6. Comparison of nodes

Figure 7 shows the comparison of delay for memory optimization of hybrid GDI NCO and NCO based 8-bitmicrochip. Compared with NCO based 8-bitmicrochip, memory optimization of hybrid GDI NCO produces less delay. Figure 8 shows the comparison of MOSFET's for memory optimization of hybrid GDI NCO and NCO based 8-bitmicrochip. Compared with NCO based 8-bitmicrochip, memory optimization of hybrid GDI NCO uses less MOSFET's.

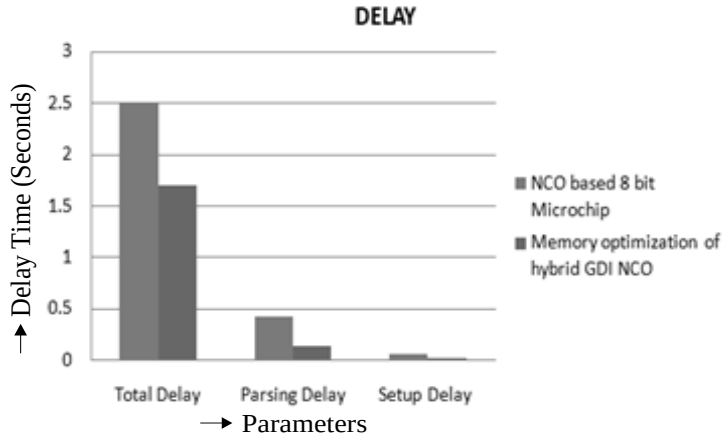

Figure 7. Comparison of delay

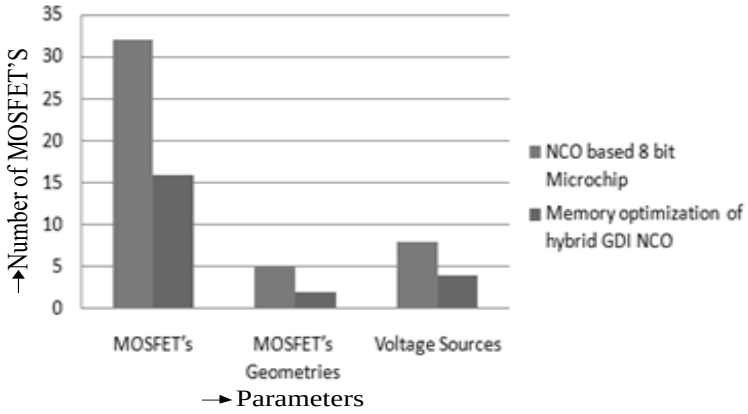

Figure 8. Comparison of MOSFET's

5. CONCLUSION

Hence in this paper design and memory optimization of hybrid GDI numerically controlled oscillator based on FPGA was implemented. compared with NCO based 8-bit microchip, memory optimization of hybrid GDI numerically controlled oscillator based on FPGA gives effective outcome in terms of delay, MOSFET's and Nodes. In this 16 MOSFET's are utilized to design. 2 MOSFET's geometries are utilized. Basically, Total nodes are classified into two types of boundary nodes and independent nodes. 1.70 seconds is taken to execute the entire seconds. 0.14 seconds is taken for parsing and 0.03 seconds is taken for setup the design. 12 total nodes are utilized, 5 boundary nodes and 7 independent nodes are utilized. Compared with NCO based 8-bit microchip design, memory optimization of hybrid GDI based NCO gives effective outcome in terms of delay, MOSFET's and nodes.

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