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Ultra-low leakage static random access memory design

Didigam Anitha, Mohd. Masood Ahmad
Department of Electronics and Communications, Faculty of Engineering, GITAM University, Telangana, India

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ABSTRACT

An ultra-low leakage static random-access memory (SRAM) cell structure with 8 transistors is proposed in this paper. Compared to the 6T SRAM and other existing 8T SRAM cells, leakage power of the proposed cell in hold mode reduced significantly. The stability parameters of the proposed cell are calculated using butterfly method and also N-curve method. Proposed SRAM achieves better write margin with slightly less read margin than 6T SRAM. Proposed technique consumes 790 PW of power in hold mode, which is very less compared to other existing techniques. Therefore, the proposed cell is appropriate for hold mode applications. The simulations are carried out by using Cadence (Virtuoso Schematic and layout editor) tools with GPDK45-nm technology.

Corresponding Author:

Didigam Anitha
Department of Electronics and Communications, Faculty of Engineering, GITAM University
Hyderabad, Telangana, India
Email: adid@gitam.edu

1. INTRODUCTION

Portable electronic gadgets lead to the scaling of devices and more battery life. To decrease the dynamic power dissipation, the supply voltage (VDD) is reduced, which makes the threshold voltage (Vth) is also to decrease. However, sub-threshold power increases due to decreased threshold voltage [1], as it is exponentially dependent on the Vth. Reduction of oxide thickness (t_{ox}) causes gate tunneling current, hot carrier injection and results in increased gate leakage current. In modern IC's leakage power is the major concern, as it is around 40% of total power consumption.

SRAM cell is the one, which consists of cross coupled inverter latch [2], used to store one-bit data. It retains this data until the supply voltage is 'ON'. No continuous refreshing mechanism is required like dynamic RAM (DRAM). SRAM finds applications in cache memory as it provides high-speed operation. These SRAM arrays cause the main sources of leakage currents as many such cells are present in on-chip memory design [3].

A novel design method is discussed in this paper to reduce the leakage power of SRAM cell by adding two extra transistors at the power supply. The proposed circuit also achieves good stability parameters along with the static power reduction. This work is mainly focused on power dissipation in hold mode. Because systems like CC cameras will be kept in standby mode for long time than active mode. Hence reduction of standby power without the stored data degradation is a major concern. The leakage power of a Metal oxide silicon field effect transistor is mainly contributed by sub-threshold leakage, junction leakage and gate leakage currents [4].

When the gate voltage (V_{gs}) of the Metal oxide silicon field effect transistor (MOSFET) is below threshold voltage (V_{th}), sub-threshold leakage occurs. Junction leakage is the leakage due to reverse biased PN junction current of the MOSFET, occurs due to minority carrier drift in the depletion region. It is dependent on the doping concentration and junction area.

$$I_{subthreshold} = I_0 e^{\frac{V_{gs}-V_{th}}{\eta V_T}}\left(1 - e^{\frac{-V_{ds}}{V_T}}\right)$$

where $I_0 = \mu_0 C_{ox} \frac{W}{L}(m-1)(V_T)^2$

Gate leakage current is described by:

$$I_{gate} = WLA\left(\frac{V_{ox}}{t_{ox}}\right)^2 \exp\left(\frac{-B\left(1-\left(1-\frac{V_{ox}}{\varphi_{ox}}\right)^{3/2}\right)}{\frac{V_{ox}}{t_{ox}}}\right)$$

where

$$A = \left(\frac{q^3}{16\pi^2 h \Phi_{ox}}\right), B = \left(\frac{4\pi\sqrt{2m_{ox}}\Phi_{ox}^{\frac{3}{2}}}{3hq}\right)$$

2. ARCHITECTURE

2.1. Basic 6T SRAM architecture

The architecture of 6T SRAM cell, shown in Figure 1. It is comprised of two inverter pairs (P0-N0 is one inverter and P1-N1 is another). These inverters are connected in the form of loop to store one bit information [2]. Outputs are available at 'Q' and 'QB' nodes, which are complement to each other. Two pass transistors N2 and N3 are connected at the output of inverters to access the data present on 'Q' and 'QB'. Source terminal of these transistors are connected to bit-line (BL) and bit-line bar (BLB).

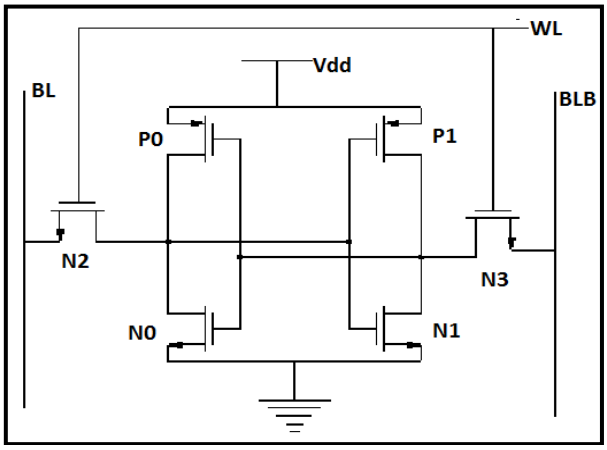

Figure 1. Circuit diagram of 6T SRAM cell

2.2. Operation of SRAM cell

In read mode, word line (WL)='1' and bit lines BL and BLB are kept at Vdd. In this mode, the contents stored in the SRAM cell will be read. To achieve better stability cell ratio ≥1.2 shall be maintained. During write mode, the contents of SRAM cell will be updated. For example, to write '1' into the SRAM cell, WL must be assumed as '1' and BL= '0' & BLB= '1'. To achieve better write stability, pull-up ratio must be maintained. In hold mode operation, since WL=0, N2 and N3 are detached from the inverter latch, and the inverter pair holds the value.

2.3. NC- SRAM cell

The architecture of NC-SRAM proposed in [6] is shown in Figure 2, uses the concept of dynamic voltage scaling (DVS). For the basic 6T SRAM cell, two NMOS transistors N4 and N5 are added as shown in figure. N4 and N5 transistors offer different grounds in read/write mode and hold mode. The source of NMOS transistors is connected to Vs (which is higher potential than VSS) in hold mode and connected to Vss in active mode. The concept of positive ground voltage reduces the leakage power considerably.

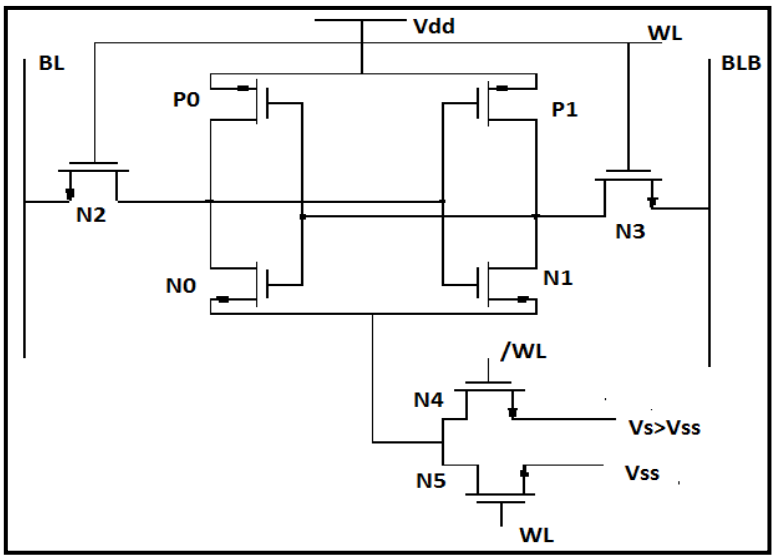

Figure 2. Circuit diagram NC SRAM Cell

2.4. 8T SRAM cell

An SRAM cell, with 8 transistors proposed in is shown in Figure 3. The architecture of this cell is same as that of NC SRAM cell, except header cells [7], [8]. The Header cell uses different VDD levels. The hold mode power dissipation is reduced significantly in this cell compared to conventional 6T SRAM and N-controlled SRAM cells. However, this 8T SRAM cell suffers to maintain the data in the hold mode.

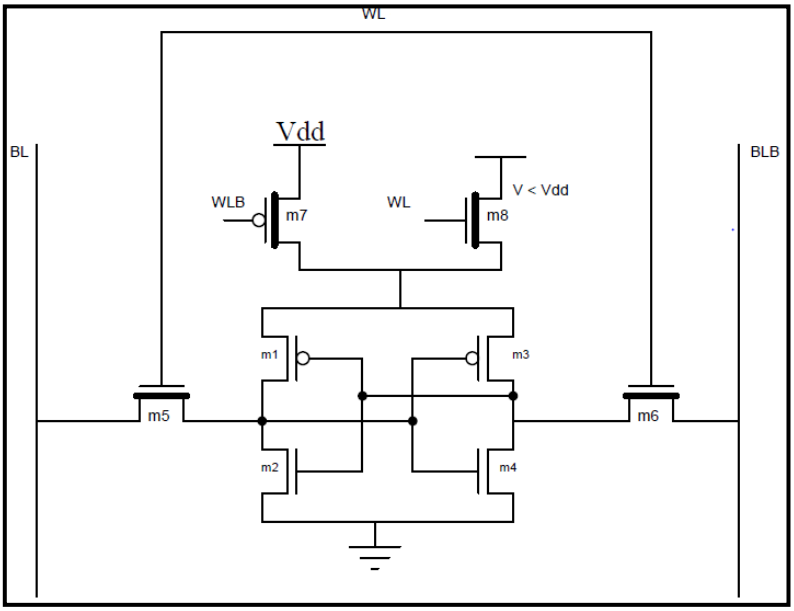

Figure 3. Circuit diagram of 8T SRAM Cell

3. PROPOSED 8T SRAM CELL

3.1. Cell Architecture

The proposed cell is slightly modified from that of 8T SRAM cell and is shown in Figure 4. In the 8T SRAM cell, transistor M8 is controlled by WL whereas in the proposed cell, M8 is controlled by WLB. For hold mode operation, WL=0 and WLB=1 makes the inverter latch to connect to reduced VDD through M8 transistor. Here M7 is a PMOS transistor is connected to VDD and M8 is a NMOS transistor connected

to reduced voltage, V<VDD. Both M7 and M8 transistors are controlled by WLB. Here, M7, M8 are high threshold (Vt) cells, to reduce the leakage power. Further, M5 and M6 also high threshold cells, used for leakage reduction in bit lines.

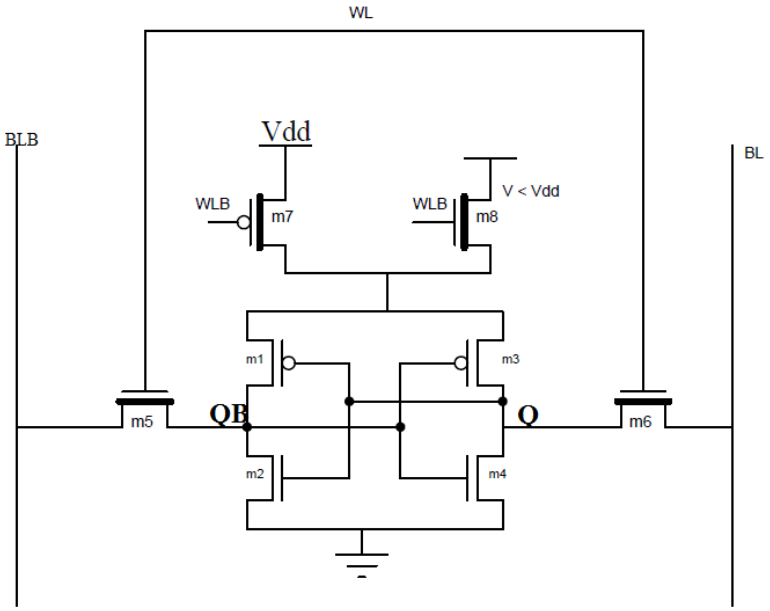

Figure 4. Proposed 8T SRAM cell circuit

3.2. Operation

3.2.1. Hold mode

In this mode, WL remains low and WLB is high. The transistors M5 and M6 remain turned off. The inverter pair is connected to the reduced supply voltage (V<Vdd) through M8, as M8 is a NMOS and is connected to WLB. Thus, the data stored in the inverter latch is maintained during this mode. Huge reduction in the power dissipation is possible with this circuit as the inverter latch is at reduced supply voltage.

3.2.2. Read mode

Bit lines (BL and BLB) are prechraged to supply voltage (VDD) [9],[10] in this mode. WL is maintained high during this mode. Read stability is obtained by proper sizing of transistors. The operation of the SRAM in read mode is as follows. Assume, '1' is being stored at node Q, '0' at node QB, then BLB discharges to ground through M5 and M2 transistors. The sense amplifiers connected surrounding the SRAM cells, detect this decrease in the voltage present at BLB and reads it as '0'.

3.2.3. Write mode

To update the contents in the SRAM cell, write mode is used. To write '0' at node 'Q', WL must be assumed as '1' and BL= '0' & BLB= '1' shall be taken. Then the values at node 'Q' and 'QB' will be written as '0' and '1' respectively.

4. RESULTS AND DISCUSSION

4.1. Power analysis

At 45 nm technology node, leakage current equations are given by (1), (2) and (3). The leakage analysis can be explained as follows. Say, '1' is stored at node 'Q' nd '0' at 'QB' and the cell is in standby mode. In this case, transistors M1, M4 and M5 [11] contributes the subthreshold leakage as described in (1). As shown in (2) and (3) describes Junction leakage & gate leakage currents. In the proposed cell, V is usually less voltage than supply voltage (Vdd). Due to this, power dissipation the proposed cell is reduced. Transistors M5, M6, M7 &M8 are high threshold cells, thus ensures further reduction in leakage currents.

Though 8T SRAM cell [6] is operating on the same principle, it is unable to retain the data in hold mode. The simulation waveforms are shown in Figure 5. From these waveforms it can be observed that, the data in the hold mode is retained by providing larger leakage reduction.

$$I_{sub=}I_{subM5} + I_{subM4} + I_{subM1} \quad (1)$$

$$I_{JN} = I_{JNdM6} + I_{JNsM6} + I_{JNdM5} + I_{JNdM4} + I_{JNdM1} \quad (2)$$

$$I_g = I_{gdM6} + I_{gsM6} + I_{gdM5} + I_{gdM1} + I_{gdM2} + I_{gsM2} + I_{gdM3} + I_{gsM3} + I_{gdM2} \quad (3)$$

And total leakage is $I_{leak} = I_{sub} + I_{JN} + I_g$

Hold mode power dissipation of 6T SRAM and proposed SRAM cells is shown in Figures 6 and 7 tabulated in Table 1.

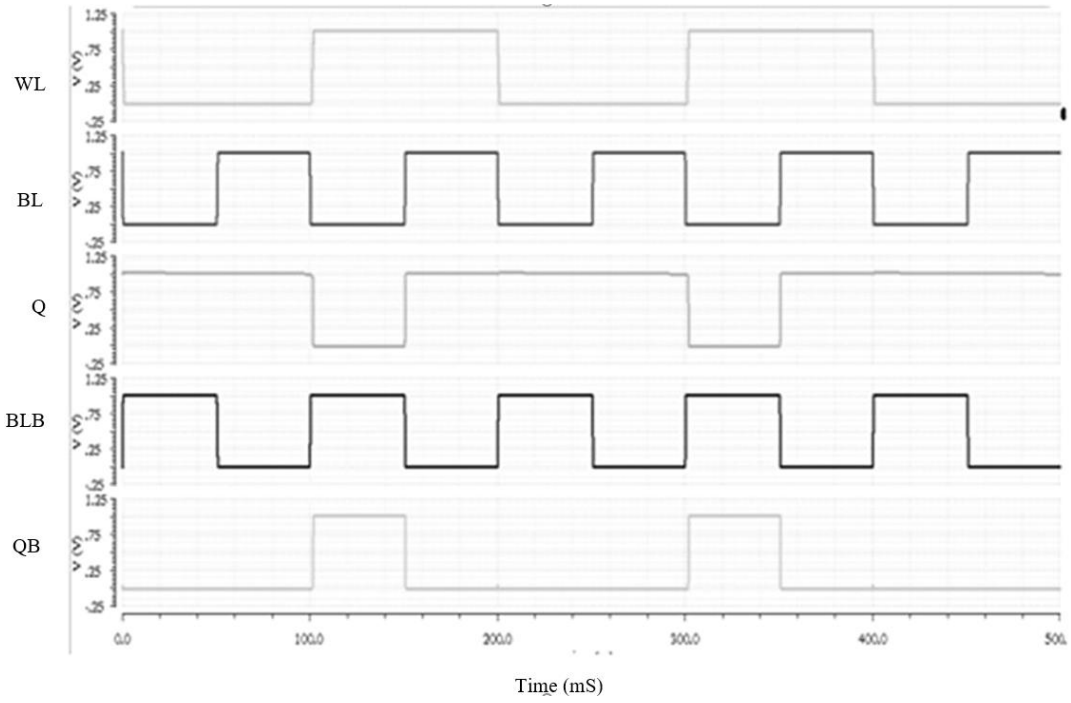

Figure 5. Simulation waveforms of the proposed SRAM cell

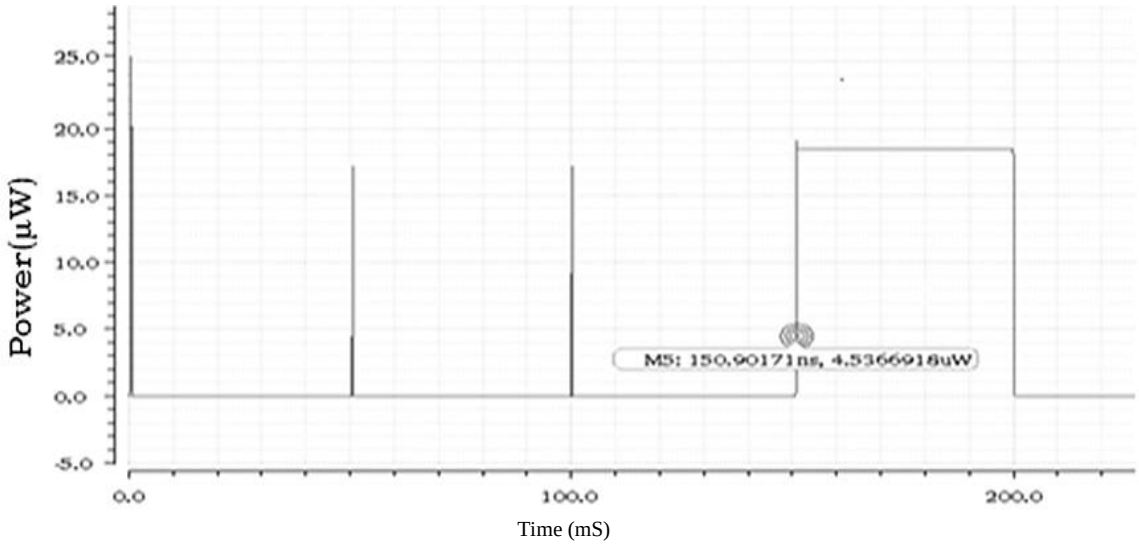

Figure 6. Hold mode Power dissipation of basic SRAM cell

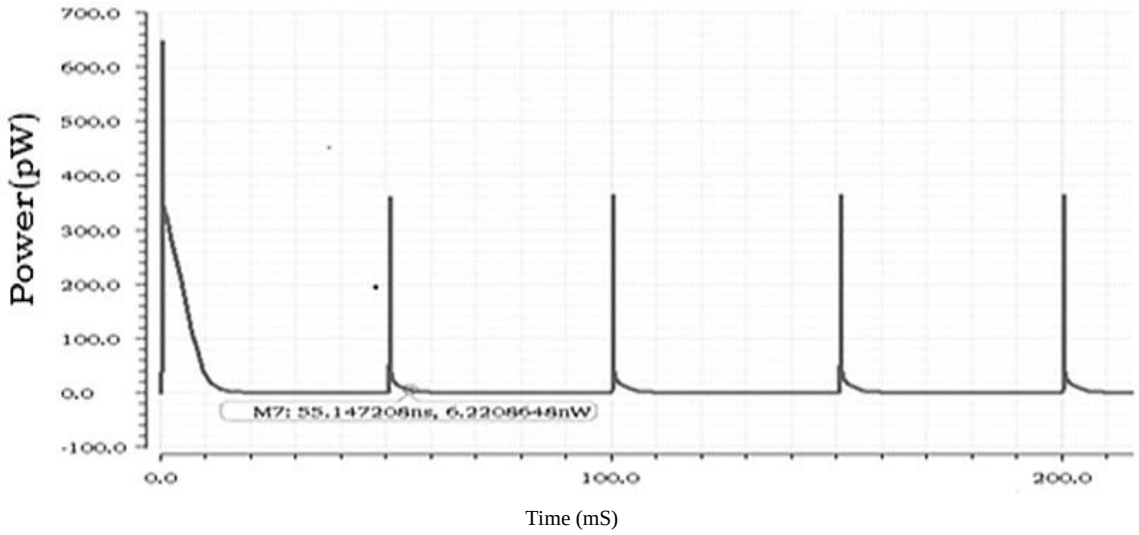

Figure 7. Hold mode power dissipaion proposed SRAM cell

Table 1. Power dissipation comparison

Parameter	6T SRAM	8T SRAM	Proposed SRAM
Static power (W)	4.2µ	6.22n	795p
Total power (W)	4.5 µ	3.4 µ	243n

4.2. Stability analysis

SRAM cell stability is described by static noise margin (SNM). This performance metric parameter of the SRAM [12]-[14] is classified into 3 types: i) read SNM: it is the SNM in read mode; ii) hold SNM: it is the SNM in hold mode; iii) write SNM: SNM in write mode.

To measure the SNM in butterfly method, inverter pair transfer characteristics are plotted, and the best fit square is drawn between these characteristic curves. In this method, two different circuits are required to obtain the read SNM and write SNM. In N-curve method [15]-[18], SNM in both read and write modes can be obtained at a time. Butterfly curves of basic 6T SRAM cell and proposed SRAM cell are depicted in Figures 8 and 9 respectively. N-curves of both cells are shown in Figures 10 and 11. Performance parameters obtained in both methods are tabulated in Tables 2 and 3.

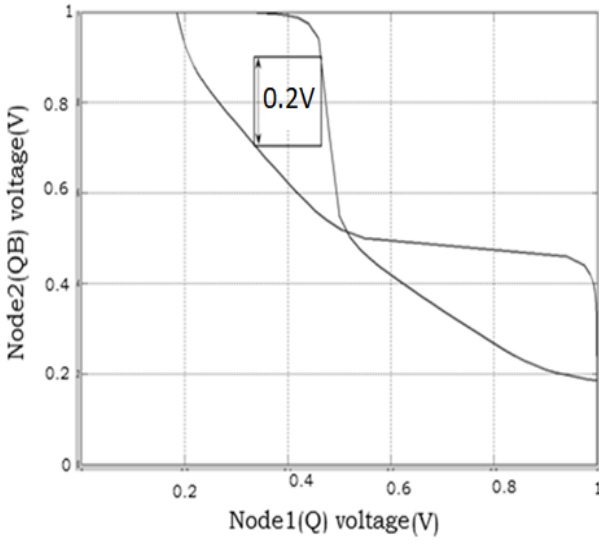

Figure 8. Read mode SNM of basic SRAM cell

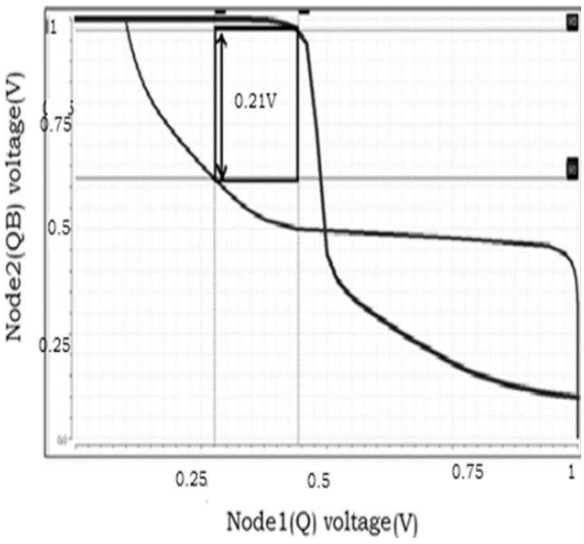

Figure 9. Read SNM of proposed SRAM cell

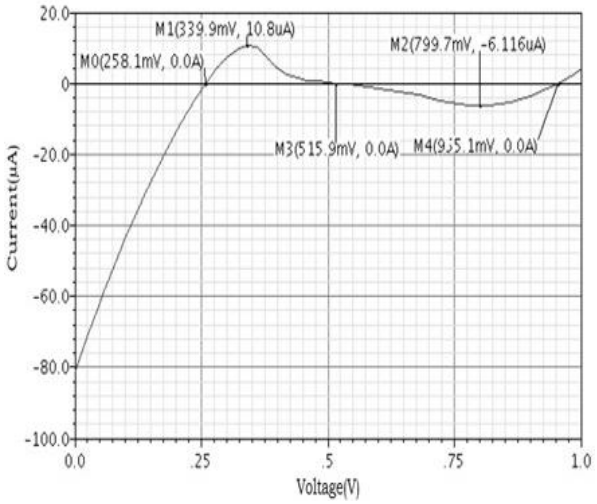

Figure 10. N-curve of 6T SRAM cell

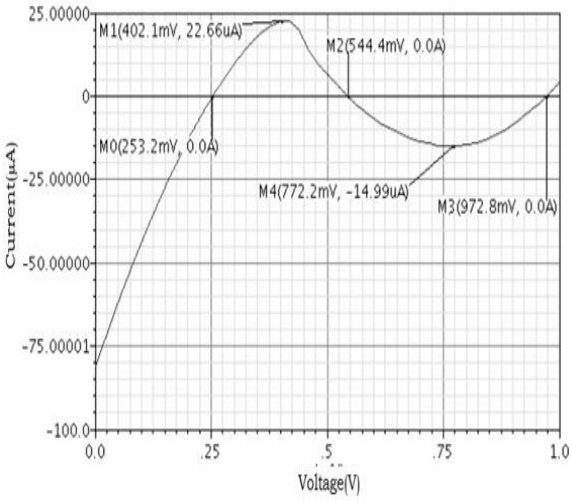

Figure 11. N-curve of proposed SRAM cell

Table 2. SNM from butterfly method

Parameter	6T SRAM	Proposed SRAM
SNM(V)	0.2	0.21
SNM @ process corners(V)	0.22	0.21

Table 3. Stability parameters from N-Curve method

Parameter	Basic 6T SRAM	Proposed SRAM
SVNM (mV)	258	293
SINM (µA)	11	23
WTV (mV)	420	429
WTI(µA)	-6.1	-15

4.3. Statistical analysis

Statistical analysis is the advanced analysis in cadence and is used to measure parametric variations and circuit robustness [19]-[22]. By initiating 10% variations in threshold voltage (Vth) along with 10% variations in oxide thickness (Tox) statistical analysis is performed for 100 runs. These results are given in Figures 12 and 13.

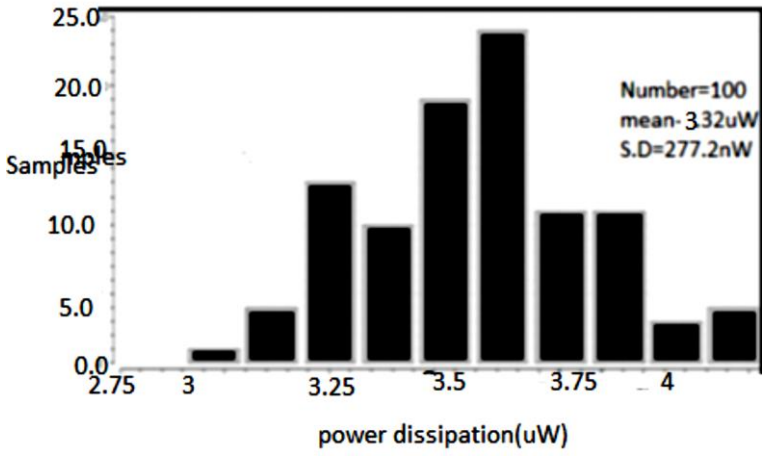

Figure 12. Histogram of hold mode power dissipation of basic 6T cell

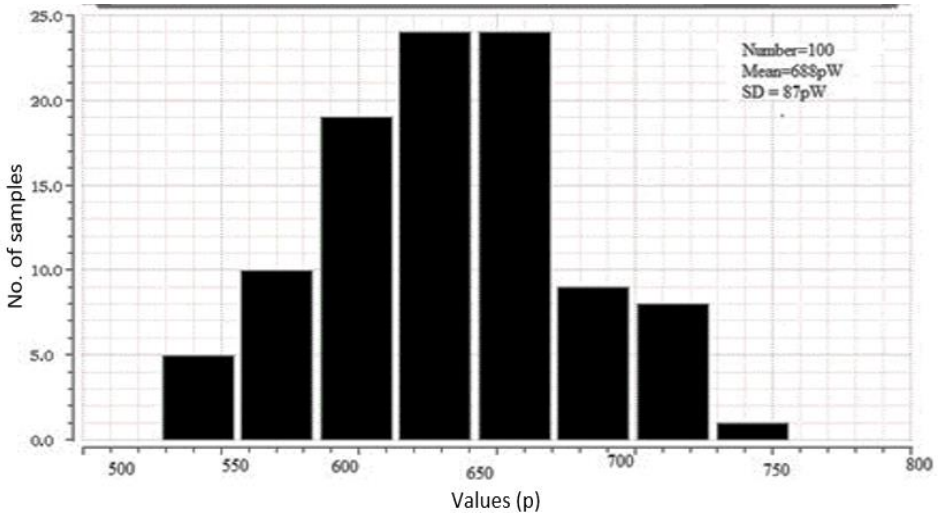

Figure 13. Histogram of hold mode power dissipation of proposed SRAM cell

4.4. Area analysis

The layouts [23]-[25] for the basic 6T SRAM cell and our proposed SRAM cell are drawn and shown in Figure 14 and Figure 15. The key observations are, proposed SRAM takes 13% more area than 6T SRAM as it consists of extra two transistors at power supply. Comparison of all performance parameters of proposed SRAM cell with other similar existing SRAM cells is given in Table 4.

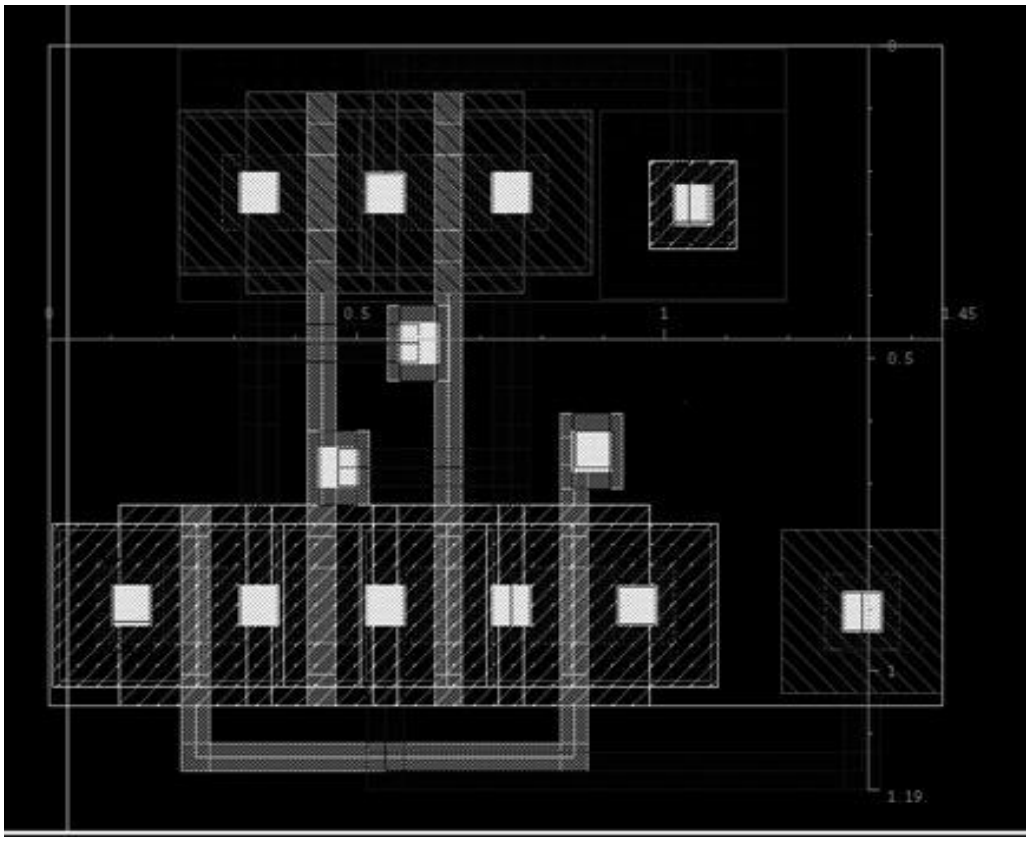

Figure 14. Layout of basic 6T SRAM cell

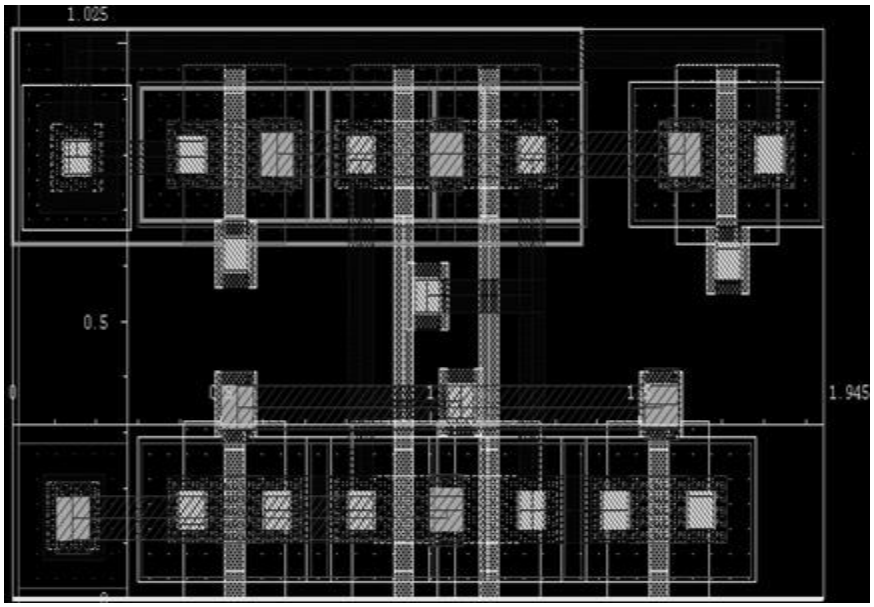

Figure 15. Layout of proposed SRAM cell

Table 4. Comparison of performance parameters of SRAM

Parameters	6T SRAM	NC-SRAM	8T SRAM	Proposed SRAM
Static power (W)	4.23 µ	262 n	3.26 µ	6.22 n
Total power (W)	4.57 µ	2.3µ	3.49 µ	3.40 µ
Static Noise Margin (V)	0.21	0.15	0.15	0.21
Delay (Sec.)	170p	213p	183p	144p
Static power delay product (W-Sec)	8.143×10^{-16}	55860×10^{-21}	596.6×10^{-16}	895.7×10^{-21}
Total Power delay product (W-Sec)	8.797×10^{-16}	4.89×10^{-16}	6.39×10^{-16}	4.89×10^{-16}

5. CONCLUSION

Design of SRAM cell with ultra-low leakage power is presented in this paper. The simulations are carried out using GPDK 45 nm CMOS technology transistors in cadence. This SRAM with 8 Transistors achieves very less leakage power compared to other existing techniques. Not only leakage power, total power dissipation of the proposed SRAM is also reduced significantly. Stability analysis is performed and the SNM is calculated by using both N-curve and butterfly methods. Proposed cell is more suitable for hold mode applications as its power dissipation in hold mode is only 790 pW. But the drawback with this proposed SRAM is, it shows 13% more area overhead than the 6T SRAM cell.

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BIOGRAPHIES OF AUTHORS

Didigam Anitha received her B.Tech degree in Electronics and Communication Engineering and her M.Tech in VLSI and Ph.D. in Low power VLSI at JNTU Hyderabad. She is working as Asst.prof. in GITAM University, Hyderabad. Her research includes VLSI, Mixed signal design and low power VLSI. She can be contacted at email: adid@gitam.edu.

Mohd. Masood Ahmad received his B. E degree in Electronics and Communication Engineering and M. Tech in VLSI and Ph.D. in Low power VLSI at JNTU Hyderabad. He is working as Asst. prof. in GITAM University, Hyderabad. His research includes VLSI, Digital design and Low power VLSI. He can be contacted at email: mmahamma@gitam.edu.