International Journal of Reconfigurable and Embedded Systems (IJRES)
Vol. 15, No. 12, July 2026, pp. 320~338
ISSN: 2089-4864, DOI: 10.11591/ijres.v15.i2.pp320-338

A review of field-programmable gate array-based biomedical signal processing for public health applications

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Article Info

Article history:

Received Oct 17, 2025
Revised May 13, 2026
Accepted Jun 12, 2026

Keywords:

Biomedical signal processing
Electroencephalography
Electromyography
Field-programmable gate arrays
Mobile health
Public health applications
Telemedicine

ABSTRACT

Biomedical signal processing is essential for modern diagnostics, monitoring, and preventive healthcare in public health and mobile health (mHealth) systems. Signals such as electroencephalography (EEG), electromyography (EMG), and heart rate variability (HRV) offer vital insights into brain, muscle, and cardiovascular health. However, achieving real-time, energy-efficient, and scalable processing remains challenging for conventional hardware such as central-processing units (CPUs), graphics-processing units (GPUs), and application-specific integrated circuits (ASICs). Field-programmable gate arrays (FPGAs) provide a promising alternative through their reconfigurability, parallelism, and adaptability to dynamic biomedical workloads. This review examines FPGA-based implementations for EEG, EMG, and HRV processing, focusing on key metrics including latency, throughput, and power efficiency. It also discusses design strategies such as low-power optimization, hardware–software co-design, and FPGA-based machine learning acceleration, with attention to data integrity and security in medical contexts. Integration with wearable, portable, and telemedicine platforms is explored, alongside comparative analyses with traditional computing architectures. The paper identifies challenges in power–performance trade-offs, design complexity, and clinical validation, and highlights emerging directions such as artificial intelligence (AI)-driven FPGA platforms, neuromorphic design, and sustainable low-cost solutions for large-scale health monitoring. Overall, FPGA-based biomedical signal processing emerges as a foundation for intelligent, efficient, and accessible next-generation public-health technologies.

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1. INTRODUCTION

Biomedical signal processing forms the technological foundation for modern healthcare analytics, enabling continuous monitoring, diagnosis, and prevention across diverse physiological domains [1]–[3]. Signals such as electroencephalography (EEG), electromyography (EMG), and heart-rate variability (HRV) provide critical insights into neurological, muscular, and cardiovascular functions, respectively [4], [5]. Their integration into public health and mobile-health (mHealth) systems supports early detection of disease, long-term management of chronic conditions, and population-level surveillance [6], [7]. However, processing these complex, high-dimensional biosignals in real time remains a major challenge for conventional

computing architectures. Central-processing units (CPUs) and graphics-processing units (GPUs) offer general-purpose flexibility but often suffer from high latency and power consumption, while application-specific integrated circuits (ASICs) lack the adaptability required for evolving biomedical workloads [4], [8], [9].

Field-programmable gate arrays (FPGAs) have emerged as a compelling alternative, offering customizable parallel architectures that can be dynamically reconfigured to meet varying computational demands [1], [6], [7]. Their ability to deliver high throughput and deterministic latency with low energy cost makes them particularly attractive for embedded and wearable health platforms operating in resource-constrained environments [5], [8]. Figure 1 illustrates the conceptual framework of FPGA-based biomedical signal processing for public health applications, highlighting how reconfigurable architectures enable real-time, energy-efficient analysis across multiple physiological domains. Recent advances in FPGA technology—such as hardware–software co-design, dynamic partial reconfiguration (DPR), and integration of lightweight artificial intelligence (AI) accelerators—have further enhanced their applicability to biomedical signal processing, from real-time seizure detection and muscle-activity classification to continuous cardiovascular monitoring [3], [7], [9].

This review provides a comprehensive synthesis of FPGA-based implementations for processing key biomedical signals (EEG, EMG, and HRV) in public-health and mHealth contexts [1], [2], [6], [7]. It analyzes architectural strategies, performance metrics, and energy-efficiency techniques that underpin next-generation health-monitoring systems [5], [8]. Beyond comparing FPGA platforms with traditional CPUs and GPUs, the paper explores cross-cutting issues such as design complexity, security, and clinical validation [3], [9]. By bridging hardware-level innovations with translational healthcare outcomes, this review highlights how reconfigurable computing can drive the development of intelligent, secure, and sustainable health technologies [1], [5], [7]. The overarching aim is to identify both the current state of FPGA-based biomedical signal processing and the future directions required to realize its full potential in scalable public-health infrastructures [2], [3].

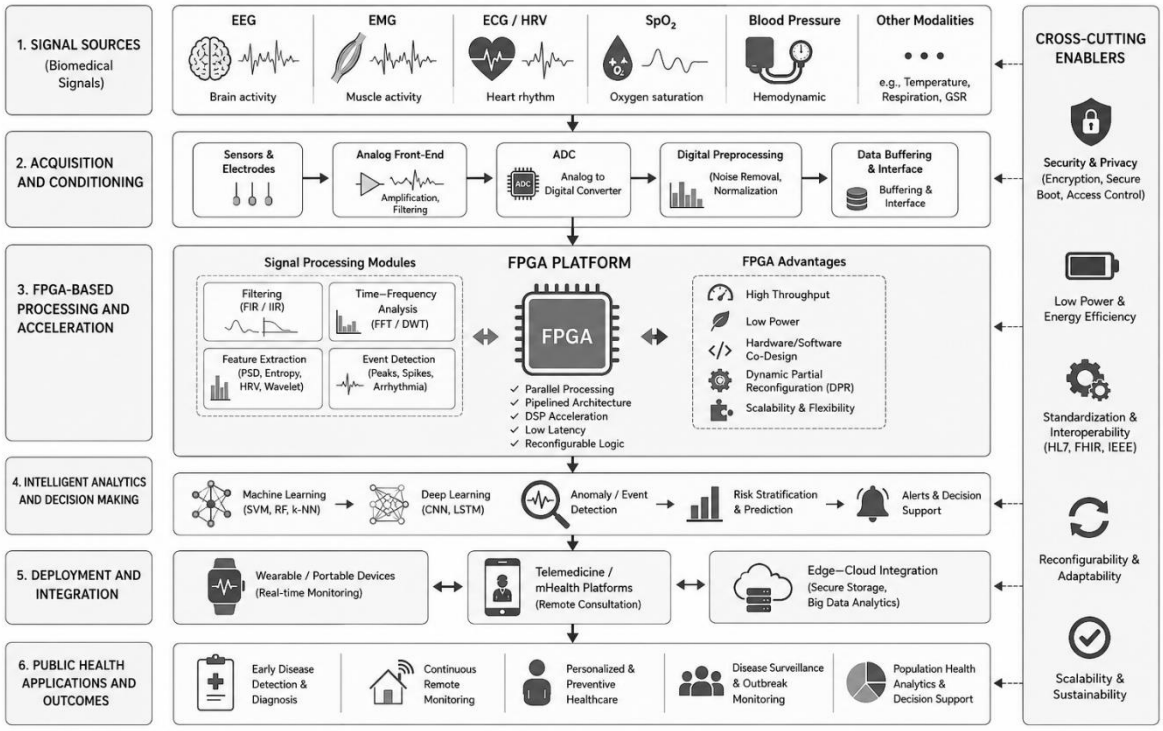

Figure 1. Conceptual framework of FPGA-based biomedical signal processing for public health applications

2. BIOMEDICAL SIGNALS IN PUBLIC HEALTH

The growing integration of biomedical signal processing within public-health frameworks has transformed how physiological data are acquired, analyzed, and applied to preventive and diagnostic care [2], [3], [6]. Biomedical signals capture continuous physiological variations that can reveal both individual health states and broader population-level trends [5], [10]. Among these, EEG, EMG, and HRV are particularly

significant because they provide non-invasive, quantifiable indicators of neurological, muscular, and cardiovascular health [4], [11]. As illustrated in Figure 2, these biomedical signals form the foundation of data-driven public-health systems, linking individual physiological monitoring to community-level health analytics. The effective utilization of these signals in mobile and remote environments is central to advancing personalized medicine, community health monitoring, and large-scale epidemiological studies [7], [9].

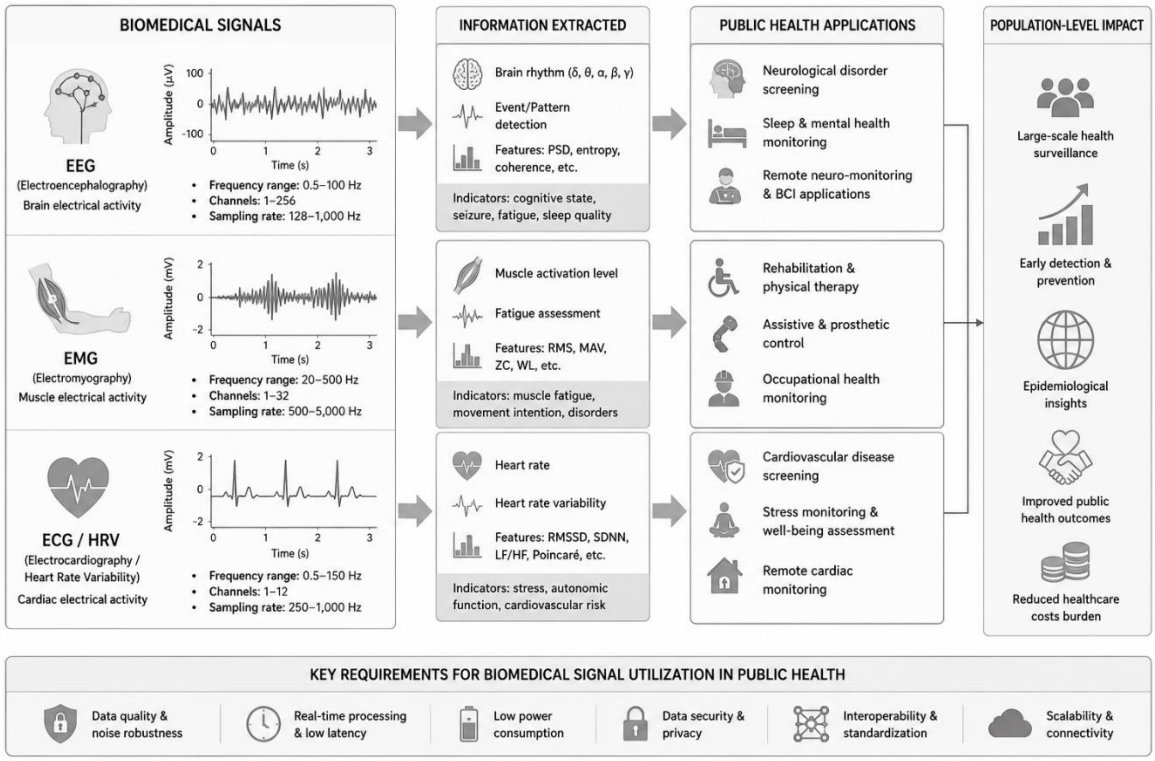

Figure 2. Biomedical signals in public-health

2.1. Electroencephalography

EEG measures brain electrical activity through scalp electrodes and has long been used for diagnosing neurological disorders such as epilepsy, sleep disturbances, and cognitive impairments [10]. In recent years, EEG processing has extended to mental-health monitoring, fatigue detection, and brain computer interfaces (BCIs) [12]. However, EEG signals are typically low-amplitude and highly susceptible to noise and artifacts, necessitating advanced filtering, feature-extraction, and classification techniques that demand substantial computational resources [10], [12]. The ability to process EEG data in real time is crucial for closed-loop neuro-monitoring systems and responsive BCIs—requirements that align well with FPGA based architectures capable of parallelized, low-latency signal handling [6], [7].

2.2. Electromyography

EMG captures electrical activity produced by skeletal muscles and provides valuable information for assessing neuromuscular disorders, prosthetic control, and rehabilitation therapies [6], [13]. Wearable EMG systems are increasingly used to monitor muscle fatigue, detect abnormal motion patterns, and support tele-rehabilitation programs [13]. These applications require high-throughput feature extraction (e.g., root-mean-square, zero-crossing (ZC), or wavelet features), and real-time classification for responsive feedback [13], [14]. FPGAs enable efficient hardware implementation of these computationally intensive algorithms while maintaining low power consumption—critical for battery-powered wearable devices used in long-term monitoring or assistive technologies [6], [15].

2.3. Heart-rate variability

HRV, derived from electrocardiogram (ECG) signals, reflects autonomic nervous-system balance and serves as a powerful biomarker for cardiovascular health, stress evaluation, and overall physiological

resilience [5], [11]. Public-health studies increasingly employ HRV to evaluate population stress levels, occupational well-being, and chronic-disease risk [11], [16]. Accurate HRV analysis requires precise detection of R-peaks and robust computation of time- and frequency-domain features, tasks that can strain embedded processors when implemented continuously in portable devices [5], [15]. FPGA-based systems provide deterministic timing and concurrent processing pipelines that enhance HRV computation accuracy and responsiveness, supporting large-scale, real-time monitoring initiatives [5]–[7].

2.4. Biomedical signal requirements for public-health systems

From a systems perspective, biomedical signal processing for public-health applications must satisfy stringent requirements; i) scalability—supporting numerous concurrent devices and users [3], [8], ii) energy efficiency—minimizing power usage for long-term operation [5], iii) low latency—enabling immediate feedback for clinical or behavioral interventions [7], [9], and iv) data integrity and security—protecting sensitive health information during acquisition and transmission [17], [18]. Meeting these requirements at the edge demands reconfigurable and adaptive hardware platforms. FPGAs, through their capacity for parallel execution and on-the-fly reconfiguration, present a viable solution that bridges individual patient monitoring with population-scale public-health analytics [6]–[8].

3. RECONFIGURABLE HARDWARE ARCHITECTURES FOR BIOMEDICAL SIGNAL PROCESSING

The growing complexity of biomedical data and the demand for real-time analysis have made hardware reconfigurability a central feature of next-generation health-monitoring systems [7], [8]. Conventional processors—although flexible—are often constrained by serial execution and high energy demands, limiting their applicability in continuous or mobile health (mHealth) environments [19], [20]. In contrast, reconfigurable computing platforms such as FPGAs, coarse-grained reconfigurable arrays (CGRAs), and heterogeneous system-on-chips (SoCs) offer the ability to tailor hardware to specific signal-processing tasks while maintaining adaptability to evolving algorithms [5], [21]. These properties make them ideal for biomedical applications, where workloads vary across acquisition, filtering, feature extraction, and classification stages [7], [8], [20]. As illustrated in Figure 3, these reconfigurable hardware architectures form a layered framework for biomedical signal processing, enabling adaptive computation pipelines optimized for real-time, and low-power healthcare applications.

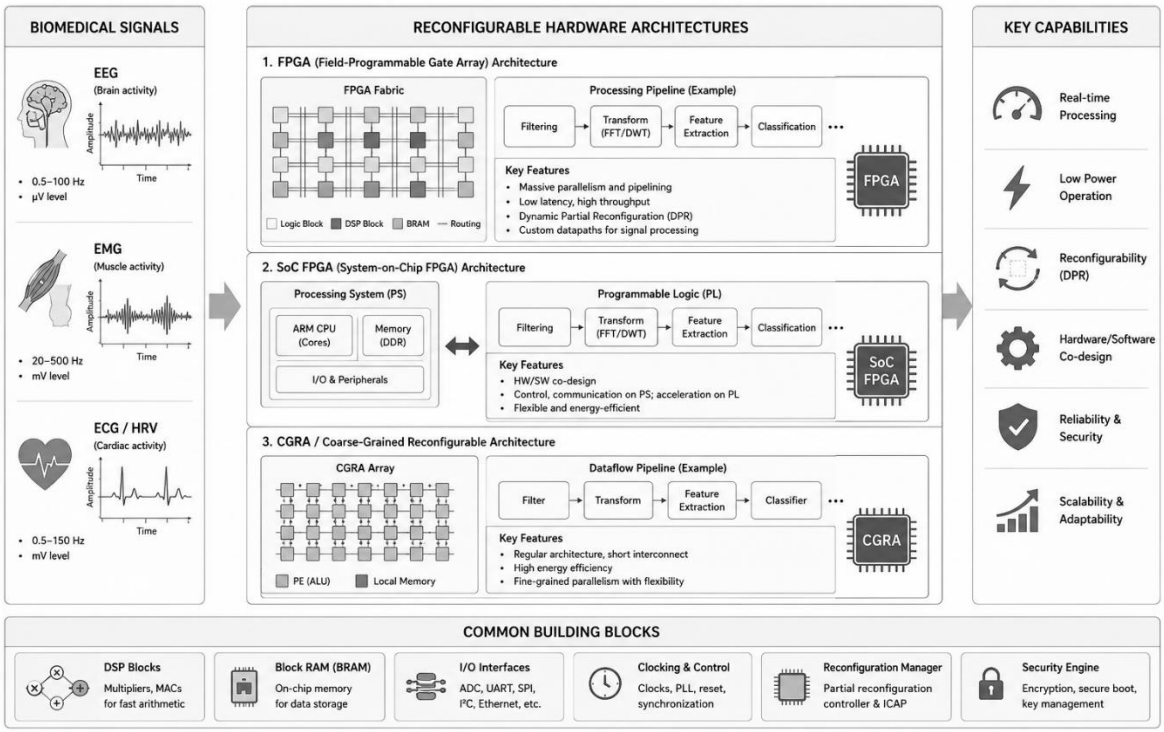

Figure 3. Reconfigurable hardware architectures for biomedical signal processing

3.1. Field-programmable gate array and system-on-chip fundamentals

An FPGA consists of an array of configurable logic blocks, programmable interconnects, and embedded resources such as digital-signal-processing (DSP) slices, block random access memories (Block RAMs), and hardware multipliers [5], [19]. Unlike fixed-function ASICs, FPGAs can be reprogrammed post-fabrication to implement different architectures or adapt to new signal-processing pipelines [8], [21]. Their inherent parallelism allows simultaneous execution of multiple processing stages—critical for handling high-frequency biosignals such as EEG and EMG—while deterministic timing ensures consistent latency, a requirement in safety-critical medical systems [19], [20].

Modern SoC-based FPGAs integrate general-purpose processing cores (e.g., ARM Cortex-A series) with reconfigurable logic fabric, creating a hybrid platform that merges software flexibility with hardware acceleration [5], [16], [21]. This architecture enables the partitioning of biomedical workloads: computationally intensive operations (e.g., wavelet transforms and filtering) are offloaded to the FPGA fabric, while control, communication, and user-interface tasks remain in the embedded processor domain [20], [21]. Such hardware–software integration provides a balanced approach for resource-constrained health devices requiring both adaptability and low-power operation [7], [16].

3.2. Field-programmable gate array design workflow for biomedical systems

The development of FPGA-based biomedical signal processors typically follows a multi-stage workflow encompassing algorithm modeling, hardware mapping, and verification [20], [21]. Initially, algorithms for signal acquisition and feature extraction are modeled in high-level languages such as MATLAB or Python. These models are then translated into hardware descriptions using hardware description languages (HDLs) like very high speed integrated circuit hardware description language (VHDL) or Verilog, or through high-level synthesis (HLS) tools that generate optimized register-transfer-level designs from C/C++ code [16], [20]. HLS frameworks significantly reduce development time, allowing biomedical engineers with limited hardware experience to design efficient FPGA accelerators [20], [21].

The verification stage involves functional simulation and hardware-in-the-loop testing to ensure reliability and accuracy—essential attributes for medical applications subject to regulatory scrutiny [19], [20]. Increasingly, design workflows incorporate hardware–software co-simulation, enabling iterative optimization between algorithmic performance and hardware constraints such as power consumption, logic utilization, and timing closure [20], [21]. Once validated, FPGA configurations can be deployed on portable health-monitoring platforms or integrated into internet-of-medical-things (IoMT) ecosystems for real-time data processing [16], [22].

3.3. Adaptability and runtime reconfiguration

A defining feature of FPGAs is their ability to support DPR—the modification of specific hardware regions during operation without interrupting the rest of the system [8], [19]. In biomedical contexts, DPR enables adaptive signal-processing pipelines that can switch algorithms on demand; for instance, transitioning from noise filtering to feature extraction as data conditions change [5], [20]. This runtime flexibility allows wearable or implantable devices to maintain performance while minimizing energy consumption, as only active modules consume power [7], [8]. Moreover, it extends the device's lifespan by allowing remote updates of diagnostic algorithms without hardware replacement—a crucial advantage in large-scale telemedicine deployments [16], [22].

3.4. Advantages for biomedical applications

Compared with CPUs and GPUs, FPGA-based architectures offer a superior combination of low latency, deterministic response, and energy efficiency [7], [19]. Their reconfigurability facilitates rapid adaptation to new biosignal models or AI-based classifiers, ensuring long-term scalability for healthcare technologies [20], [21]. Furthermore, their parallel pipeline structure aligns naturally with the multi-stage nature of biomedical signal processing—acquisition, filtering, feature extraction, and classification—allowing concurrent operation with minimal delay [7], [8], [20]. When integrated into SoC environments, FPGAs can achieve real-time data throughput within tight energy budgets, making them particularly suitable for continuous, wearable, or battery-powered health-monitoring systems [5], [16], [22].

In summary, reconfigurable architectures bridge the performance–flexibility gap between conventional processors and fixed-function accelerators, offering a customizable foundation for biomedical signal processing [7], [8], [21]. As the subsequent sections demonstrate, FPGA-based designs have already proven effective across EEG, EMG, and HRV applications, delivering tangible improvements in throughput, latency, and energy performance—key enablers of next-generation public-health and mHealth solutions [16], [22].

4. FPGA-BASED IMPLEMENTATIONS FOR BIOMEDICAL SIGNALS

The effectiveness of FPGA technology in biomedical signal processing lies in its ability to combine high performance, deterministic latency, and energy efficiency within compact, reconfigurable hardware [5], [6]. Over the past decade, numerous FPGA-based implementations have been developed for processing physiological signals such as EEG, EMG, and HRV [10], [11], [13]. These systems are designed to meet the stringent demands of real-time operation, low power consumption, and accurate feature extraction in wearable and mobile healthcare environments [10], [12]. The overall architecture and representative FPGA based implementations for these biomedical signal domains are illustrated in Figure 4, highlighting the diversity of design approaches and their relevance to public-health and mHealth applications [5], [23]. This section reviews state-of-the-art FPGA architectures applied to each signal domain and discusses comparative performance insights relevant to real-world deployment scenarios.

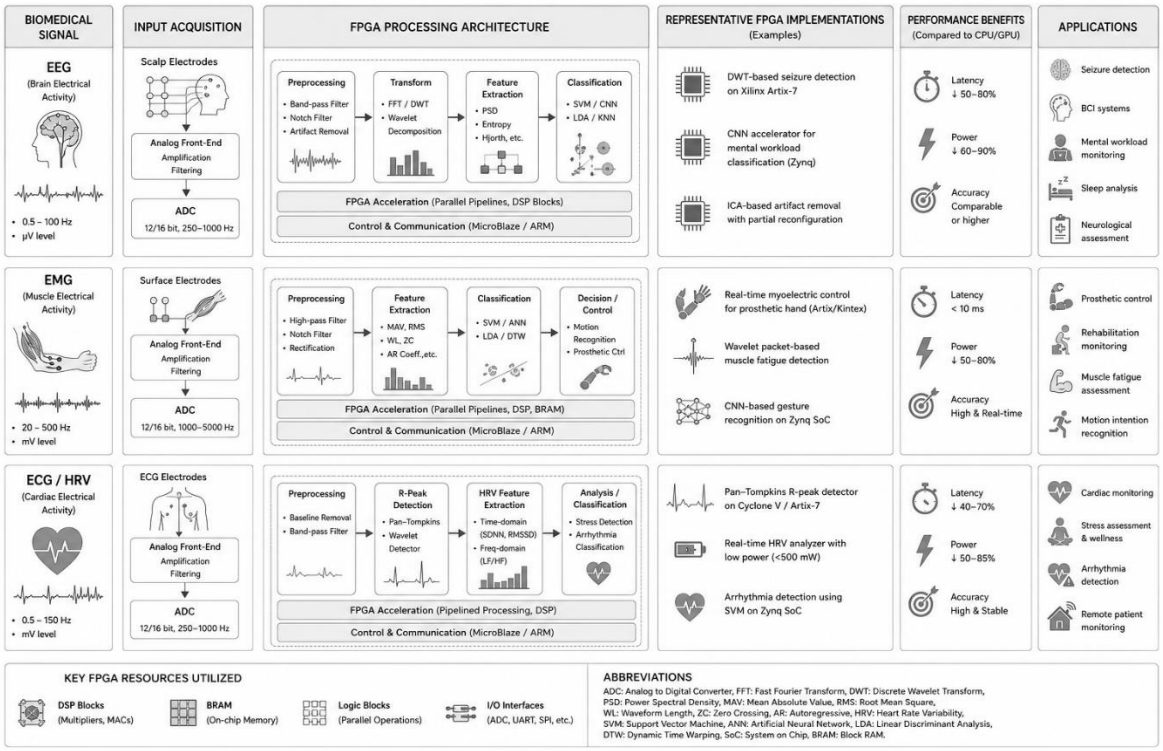

Figure 4. FPGA-based implementations for biomedical signals

4.1. Field-programmable gate array implementations for electroencephalography processing

EEG presents a unique computational challenge due to the large volume of high-frequency, low-amplitude signals that require real-time noise removal, feature extraction, and classification [10], [12]. Traditional software-based implementations often struggle to satisfy the latency requirements of clinical monitoring and brain–computer interface (BCI) applications [12]. FPGA-based EEG systems address these limitations by exploiting hardware-level parallelism to accelerate core signal-processing operations. For example, discrete wavelet transforms (DWT) and fast Fourier transform (FFT) modules have been implemented directly in FPGA fabric to perform multilevel filtering and spectral analysis [10], [12], [23]. Recent studies have reported substantial latency reductions compared with software-based approaches while maintaining reliable accuracy in event detection and seizure classification [10], [24].

In addition, artifact-removal techniques, such as independent component analysis (ICA) and adaptive filtering, have been efficiently mapped onto reconfigurable hardware pipelines [13]. Modern FPGA–SoC platforms further enhance system flexibility by integrating embedded processors, such as ARM Cortex-A9 cores, to support adaptive parameter updates and hybrid online EEG analysis [13], [14]. FPGA based machine-learning classifiers, including support vector machines (SVMs) and lightweight convolutional neural networks (CNNs), have also been deployed for cognitive-state recognition and mental-fatigue detection [13], [21]. Collectively, these developments demonstrate the potential of FPGA-based architectures

to deliver low-latency, energy-efficient, and scalable EEG processing for both clinical and wearable neuro-monitoring applications [10], [12], [23].

4.2. Field-programmable gate array implementations for electromyography processing

EMG processing benefits significantly from FPGA-based acceleration due to its demand for high-speed computation and continuous data flow [6], [13]. EMG signals, typically in the 20–500 Hz range, are widely used in prosthetic control, muscle-fatigue assessment, and tele-rehabilitation [13]. Processing involves several computationally intensive steps: pre-filtering, feature extraction, and pattern classification [13], [14]. FPGAs are particularly well-suited for real-time feature extraction, implementing metrics such as mean-absolute value (MAV), zero-crossing, waveform-length (WL), and autoregressive coefficients through pipelined hardware [12], [14]. Studies have demonstrated FPGA-based EMG systems achieving up to 10× lower latency and 5× lower power consumption compared with microcontroller or DSP-based designs [6], [13], [23].

A representative example is the implementation of an FPGA-controlled prosthetic hand, where surface EMG signals are processed through a hardware-accelerated SVM classifier [13], [14]. The architecture achieved real-time control with latency below 10 ms, enabling smooth motion transitions [12], [14]. In another approach, wavelet-packet decomposition (WPD) was implemented in FPGA fabric to extract muscle-fatigue features, showing substantial performance gains over CPU-based computation [13], [14], [23]. These architectures illustrate how reconfigurable designs not only meet timing constraints but also extend battery life for portable and wearable EMG applications—an essential factor in long-term rehabilitation and assistive technologies [6], [13], [23].

4.3. Field-programmable gate array implementations for heart-rate variability processing

HRV, derived from ECG signals, serves as an essential biomarker for cardiovascular and autonomic-nervous-system function [5], [11]. FPGA-based HRV systems focus on achieving high accuracy in R-peak detection and on efficient computation of HRV features in both time and frequency domains [5], [11], [23]. Early FPGA implementations employed threshold-based R-peak detectors with pipeline parallelism to ensure deterministic timing [11], [14]. Later designs integrated advanced algorithms such as Pan–Tompkins, Hilbert transform, and wavelet-based detectors, significantly improving detection accuracy while maintaining real-time performance [5], [11], [23]. A typical FPGA-based HRV processing pipeline includes:

- Preprocessing: baseline correction and bandpass filtering.
- R-peak detection: hardware implementation of adaptive thresholding.
- Feature computation: real-time calculation of RMSSD, SDNN, LF/HF ratio, and Poincaré plot parameters.

Recent designs demonstrate that FPGA-based HRV analyzers can achieve sampling rates above 250 Hz while consuming less than 500 mW—making them ideal for battery-operated ECG patches or chest-strap monitors [5], [11], [23]. Furthermore, integrating machine-learning modules into the FPGA fabric enables on-device classification of arrhythmias or stress states without the need for cloud processing, preserving data privacy and reducing communication latency [5], [11], [23].

4.4. Comparative analysis across biomedical signals

Comparative evidence from the reviewed literature suggests that FPGA-based implementations generally achieve lower latency and improved energy efficiency than software-based CPU and GPU implementations for many biomedical signal-processing tasks, while maintaining competitive classification or detection accuracy [5], [6], [13], [23], [24].

- Latency: many FPGA-based implementations report latency levels compatible with real-time biomedical monitoring and closed-loop healthcare applications, suitable for closed-loop and real-time monitoring.
- Power efficiency: PGA-based systems generally exhibit significantly lower power consumption than GPU-based solutions, making them attractive for wearable and battery-powered healthcare devices.
- Adaptability: partial reconfiguration enables hardware reuse across multiple biomedical modalities, improving scalability.

However, the trade-off lies in the complexity of FPGA development and the need for domain-specific optimization to maximize resource utilization. The use of HLS and AI hardware compilers is mitigating this challenge by abstracting low-level design steps and automating parameter tuning [19]–[21], [23].

From a healthcare perspective, these FPGA-based solutions contribute directly to public-health outcomes by enabling continuous, decentralized monitoring and low-cost diagnostic platforms deployable in remote or resource-limited settings [5], [6], [23], [24]. The convergence of low-power design, AI

acceleration, and hardware adaptability establishes FPGAs as a transformative enabler for scalable and sustainable public-health systems [5], [6], [23], [24]. To provide a broader architectural perspective, Table 1 summarizes the general characteristics of CPUs, GPUs, FPGAs, and ASICs in terms of performance, power efficiency, flexibility, and deployment considerations reported in the literature. This qualitative comparison highlights key architectural trade-offs rather than specific benchmark results. While each platform offers distinct advantages, FPGA-based architectures provide a particularly effective balance between computational performance, power efficiency, and design flexibility for biomedical signal processing applications. Unlike ASICs, which achieve high efficiency but offer limited adaptability, FPGAs support post-deployment reconfiguration, enabling healthcare systems to incorporate evolving signal-processing algorithms, AI models, and clinical requirements without hardware replacement. Combined with low-power operation and real-time processing capabilities, these features make FPGAs an attractive platform for wearable monitoring, telemedicine, edge-AI healthcare systems, and scalable public-health applications.

Table 1. General comparison of computing architectures for biomedical signal processing applications

Metric	CPU	GPU	FPGA	ASIC
Latency	High	Medium	Low	Very low
Power efficiency	Low	Low	High	Very high
Reconfigurability	High	Medium	High	None
Development cost	Low	Medium	Medium	Very high
Suitability for mHealth	Moderate	Moderate	High	Limited

5. INTEGRATION WITH MHEALTH AND PUBLIC HEALTH SYSTEMS

The practical value of FPGA-based biomedical signal processing is best realized when these technologies are integrated into broader mHealth and public-health ecosystems. Such integration enables continuous health monitoring, decentralized diagnostics, and real-time clinical decision-making. In recent years, the fusion of reconfigurable computing with edge and cloud infrastructures has emerged as a key enabler for next-generation telemedicine platforms. FPGAs, due to their reconfigurability, high throughput, and low energy requirements, serve as ideal edge-computing devices for real-time biosignal analysis, while supporting secure, scalable data exchange with centralized health systems [5], [6], [22], [23]. The conceptual framework for this integration is illustrated in Figure 5, which depicts how FPGA-based biomedical devices interface with edge, cloud, and public-health layers to enable seamless, data-driven healthcare delivery.

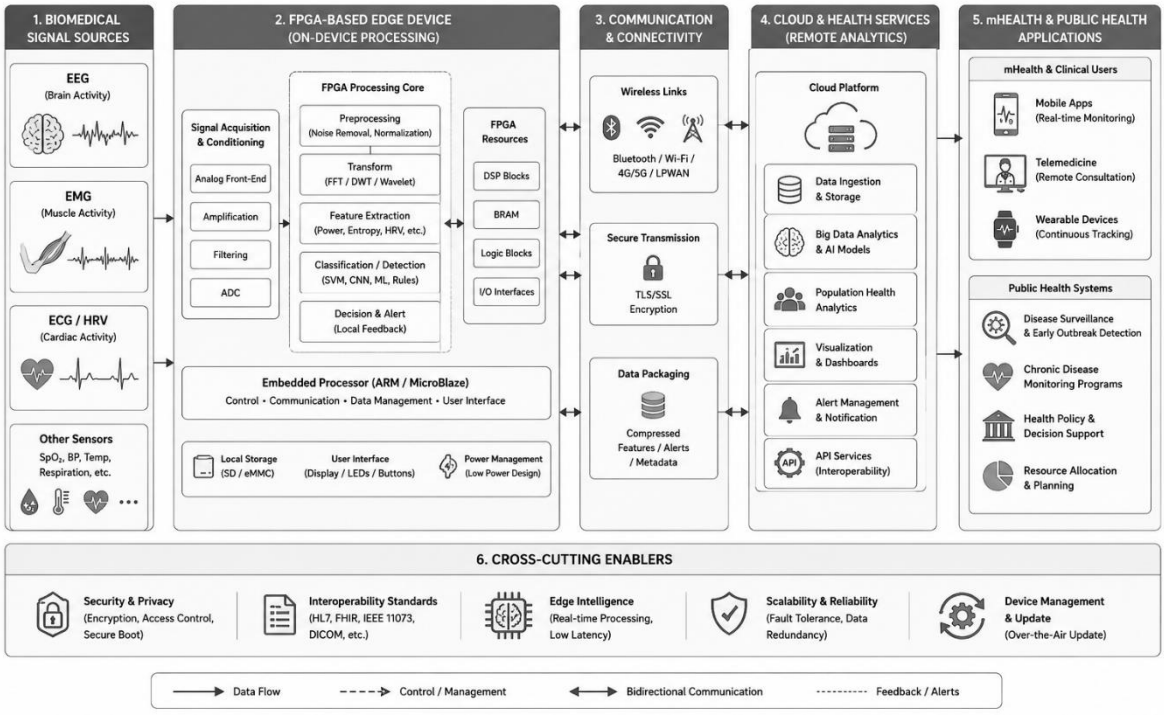

Figure 5. Integration of FPGA-based biomedical systems with mHealth and public health systems

5.1. Edge–cloud architectures for health monitoring

The deployment of biomedical systems in public health increasingly adopts a hierarchical architecture that spans from wearable edge devices to cloud-based analytics. In this framework, FPGAs function as intelligent edge processors that execute time-sensitive tasks—such as noise filtering, feature extraction, and anomaly detection—directly on-device. By processing signals locally, latency is minimized and only high-level features or diagnostic summaries are transmitted to the cloud, thereby conserving bandwidth and improving privacy [5], [6], [8], [11], [13], [22], [23]. A typical workflow involves tiers:

- Sensor layer–biomedical sensors (EEG, EMG, and ECG) acquire raw data and feed it to FPGA modules for initial preprocessing [5], [6].
- Edge layer–FPGA or SoC-based nodes perform real-time signal analysis, classification, or alert generation [5], [6], [23].
- Cloud layer–aggregated data from multiple users are stored and analyzed for population-level trends, epidemiological modeling, and remote physician review [6], [11], [22], [23].

FPGA-enabled edge devices can adapt dynamically through partial reconfiguration, allowing new algorithms to be uploaded remotely as medical requirements evolve [5], [6], [8], [11]. This architecture supports continuous patient monitoring even in areas with limited network connectivity, thereby extending healthcare accessibility [6], [11], [23], [24].

5.2. Interoperability and data standards

Interoperability is a foundational requirement for integrating FPGA-based devices into national or global health networks [5], [8], [22]. Medical data must adhere to standardized protocols to ensure seamless communication between devices, healthcare providers, and databases [5], [8], [22], [23]. Modern FPGA-based systems are increasingly being designed to comply with health level seven (HL7), fast healthcare interoperability resources (FHIR), and IoMT standards [5], [6], [22], [23].

By implementing these communication protocols at the hardware level, FPGAs can facilitate low-latency, secure data transmission directly from biosensors to electronic health record (EHR) systems [5], [8], [22], [23]. Hardware-level support for encryption (e.g., AES and RSA) and authentication protocols enhances data integrity and confidentiality—critical for protecting sensitive medical information [5], [6], [8], [22]. Moreover, reconfigurable logic allows updates to communication stacks as interoperability standards evolve, providing long-term system sustainability [6], [8], [22], [23]. Such standardization is essential for public-health surveillance, where aggregated biomedical data from diverse devices contribute to predictive analytics and early outbreak detection [5], [6], [23], [25]. FPGA-based systems, through their modular communication architecture, offer a path toward harmonized and compliant digital-health infrastructures [5], [8], [23], [25].

5.3. Case studies in mHealth platforms

FPGA-enabled health monitoring has transitioned from laboratory prototypes to commercially relevant mHealth platforms [5], [6], [11], [13], [23]. Several notable implementations illustrate how reconfigurable architectures enhance real-world health applications [5], [8], [23], [25]:

- EEG headsets for cognitive monitoring: portable FPGA-based EEG headsets have been developed for fatigue and cognitive-load assessment in occupational settings [10], [11], [13], [23]. By performing on-device filtering and spectral analysis, these systems eliminate the need for high-bandwidth wireless transmission, achieving power reductions of over 70% compared to GPU-based solutions [10], [13], [23].
- Wearable ECG and HRV devices: low-power FPGA cores integrated into ECG chest straps and wristbands allow real-time HRV analysis and arrhythmia detection [5], [11], [13], [23]. The processed results are transmitted to mobile applications for visualization and clinical alerts, enabling preventive cardiac care [5], [13], [23].
- Rehabilitation and prosthetic systems: FPGA-controlled EMG interfaces in smart prosthetics support adaptive motor control, improving response time and energy efficiency [5], [6], [13], [23]. These systems can operate independently or communicate with cloud-based rehabilitation platforms for patient progress tracking [5], [13], [23].
- Community health monitoring nodes: in developing regions, FPGA-based multi-signal acquisition units have been deployed for rural health screening, integrating ECG, temperature, and SpO_2 sensors [5], [11], [23], [24]. The devices perform initial triage at the edge and synchronize with cloud databases when connectivity permits, exemplifying scalable and cost-effective healthcare delivery [5], [23], [24].

These case studies highlight how FPGA technology bridges the gap between high-performance biomedical signal processing and practical public-health solutions [5], [6], [11], [23].

5.4. Scalability and sustainability considerations

For FPGA-based health systems to achieve large-scale impact, scalability and sustainability must be prioritized. Scalable architectures require modularity—allowing new sensors, algorithms, or communication interfaces to be added without redesigning the entire hardware platform. FPGAs naturally support such extensibility through programmable logic and DPR. From a sustainability perspective, FPGA-based systems contribute to energy-efficient healthcare infrastructure, reducing carbon footprint through low-power edge computing and extended device lifecycles. Reprogrammability also minimizes electronic waste, as devices can be upgraded via firmware updates instead of hardware replacement. Furthermore, the emergence of open-source FPGA toolchains (e.g., OpenCL and Vitis HLS) enhances accessibility for researchers and public institutions, fostering innovation and local capacity building in digital health technologies [5], [6], [11], [23], [24].

5.5. Implications for public health

The integration of FPGA-based biomedical systems into mHealth ecosystems represents a paradigm shift in how health data are collected, processed, and utilized. Real-time, edge-driven analytics support proactive healthcare, enabling early intervention and reducing hospital dependency. At a broader level, population-scale deployment of such devices facilitates data-driven public-health management, including trend analysis, behavioral-health assessment, and early detection of systemic risks. By combining adaptability, interoperability, and energy efficiency, FPGAs serve as a cornerstone technology for resilient digital-health ecosystems. Their deployment within mobile and public-health frameworks has the potential to enhance both individual patient outcomes and the operational efficiency of healthcare systems worldwide [5], [6], [17], [23], [24].

6. CROSS-CUTTING FPGA DESIGN STRATEGIES

The successful deployment of FPGA-based biomedical systems in real-world health applications depends not only on architecture selection but also on the application of efficient design strategies that balance energy, performance, adaptability, and security. As biomedical signal processing often involves continuous and dynamic workloads, optimizing these systems requires a holistic approach that spans hardware–software integration, low-power design, machine-learning acceleration, and data protection. This section presents a synthesis of cross-cutting FPGA design methodologies that underpin state-of-the-art health-monitoring and telemedicine systems [5], [6], [8], [23].

6.1. Hardware–software co-design

Hardware–software co-design represents a fundamental paradigm for building flexible and efficient FPGA-based biomedical systems [5], [6], [8], [12], [13]. It enables designers to partition computational tasks between programmable logic (hardware) and embedded processor cores (software), optimizing for both performance and flexibility.

In biomedical applications, algorithms such as digital filtering, feature extraction, and transformation (FFT and DWT) are typically offloaded to the FPGA fabric, where they can execute in parallel with deterministic latency. Conversely, non–time-critical tasks, including data aggregation, communication, and control flow, are managed by the embedded CPU cores integrated within FPGA SoC platforms (e.g., Xilinx Zynq or Intel SoC FPGAs) [5], [10], [12]–[14].

This hybrid model provides a balanced compromise: FPGA acceleration ensures real-time responsiveness, while software layers maintain adaptability to new algorithms and user interfaces [5], [6], [8], [13]. Moreover, HLS tools, such as Xilinx Vitis HLS or intel HLS compiler, simplify this co-design process by allowing biomedical engineers to describe algorithms in C/C++ or OpenCL. Studies have demonstrated that FPGA–SoC designs can achieve 5–15× performance improvements over pure software implementations while maintaining reconfigurability—a critical feature for evolving medical applications [5], [6], [10], [13], [14], [19], [20].

6.2. Low-power design techniques

Energy efficiency is a primary design consideration for wearable and mHealth devices. Power constraints directly influence usability, battery life, and sustainability—especially in continuous monitoring scenarios. FPGAs enable several hardware-level strategies to minimize power consumption without sacrificing computational performance [5], [8], [23], [24]:

- DPR: allows modification of specific FPGA regions at runtime while the rest of the device continues to operate. In biomedical systems, this technique enables switching between processing modes (e.g., filtering vs. classification) as needed, reducing active power by up to 40% [8], [23], [24].

- Clock gating and voltage scaling: by selectively disabling unused clock regions or dynamically adjusting supply voltage, FPGAs can significantly lower dynamic and static power consumption. These techniques are particularly beneficial in energy-constrained wearable devices for HRV and EMG monitoring [5], [8], [23], [24].
- Hardware reuse and time multiplexing: time-multiplexed pipelines allow multiple biosignal-processing stages to share hardware resources sequentially, balancing energy use with performance [5], [6], [8], [13], [23].
- Algorithmic optimization: simplified or approximate algorithms—such as reduced-precision arithmetic or fixed-point representation—can be implemented without compromising clinical accuracy. Empirical evaluations have shown up to 60% energy savings compared to full-precision designs [5], [8], [13], [23], [24].

The combination of these strategies establishes a framework for sustainable biomedical FPGA systems, particularly in mHealth environments where long-term autonomy is essential.

6.3. Artificial intelligence and machine learning on field-programmable gate arrays

The integration of AI into FPGA-based biomedical systems represents a major evolution in digital health technology. FPGAs are uniquely suited to host AI accelerators that support deep-learning inference at the edge, providing real-time diagnostic insights while preserving data privacy[5], [6], [8], [13], [20], [21], [23]. Lightweight neural network architectures—such as CNNs, recurrent neural networks (RNNs), and spiking neural networks (SNNs)—can be mapped efficiently onto FPGA hardware. FPGA-based CNN accelerators have demonstrated high-throughput classification for EEG-based seizure detection, EMG pattern recognition, and HRV-based stress assessment [5], [8], [10], [13], [20], [21], [23].

Through parameter quantization, pruning, and model compression, these accelerators achieve inference performance comparable to GPU systems while consuming less than 20% of the power. Moreover, emerging frameworks like TensorFlow Lite for FPGAs and Vitis AI enable rapid deployment of pre-trained models, bridging the gap between algorithm development and hardware realization. Combined with hardware–software co-design, AI-capable FPGAs facilitate adaptive health systems capable of self-learning and reconfiguration based on patient-specific data—a key step toward personalized medicine [5], [6], [8], [20], [21], [23], [24].

6.4. Security and data integrity

As biomedical systems handle sensitive health information, maintaining data integrity and security is as important as computational efficiency. Reconfigurable hardware introduces unique challenges and opportunities in this [5], [6], [8], [22], [25]:

- Encryption and authentication: FPGA-based designs can integrate hardware-accelerated cryptographic modules (AES, RSA, and SHA) to secure data during acquisition and transmission. These implementations outperform software encryption by several orders of magnitude while maintaining low latency [5], [8], [22], [25].
- Secure boot and bitstream protection: to prevent unauthorized reconfiguration or bitstream tampering, secure boot mechanisms verify firmware integrity during system startup. Encryption of configuration files ensures that FPGA logic remains protected from reverse engineering or malicious modification [5], [8], [22], [23], [25].
- Access control and data privacy: biomedical systems must comply with regulatory frameworks such as general data protection regulation (GDPR) and health insurance portability and accountability act (HIPAA). FPGAs can enforce access policies through embedded hardware firewalls and dedicated authentication modules. Edge-level AI inference also minimizes data exposure by processing sensitive signals locally rather than in the cloud [5], [8], [21], [22], [25].
- Fault tolerance and reliability: built-in redundancy and error-correction mechanisms enhance the reliability of medical-grade FPGA systems. This ensures consistent performance in safety-critical applications, such as cardiac monitoring and neuroprosthetic control [5], [8], [23]–[25].

Together, these mechanisms create a secure computational environment that aligns with regulatory and ethical requirements, strengthening public trust in digital health technologies.

6.5. Toward unified optimization frameworks

The intersection of co-design, power management, AI integration, and security defines a multidimensional optimization problem in FPGA-based biomedical systems. Future development increasingly relies on automated design frameworks that can balance these competing objectives. Emerging methodologies leverage AI-driven design space exploration (DSE) to automatically determine optimal

configurations for performance, power, and area trade-offs. Such frameworks will accelerate the adoption of FPGAs in healthcare by simplifying customization and reducing engineering barriers [5], [6], [8], [10], [19]–[21], [23], [24].

6.6. Summary

The strategies summarized in Figure 6 demonstrate how hardware–software co-design, low-power techniques, AI integration, and security measures work together to enable scalable, adaptive, and secure FPGA-based biomedical systems. These cross-cutting design strategies form the backbone of modern FPGA implementations. By integrating co-design, power-aware optimization, and embedded intelligence, FPGAs can deliver medical-grade signal processing that is efficient, flexible, and robust. Such techniques allow reconfigurable systems to meet the stringent requirements of mHealth and public-health applications, ensuring that future healthcare technologies remain both high-performing and sustainable [5], [6], [8], [17], [23], [24].

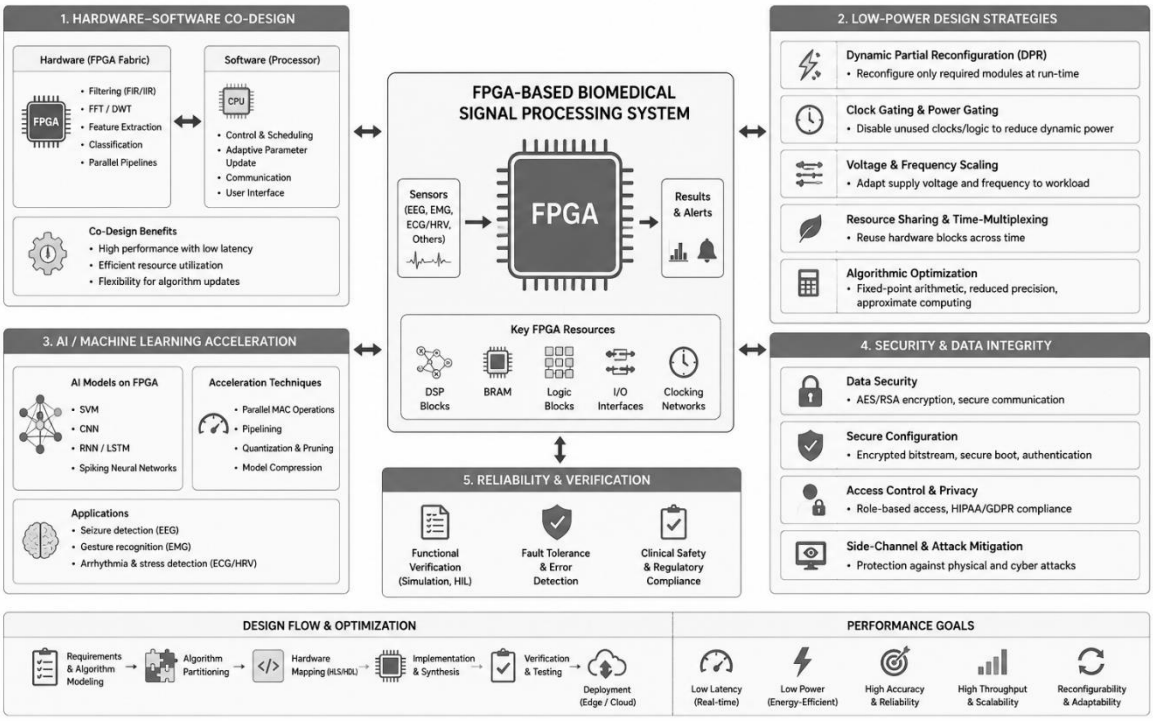

Figure 6. Cross-cutting FPGA design strategies for biomedical signal processing

7. CHALLENGES AND RESEARCH GAPS

Despite substantial advances in FPGA-based biomedical signal processing, several persistent challenges continue to limit widespread adoption in clinical and public-health contexts. These challenges extend beyond hardware optimization, encompassing software complexity, interoperability, security, and regulatory considerations. Understanding and addressing these limitations is crucial to translating reconfigurable computing technologies into sustainable, patient-centered healthcare solutions [5], [8], [23], [24].

7.1. Power–performance trade-offs

Although FPGAs provide significantly better energy efficiency than CPUs and GPUs for many biomedical applications, they still face inherent power–performance trade-offs. Achieving ultra-low power operation often requires sacrificing computational throughput or precision [5], [6], [8], [23]. Biomedical systems that rely on continuous monitoring—such as ECG and EEG recorders—must operate within tight energy budgets, particularly for battery-powered wearables [5], [6], [8], [10], [13], [23].

DPR and clock-gating techniques mitigate this challenge but introduce additional design complexity and timing constraints. Moreover, fine-grained power control remains difficult in heterogeneous SoCs where multiple subsystems share resources. Future research must focus on developing adaptive power-management frameworks that dynamically scale energy consumption according to workload intensity and physiological

event detection requirements. The integration of machine-learning-based power controllers offers a promising direction for achieving context-aware energy optimization [5], [8], [20], [21], [23].

7.2. Lack of standardized frameworks and interoperability

A major barrier to the broader adoption of FPGA-based biomedical systems is the absence of standardized design frameworks and interoperability protocols. Unlike software ecosystems, where modular libraries and APIs are well established, FPGA development lacks universal standards for biomedical data interfaces, algorithmic integration, and verification procedures [5], [6], [8], [22], [23].

As a result, designs are often platform-specific and difficult to reuse or adapt across different hardware or healthcare infrastructures. This fragmentation limits scalability and slows down innovation, particularly in multi-institutional or cross-border public-health projects. Establishing open-source, interoperable FPGA design ecosystems—with standardized IP cores for biomedical filtering, feature extraction, and encryption—would greatly enhance collaboration between engineers, clinicians, and researchers. Harmonization with healthcare standards such as HL7, FHIR, and IEEE 11073 remains a crucial step toward seamless data exchange between FPGA-based devices and medical information systems [5], [8], [22], [23], [25].

7.3. Design complexity and accessibility

Developing FPGA systems for biomedical applications requires specialized knowledge in HDLs, DSP, and system verification—expertise that is often beyond the reach of biomedical researchers or clinicians. This steep learning curve presents a major barrier to interdisciplinary collaboration. Although HLS and AI-assisted design tools have reduced entry barriers, many researchers still find FPGA workflows non-intuitive compared with traditional software development. Additionally, achieving optimal timing closure and power efficiency often demands iterative low-level tuning. To address this, there is a pressing need for domain-specific design automation tools that abstract hardware complexity while maintaining performance. Such tools should integrate algorithm-to-hardware mapping, automated resource allocation, and medical-signal validation pipelines, thereby enabling faster prototyping and clinical translation [5], [8], [20], [21], [23], [24].

7.4. Limited clinical validation and regulatory challenges

While numerous FPGA-based biomedical systems have demonstrated strong technical performance in laboratory settings, few have undergone comprehensive clinical validation. Most reported works focus on algorithmic accuracy and hardware efficiency rather than patient safety, long-term reliability, or compliance with medical-device regulations. Bridging this gap requires structured validation studies in collaboration with hospitals and healthcare agencies. FPGA-based devices must also meet the stringent requirements of international standards, such as IEC 60601 for electrical safety and ISO 13485 for medical-device quality management. Furthermore, the regulatory approval process for reconfigurable systems poses unique challenges: because FPGA logic can be updated post-deployment, ensuring compliance after each reconfiguration becomes a non-trivial task. Developing regulatory frameworks tailored to reconfigurable medical hardware would facilitate the safe adoption of these systems in clinical practice [5], [8], [17], [23], [25].

7.5. Data privacy and security concerns

Biomedical systems inherently handle sensitive personal data, and FPGA-based implementations must address security at every stage of operation. Although hardware encryption and secure-boot mechanisms provide strong protection, vulnerabilities can still arise from bitstream manipulation, side-channel attacks, or insecure firmware updates [5], [8], [22], [23], [25].

Moreover, as FPGA-based devices increasingly connect to IoMT and cloud platforms, risks related to unauthorized access and data leakage intensify. Ensuring privacy and compliance with frameworks such as the GDPR and the HIPAA requires robust end-to-end encryption, hardware-based authentication, and fine-grained access control mechanisms. Future research should explore privacy-preserving FPGA architectures, such as homomorphic encryption accelerators or federated-learning models that allow distributed data processing without exposing sensitive information [5], [8], [17], [21], [23], [25].

7.6. Integration barriers in public-health contexts

Scaling FPGA-based biomedical systems to population-level health initiatives introduces additional challenges in data management, communication bandwidth, and device maintenance. Public-health infrastructures typically integrate heterogeneous devices and sensors from multiple vendors, each with differing communication standards and computational capabilities. Synchronizing data streams from thousands of FPGA-enabled sensors demands standardized middleware and efficient data-fusion techniques [5], [8], [22]–[25].

Furthermore, in developing regions, logistical constraints such as limited power availability, inconsistent connectivity, and cost sensitivity hinder large-scale adoption. Addressing these barriers requires a focus on low-cost, open-hardware FPGA platforms and edge–cloud synchronization frameworks that can function under limited resources. Partnerships between academic institutions, public-health organizations, and industry are essential to building robust, scalable digital-health ecosystems [5], [6], [8], [17], [23].

7.7. Summary of research gaps

To summarize, several open research questions remain in the pursuit of fully integrated, clinically validated FPGA-based biomedical systems [5], [6], [8], [10], [13], [23]:

- How can FPGA design automation be improved to simplify adoption across disciplines?
- What standardized frameworks will ensure interoperability and regulatory compliance?
- How can real-time power management and AI-driven adaptability be balanced?
- What security architectures best protect patient data in reconfigurable environments?
- How can FPGA systems be scaled sustainably to serve population-level public-health monitoring?

Addressing these gaps will require sustained collaboration between hardware engineers, biomedical scientists, data-security experts, and healthcare policymakers. Such multidisciplinary engagement will ensure that FPGA technology evolves beyond a high-performance computing tool into a trusted, scalable backbone for the next generation of intelligent, accessible, and secure healthcare systems.

8. FUTURE DIRECTIONS

The future of FPGA-based biomedical signal processing lies at the convergence of advanced hardware design, intelligent computing, and sustainable healthcare systems. As global health priorities shift toward personalized, preventive, and data-driven care, reconfigurable embedded architectures will become central to enabling scalable, adaptive, and energy-efficient medical technologies [5], [6], [8], [11], [13], [23]. Figure 7 illustrates the emerging paradigms—AI-driven hardware adaptability, neuromorphic and in-memory computing (IMC), sustainability-focused design, and global accessibility—that are poised to transform how FPGA platforms support digital public health.

8.1. Artificial intelligence-driven reconfigurable architectures

One of the most promising trends in biomedical FPGA development is the integration of AI directly into reconfigurable hardware. Traditionally, FPGAs have been used as fixed-function accelerators for filtering, transformation, or feature extraction. However, future systems are expected to incorporate AI-driven adaptability, where embedded machine-learning models autonomously optimize hardware configurations in response to dynamic workloads and signal variations [5], [8], [20], [21], [23].

For example, FPGA fabrics could host reinforcement-learning agents capable of reconfiguring processing pipelines based on detected physiological patterns, thereby allocating more resources during critical health events (e.g., arrhythmia onset) and conserving power during stable conditions. Similarly, self-optimizing compilers could enable hardware-aware neural architecture search (NAS), tailoring deep learning models to FPGA constraints without manual intervention. These adaptive mechanisms would transform FPGA-based health devices into intelligent, context-aware systems capable of evolving in real time alongside patients' physiological states [5], [8], [20], [21], [23], [24].

8.2. Neuromorphic and in-memory computing integration

Traditional von Neumann architectures face fundamental bottlenecks related to memory access latency and power dissipation. To overcome these limitations, researchers are increasingly exploring neuromorphic and IMC paradigms, which emulate brain-inspired information processing and reduce data movement between computation and storage units [5], [8], [20], [21], [23], [24].

FPGAs, due to their configurability, are ideal platforms for prototyping neuromorphic circuits that mimic SNNs or synaptic plasticity mechanisms. Such architectures could enable real-time classification of EEG or EMG signals using event-driven computation that consumes only microwatts of power. Similarly, integrating in-memory computation modules—such as resistive RAM (ReRAM) or phase-change memory (PCM)—within FPGA-based systems could accelerate HRV analysis by performing matrix operations directly in the memory domain [5], [8], [20], [21], [23], [24]. The convergence of FPGA reconfigurability with neuromorphic efficiency holds the potential to revolutionize low-power biomedical analytics, paving the way for implantable and always-on monitoring systems capable of operating autonomously for years.

8.3. Sustainable and energy-aware design paradigms

As healthcare systems aim for sustainability, the energy and environmental footprint of medical electronics have become an essential consideration. FPGAs already offer advantages over traditional processors due to their reusability and efficiency, but future development will need to embrace carbon-aware design methodologies. Energy profiling tools integrated into FPGA design environments could allow developers to quantify the carbon cost of computation and optimize configurations for minimal environmental impact. Similarly, lifecycle-oriented hardware design—prioritizing reusability, modularity, and recyclability—will be critical for reducing electronic waste. Open hardware initiatives that promote repairable and upgradeable FPGA-based devices can further extend system lifetimes and reduce healthcare e-waste. Sustainability also encompasses operational resilience: in rural or resource-constrained settings, FPGA-based health devices must operate efficiently on renewable energy sources such as solar or kinetic harvesting. Designing for energy autonomy ensures that the benefits of digital health reach underserved populations without exacerbating energy inequities [5], [6], [8], [17], [23].

8.4. Global accessibility and low-cost reconfigurable platforms

Bridging the digital divide in healthcare requires affordable and accessible technology. The flexibility of FPGA architectures can be harnessed to create low-cost, open-source biomedical platforms tailored to regional needs. Initiatives using low-end FPGAs or FPGA-based system-on-modules (SoMs) can provide scalable hardware frameworks for local universities, hospitals, and startups to develop telemedicine solutions without relying on proprietary tools [5], [8], [17], [23], [24].

Collaborative projects—such as the open health hardware initiative (OHHI)—aim to democratize biomedical device development by sharing reference designs, hardware description libraries, and validation datasets. FPGA-based systems designed under open hardware principles can support local manufacturing, reduce supply-chain dependencies, and encourage innovation in developing regions. Furthermore, incorporating multilingual firmware interfaces and adaptable connectivity standards ensures inclusivity and interoperability across diverse healthcare infrastructures. As global health challenges become increasingly interconnected, accessible FPGA-based systems could serve as a universal foundation for population-level health analytics and epidemiological modeling [5], [8], [17], [23], [24].

8.5. Standardization, security, and ethical artificial intelligence

Future FPGA-based healthcare technologies will need to align closely with regulatory, ethical, and cybersecurity frameworks. As devices gain autonomy through AI-driven reconfiguration, explainable and verifiable hardware behavior becomes essential for clinical acceptance. Standardized methodologies for verifying FPGA configurations, encryption modules, and AI inference processes will ensure transparency and trustworthiness [5], [8], [17], [22], [23], [25].

Security will evolve toward post-quantum cryptographic architectures implemented directly in reconfigurable hardware, safeguarding long-term medical data confidentiality. In parallel, ethical AI principles—such as fairness, accountability, and non-discrimination—must be integrated into FPGA–AI co-design pipelines. This ensures that edge-based health intelligence respects privacy and equality while enhancing clinical efficacy. Efforts toward global interoperability standards—combining medical data protocols (HL7 and FHIR) with hardware certification frameworks—will accelerate regulatory approval and deployment in clinical environments [5], [8], [17], [22], [23], [25].

8.6. Toward a unified field-programmable gate array-based public health infrastructure

The long-term vision for FPGA-based biomedical signal processing extends beyond individual health devices toward a distributed public-health infrastructure powered by reconfigurable computing. Such an ecosystem would integrate millions of edge devices performing continuous biosignal analysis, feeding anonymized, aggregated data to cloud-based analytics platforms [5], [6], [8], [23], [24].

Real-time insights derived from this network could guide preventive health interventions, predict outbreaks, and support population-wide wellness. By combining edge intelligence, cloud connectivity, and ethical AI, FPGAs could become the backbone of data-driven, equitable healthcare systems—bridging the gap between clinical precision and public-health scale. Achieving this vision will require not only technological innovation but also cross-sector collaboration among engineers, healthcare providers, policymakers, and global health organizations scale [5], [6], [8], [17], [23], [24].

8.7. Summary

In summary, the next generation of FPGA-based biomedical systems will be defined by intelligence, adaptability, and sustainability. As illustrated in Figure 7, advances in AI-driven hardware reconfiguration, neuromorphic design, energy-aware techniques, and low-cost open platforms will transform how health data

are processed and applied. These technologies will democratize healthcare, enable continuous monitoring, and support data-driven public-health decision-making. By integrating reconfigurable computing with ethical, accessible, and sustainable design principles, FPGA-based systems offer a transformative pathway toward resilient and inclusive global healthcare [5], [6], [8], [17], [23], [24].

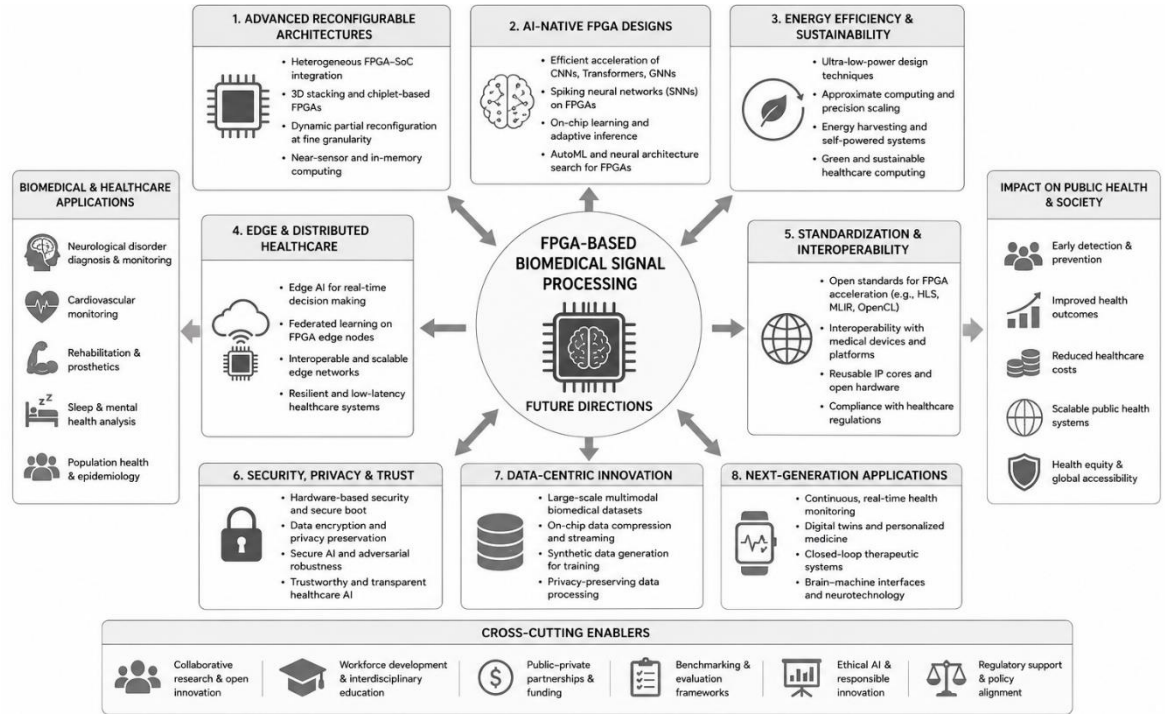

Figure 7. Future directions for FPGA-based biomedical signal processing

9. CONCLUSION

The advancement of FPGA-based biomedical signal processing marks a pivotal evolution in digital health and public-health technology. By bridging the gap between flexibility and efficiency, reconfigurable embedded architectures provide a powerful foundation for real-time, energy-aware, and adaptive health-monitoring systems. Across key biomedical domains—EEG, EMG, and HRV—FPGA implementations have demonstrated substantial improvements in latency, throughput, and power efficiency compared to conventional CPU- and GPU-based platforms. These advantages enable continuous and decentralized healthcare delivery, supporting wearable, portable, and telemedicine applications that align with the emerging paradigms of preventive and personalized medicine. Beyond their technical strengths, FPGAs play a transformative role in integrating biomedical signal processing within mHealth and public-health ecosystems. Their compatibility with edge–cloud architectures and interoperability standards allows scalable population-level monitoring and rapid clinical response. Through hardware–software co-design, DPR, and embedded AI acceleration, FPGA-based systems have evolved from laboratory prototypes into practical tools for real-world healthcare management. Furthermore, advances in low-power design and runtime adaptability have positioned FPGAs as a cornerstone for sustainable, energy-efficient medical technologies that extend beyond individual diagnostics to broader societal well-being. Nevertheless, several challenges persist. Power–performance trade-offs, limited standardization, design complexity, and the lack of large-scale clinical validation continue to restrict widespread adoption. Addressing these barriers requires interdisciplinary collaboration among engineers, biomedical scientists, and healthcare policymakers to ensure that technological innovation translates into safe, accessible, and equitable healthcare solutions. Emerging paradigms such as AI-driven reconfigurable architectures, neuromorphic computing, and open-source FPGA frameworks hold great promise in overcoming these limitations while advancing sustainability and affordability. In conclusion, FPGA-based biomedical signal processing represents a vital convergence of hardware innovation and public-health impact. As reconfigurable systems become increasingly intelligent, secure, and adaptive, they are poised to underpin the next generation of digital healthcare—delivering scalable, precise, and ethically grounded technologies capable of transforming how health is monitored, analyzed, and delivered worldwide.

ACKNOWLEDGMENTS

The authors gratefully acknowledge the institutional support provided by Universitas Ahmad Dahlan (UAD) and Universiti Teknikal Malaysia Melaka (UTeM), which was instrumental in facilitating this research. Special appreciation is extended to the Embedded System and Power Electronics Research Group (ESPERG) for their sustained technical contributions, collaborative engagement, and domain-specific expertise. The ESPERG team's involvement significantly enriched the methodological rigor and practical relevance of the study, particularly in the areas of embedded system design and power optimization. The AI tool (ChatGPT) was used solely for visualization and illustration purposes. All scientific content and interpretations were provided and verified by the authors.

FUNDING INFORMATION

The research was funded by PT. Intelektual Pustaka Media Utama (IPMU) under contract number 07/RST-E/IPMU/I/2025, which supported the facilitation of this work.

AUTHOR CONTRIBUTIONS STATEMENT

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C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

Authors state no conflict of interest.

DATA AVAILABILITY

Data availability is not applicable to this paper as no new data were created or analyzed in this study.

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