

A low power comparator utilizing MTSCStack, DTTS, and bulk-driven techniques

Mohd Tafir Mustaffa

School of Electrical and Electronic Engineering, Universiti Sains Malaysia, Malaysia

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ABSTRACT

Comparator is one of the main blocks that play a vital task in the performance of analog to digital converters (ADC) in all modern technology devices. High-speed devices with low voltage and low power are considered essential for industrial applications. The design of a low-power comparator with high speed is required to accomplish the requirements mostly in electronic devices that are necessary for high-speed ADCs. However, a high-speed device that leads the scaling down of CMOS process technology will consume more power. Thus, power reduction techniques such as multi-threshold super cut-off stack (MTSCStack), dual-threshold transistor stacking (DTTS), a bulk-driven, and a bulk-driven differential pair were studied in this work. This study aims to find and build the combination of these techniques to produce a comparator that can operate in low power without compromising existing performance using the 0.13- μm CMOS process. A comparator with a combination of MTSCStack, DTTS, and NMOS bulk-driven differential pair shows the most promising result of 6.29 μW for static power, 17.15 μW for dynamic power, and 23.44 μW for total power.

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Corresponding Author:

Mohd Tafir Mustaffa

School of Electrical and Electronic Engineering

Universiti Sains Malaysia

14300 Nibong Tebal, Pulau Pinang, Malaysia

Email: tafir@usm.my

1. INTRODUCTION

For years, the consumer electronics such as phone, laptop, or any other IC-based devices have dramatically enjoyed a better performance in terms of speed, due to the increasing amount of the transistors that can fit into the same size of such devices. The higher number of transistors per unit area that resides in such devices was made possible due to the scaling down of IC technology namely CMOS technology. However, this smaller transistor comes with a problem of power dissipation known as leakage power [1], [2]. Leakage power is now a dominating component of total power consumption in IC-based devices. So, researchers have started introducing the state-of-the-art techniques to develop a low power circuit in almost all the new consumer electronics products.

For instance, a handset always has a component known as the transceiver chip. One vital component in that chip is analog to digital converters or known as analog to digital converters (ADC). They are used to process, transport, or store any analog signal in digital form. ADC mainly consists of a comparator. According to past work, the comparator is responsible for about 70% of the ADC speed [3], [4]. ADC is currently adopted in many application fields to improve the digital system, which achieves superior performance concerning analog solutions.

As reported by [5], [6], the impact of leakage power to the total power consumption is steadily increasing due to the scaling down of CMOS technology. Thus, the fundamental principle of low power is to start with less leakage current. To reduce the dynamic and static power consumption, low power techniques must be applied to the integrated circuit. The possible techniques are multi-threshold super cut-off stack (MTSCStack), dual-threshold transistor stacking (DTTS), and bulk-driven [7]-[9]. These techniques were then studied and applied in the design of the comparator circuit [10] and the details are presented in the following section.

2. RESEARCH METHOD

This section provides the circuit schematic of the chosen five circuits for discussion out of eight combinations used for this study. The eight combinations consist of a range of one to three chosen techniques combined into one circuit.

2.1. Conventional comparator

In this project, a 3-stage comparator utilizing a 2-stage CMOS operational amplifier (op-amp) with the output inverter is used. Figure 1 shows a circuit of the reference (main) comparator used in this study [9], [10]. The circuit provides a high speed with moderate power consumption and it is easier to be optimized due to its simple architecture.

The first stage of the conventional comparator is the NMOS differential pair which are NM1 and NM2. The differential pair is driven by tail current transistor NM5. An NMOS differential is chosen because the NMOS transistor has higher mobility compared to the PMOS transistor. Besides, the NMOS transistor also more efficient as conductivity is proportional to mobility. As the mobility of the carriers in an NMOS is approximately 2 to 3 times higher than PMOS, the PMOS must be 2 to 3 times the size of the NMOS. Therefore, the length of PM3 and PM4 is 0.26- μm in which twice the value of NM1 and NM2. Input voltage (V_{IN}) and reference voltage (V_{REF}) are applied to transistor NM1 and NM2 respectively. The range of input voltage applied is from 0V to 0.9 V and the reference voltage is set to 0.45 V based on (1). The bias voltage of the transistor NM5 which acts as the tail current transistor is 0.35 V. When the applied bias is slightly less than V_{TH} the NMOS operates in a subthreshold region where the channel beneath the gate is weakly inverted. Equation (2) was used to determine the size of the tail-current transistor NM5 and bias-current, I_{BIAS} was set as 3 μA . The transistor length was 130-nm and the assumption was made where V_{DSAT} is 0.5 V. The transistor is set to be in the saturation to experience a stable and higher gain.

$$V_{ref} = \frac{1}{2}V_{dd} \quad (1)$$

$$I_{BIAS} = \frac{1}{2} \cdot \mu_n \cdot C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_{TH})^2 \quad (2)$$

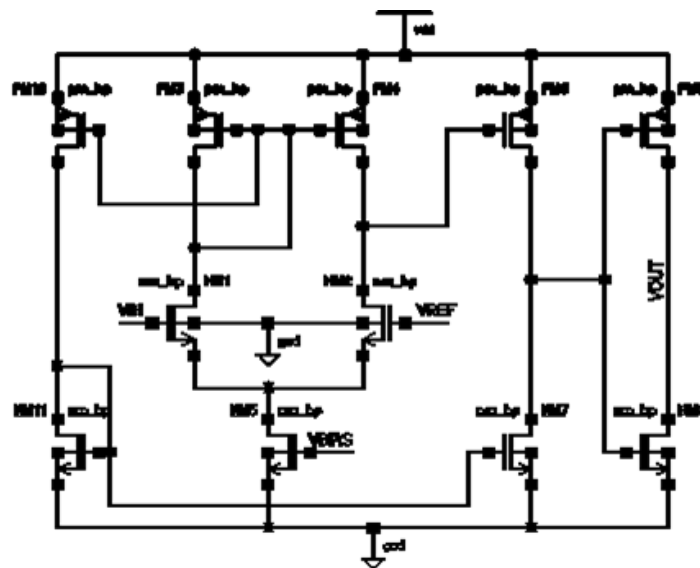


Figure 1. Conventional comparator circuit

In the second stage, a common source amplifier, PM6 provides a high and total voltage gain. Meanwhile, PM3, PM4, and PM10 are the diode loads to the differential pair. The final stage consists of PM8 and NM9, the push-pull inverter is the output driver of the comparator. The inverter is used to provide modest gain and increase the slew rate of the circuit [9]. Table 1 shows the length and width of all the transistors used in this conventional comparator circuit.

Table 1. W/L of conventional comparator

Transistor	Width (μm)	Length (μm)
NM1 - NM2	0.67	0.13
PM3 - PM4	1.33	0.26
NM5, NM7, NM9, NM11	2	0.13
PM6, PM8, PM10	2	0.13

2.2. Comparator with DTTS and MTSCStack

DTTS is used to reduce the leakage current with less impact on the propagation delay. The leakage current can be reduced when a higher threshold voltage is assigned to some resistor in the non-critical path. Therefore, the performance can be sustained due to the low threshold voltage transistor in the critical path. A high threshold voltage is applied to the sleep transistors based on the MTCMOS technique [11]-[13]. Therefore the sleep transistor turns off during standby mode. The threshold voltage can be increased by increasing the V_{SB} which is sourced to the bulk voltage based on (3) [14]-[18].

$$V_{TH} = V_{TH0} + \gamma \left[\sqrt{2\Phi_F + V_{SB}} - \sqrt{2\Phi_F} \right] \quad (3)$$

Where γ is a body-effect coefficient, Φ_F is Fermi potential, V_{SB} is a source-bulk potential difference and V_{TH0} is threshold voltage in the absence of V_{SB} .

In the power reduction technique, threshold voltage and leakage current are the major contributors and the relation between these two is stated in (4). The increasing threshold voltage leads to the reduction of sub-threshold leakage.

$$I_{SUB} = K \left(\frac{W}{L} \right) e^{\left(\frac{V_{GS} - V_{TH}}{nVT} \right)} \left(1 - e^{-\frac{V_{DS}}{VT}} \right) \quad (4)$$

where K is Boltzmann's constant ($1.38 \times 10^{-23} \text{J/K}$), W/L is the width divided by length, n is the technology parameter, V_{GS} is gate-source voltage, V_{TH} is threshold voltage, and V_{DS} is a drain-source voltage. The schematic of the comparator with the implementation of DTTS and MTSCStack technique is shown in Figure 2.

Based on Figure 2, the transistors PM8a, PM8b, NM9a, and NM9b are the sleep transistors. Transistors PM8a and NM9a are the additional transistors that build with high V_{TH} by applying different body biasing. The size of PM8a, PM8b, NM9a, and NM9b is half of the original width size due to the force stack approach. The V_{BP} and V_{BN} are set 0.75 V and 0.5 V respectively. The sleep transistor is turned on during active mode and turn off during standby mode. The leakage can be reduced much lower than the conventional comparator due to the stacking effect. This is because the two transistors in series turn off together during standby mode and no current flowing through the circuit.

The second technique which is MTSCStack is introduced to reduce the leakage power in active mode and at the same time retaining the logic state of the comparator during the idle state. Compared to the conventional circuit, there are an additional four transistors which consist of two PMOS transistors (PM12 and PM15) and two NMOS transistors (NM13 and NM14). During active mode, the sleep transistor PM12 is turned off while sleep bar transistor NM14 is turned on. Therefore the circuit operates as normal. However, the leakage current can be reduced because of the stacking effect of PM12 and NM14. While in sleep or standby mode, the sleep transistor is turned on while the sleep bar transistor is turned off. As a result, all sleep transistors turned off except PM15 and NM13 because it will give the ability to retain the logic state to the circuit.

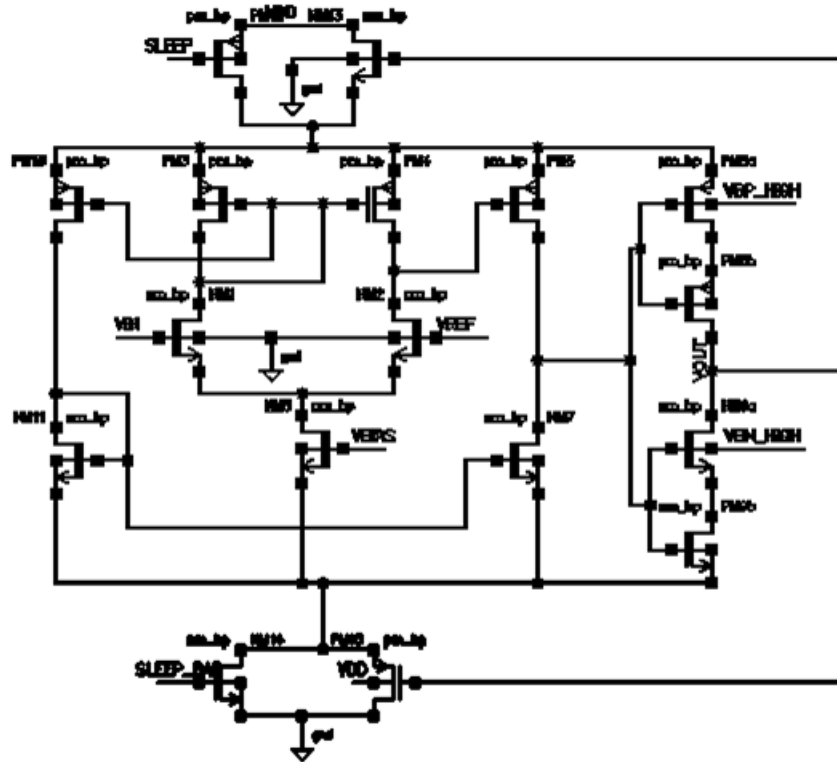


Figure 2. Comparator with DTTS and MTSCStack technique

A slightly negative gate voltage is applied to the sleep transistor to reduce the leakage current. This is because the V_{GS} will affect the sub-threshold leakage based on (4). The gate voltage for the sleep transistor and sleep bar transistor is -1.1 V and 0.78 V respectively. Transistor NM13 is designed to parallel with the PM12 sleep transistor with its source connected to VDD to maintain high value in the ideal mode. In contrast, PM15 is designed to parallel with the NM14 sleep bar transistor with its source to GND to maintain a low value in the ideal mode. Table 2 shows the width and length of all the transistors used in this circuit.

Table 2. W/L values of the comparator with DTTS and MTSCStack

Transistor	Width (μm)	Length (μm)
NM1 - NM2	0.67	0.13
PM3 - PM4	1.33	0.26
NM5, NM7, NM11, NM13, NM14	2	0.13
PM6, PM10, PM12, PM15	2	0.13
PM8a, PM8b, PM9a, PM9b	1	0.13

2.3. Comparator with DTTS and MTSCStack and bulk-driven current mirror

Comparator circuit with DTTS, MTSCStack, and bulk-driven current mirror technique applied is shown in Figure 3. The leakage power can be reduced using DTTS and MTSCStack techniques and the threshold voltage can be controlled using the bulk-driven current mirror technique.

The design structure of the bulk-driven PMOS current mirror with the bulks of PM1 and PM2 are tied together rather than the gates [19]-[22]. By using (5), the current across the MOSFET can be determined. Precaution must be taken that the value of V_{BS} is such that bulk-source junction either reverse biased or slightly forward biased with V_{BS} less than V_{TH} to ensure the negligible bulk current in the circuit. The constant bulk source is applied to get the operation current mirror of the bulk-driven circuit, PM1, and PM2 MOSFETs. To enhance the current range, the transistor pair must be in a saturation region. It is done by connecting their gates to an appropriate value of input voltage (V_{IN}) and reference voltage (V_{REF}).

$$I_D^{(sat)} = \frac{\beta}{2} (V_{GS} - V_{TH0} - \gamma \sqrt{|2\Phi_F| - V_{BS}} + \gamma \sqrt{|2\Phi_F|})^2 \quad (5)$$

where $\beta = \mu C_{ox} W/L$, μ is the mobility of the carriers, C_{ox} is gate oxide capacitance per unit area, W/L is the aspect ratio of MOSFET, Φ_F is absolute fermi potential, V_{TH0} is zero bias threshold voltage and γ is a body-effect coefficient.

Hence it is allowing for a significant rise in the available voltage headroom and reduces the total supply voltage of the circuit. An additional stage of an inverter (PM0 and NM0) is added in this circuit to invert the output since the first stage is based on PMOS bulk-driven current mirror. Table 3 shows the width and length of all the transistors used in this circuit.

Table 3. W/L values of the comparator with DTTS, MTSCStack and bulk-driven current mirror

Transistor	Width (μm)	Length (μm)
PM1 - PM2	0.67	0.13
PM3 - PM4	1.33	0.26
NM0, NM5, NM7, NM11, NM13, NM14	2	0.13
PM0, PM6, PM10, PM12, PM15	2	0.13
PM8a, PM8b, PM9a, PM9b	1	0.13

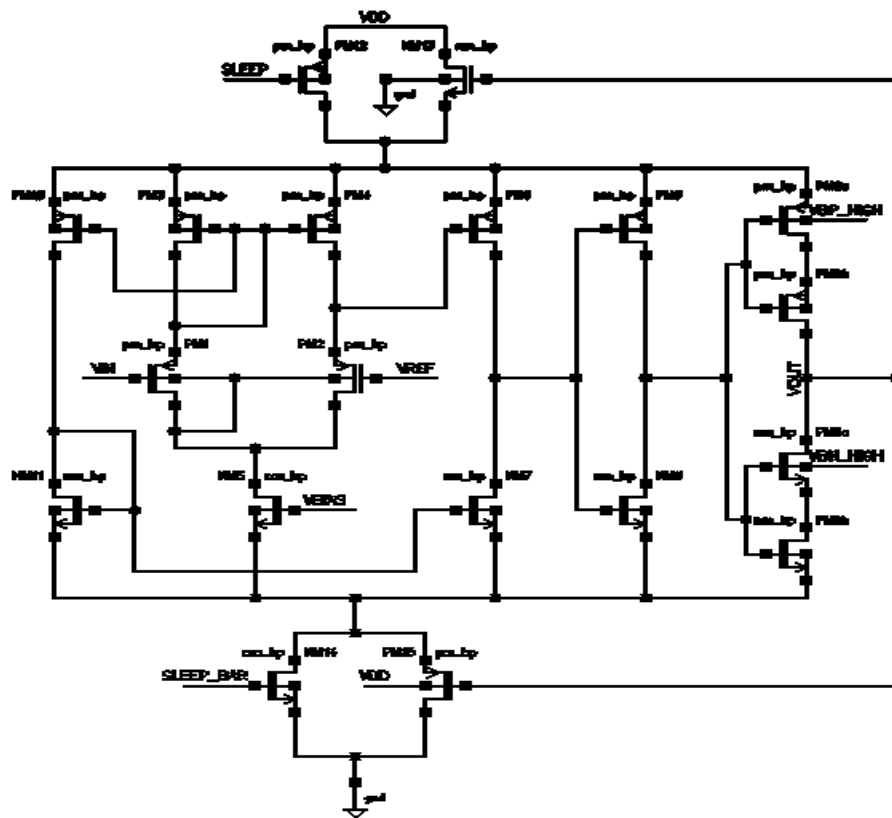


Figure 3. Comparator with DTTS, MTSCStack, and bulk-driven current mirror technique

2.4. Comparator with DTTS & MTSCStack and NMOS/PMOS bulk-driven differential pair

In these circuits, a combination of three techniques of DTTS, MTSCStack, and NMOS/PMOS bulk-driven differential pair is implemented [23]-[25]. In the bulk-driven approach, the input signals (V_{IN} and reference voltage V_{REF}) are applied to the bulk terminals of transistors NM1 and NM2, whereas the gate terminals of these devices are biased with a V_G of 0.5 V. The channel current is modulated by the input signals applied to the bulk terminals. Figure 4 graphically shows the combination of the techniques used. For the NMOS type circuit, Figure 4(a), note that the sizing of all the transistors used in this comparator circuit is the same as in Table 2 since the components used are the same. For the PMOS type circuit, Figure 4(b), note that the sizing of all the transistors used in this comparator circuit is the same as in Table 3 since the components used are the same. Also, the inverter circuit is labeled as NM12 and PM18 instead of NM0 and PM0 (see Figure 3) but they are the same circuit.

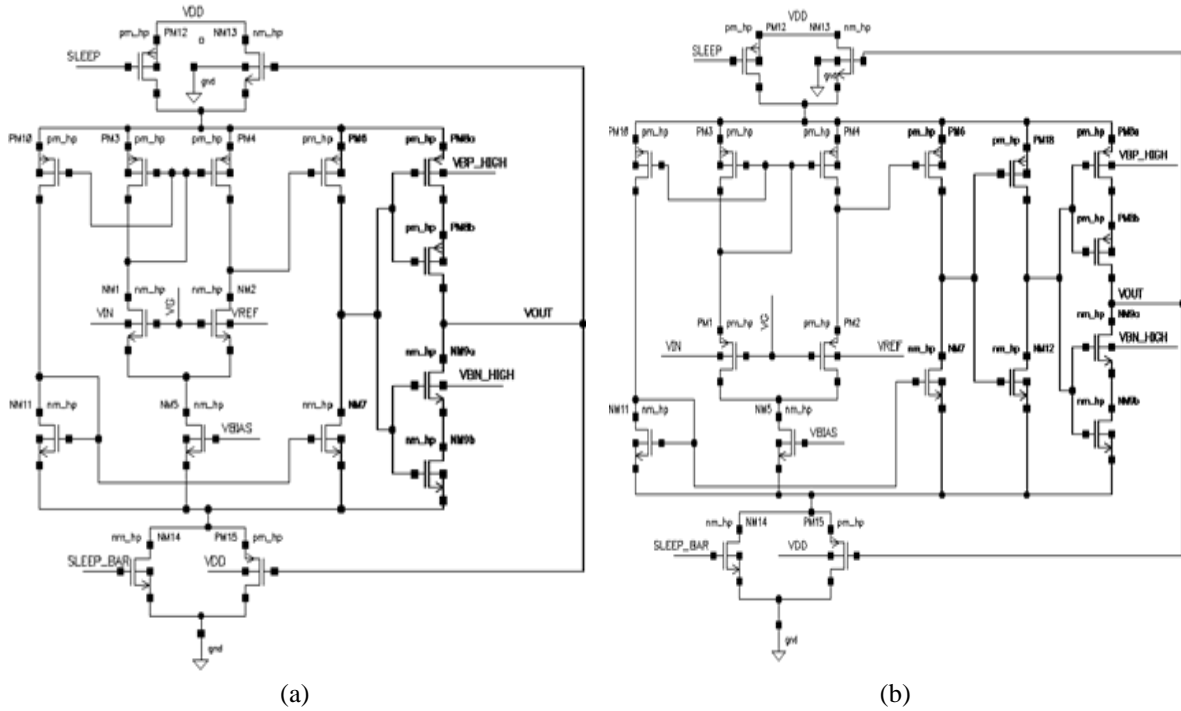


Figure 4. Comparator with DTTS, MTSCStack, and NMOS/PMOS bulk-driven differential pair techniques:
(a) NMOS bulk-driven, (b) PMOS bulk-driven

3. RESULTS AND DISCUSSION

In this section, the results of the research are explained and at the same time, a comprehensive discussion is given.

3.1. Static and dynamic characteristics

Cadence virtuoso analog design environment was used to run all the simulations. The static characteristic of comparators can be simulated by using DC analysis. During the DC analysis, V_{IN} (input voltage), has been swept to obtain the output of the comparators. The V_{IH} (upper input), V_{IL} (lower input), V_{OH} (upper output), and V_{OL} (lower output) were extracted from the transfer curve and used in the calculation of the gain by using (6). Besides, the resolution and offset of the comparator were also calculated based on (7) and (8) respectively.

$$A_v = \frac{V_{OH} - V_{OL}}{V_{IH} - V_{IL}} \quad (6)$$

$$Resolution = V_{IH} - V_{IL} \quad (7)$$

$$Offset = V_{IH} - \text{intersection curve with } V_{REF} \quad (8)$$

The DC response and transient response of one of the comparators are shown in Figure 5. Table 4 shows the mentioned static parameters for all the combinations of the comparators. It shows that the performance of all comparators is comparable.

For dynamic characteristics, transient analysis, with one cycle has been used to get the propagation delay. Pulse signal has been used as the input signal. The difference of input and output signal at 50% transition of logic 0 to logic 1 gives the calculation of the delay. From the transient response in Figure 5(b), the delay for each design was calculated. Table 5 shows the propagation delays of all comparators. It is observed that the lowest delay is obtained from the conventional comparator, while the highest delay was coming from the comparator with MTSCStack, DTTS, and PMOS bulk-driven differential pair. The results also show that the comparators with PMOS transistors experience the worst delay i.e., a comparator with PMOS bulk-driven differential pair and comparator with MTSCStack, DTTS, and PMOS bulk-driven differential pair.

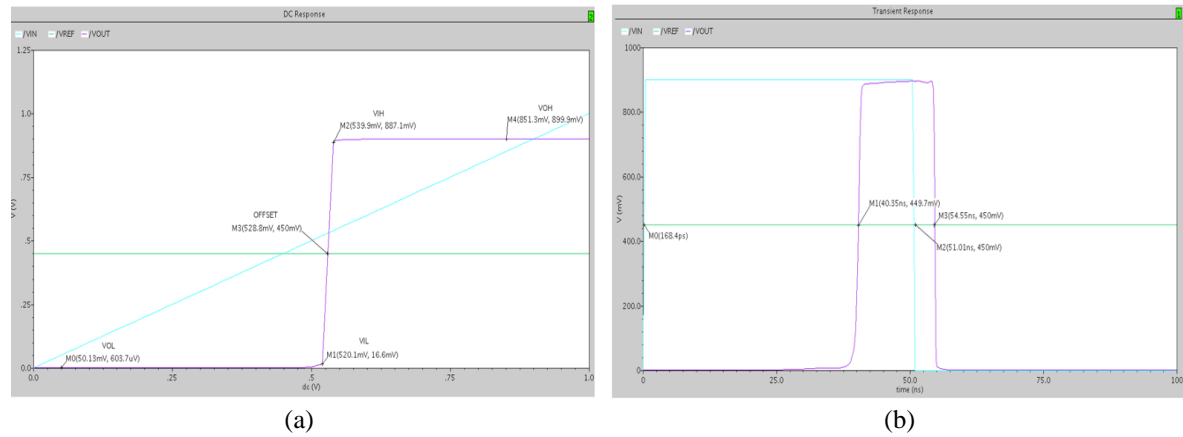


Figure 5. Results of the comparator with MTSCStack and DTTS and PMOS bulk-driven differential pair: (a) DC response, (b) Transient response

Table 4. Static characteristic

Comparator	Offset (mV)	Resolution (mV)	Voltage gain
Conventional comparator	10.3	20.0	40.1
Comparator with MTSCStack and DTTS	11.2	21.2	37.8
Comparator with bulk-driven current mirror	11.2	21.3	37.6
Comparator with NMOS bulk-driven differential pair	9.6	19.8	40.5
Comparator with PMOS bulk-driven differential pair	10.2	19.9	40.3
Comparator with MTSCStack and DTTS and bulk-driven current mirror	11.3	21.3	37.6
Comparator with MTSCStack and DTTS and NMOS bulk-driven differential pair	10.3	20.3	39.5
Comparator with MTSCStack and DTTS and PMOS bulk-driven differential pair	11.1	19.8	40.5

Table 5. Propagation delay

Comparator	Propagation delay (ns)
Conventional comparator	2.03
Comparator with MTSCStack and DTTS	2.34
Comparator with bulk-driven current mirror	4.58
Comparator with NMOS bulk-driven differential pair	2.37
Comparator with PMOS bulk-driven differential pair	20.98
Comparator with MTSCStack and DTTS and bulk-driven current mirror	6.70
Comparator with MTSCStack and DTTS and NMOS bulk-driven differential pair	2.80
Comparator with MTSCStack and DTTS and PMOS bulk-driven differential pair	21.86

3.2. Power consumption

Pulse input signal has been used at the input when getting the dynamic power, recorded when there was a switching activity. The dynamic power of a comparator is the difference between total power consumption and static power. On the opposite, a static DC voltage has been applied as an input signal when getting a static power, produced by the leakage current that happened in a transistor. The supply voltage used was 0.9 V because it is the most suitable value for obtaining stable power consumption and propagation delay. If the supply voltage assigned is higher, the propagation delay will be lower and power consumption will be higher. Since the objective of the work is to design a low power comparator, the low power supply was chosen.

Figure 6 shows the results of the power consumption for the comparators. Figure 6(a) shows conventional comparator and comparator with MTSCStack and DTTS have very low static power compared to the others. For dynamic power, a comparator with MTSCStack, DTTS and PMOS, or NMOS bulk-driven differential pair have shown that there is a very significant reduction of dynamic power compared to conventional comparator or comparator with MTSCStack and DTTS. However, the low power reduction achieved at the expense of higher propagation delay compared to conventional comparator as can be observed in Table 5. Figure 6(b) shows the total power consumption of the comparators.

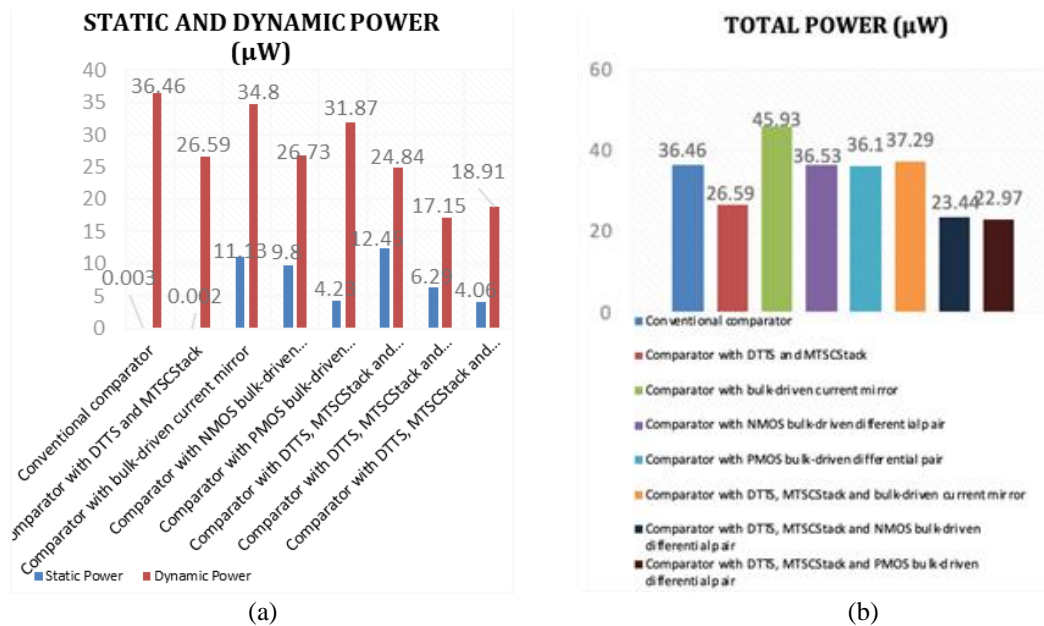


Figure 6. Power consumption of the comparators: (a) Static and dynamic power, (b) Total power

4. CONCLUSION

In this work, power reduction methods or techniques are known as MTSCStack, DTTS, bulk-driven current mirror, NMOS, and PMOS bulk-driven differential pair were studied. Though MTSCStack and DTTS were often used in digital circuits previously, this work has shown that they are also fit in analog circuits. However, compared to the reference comparator, proposed comparators relatively, have higher propagation delay. These factors will slightly influence the speed performance of the comparators.

Nonetheless, this work has proved that out of seven proposed comparators, the combination of MTSCStack, DTTS, and NMOS bulk-driven differential pair showed the best performance of low power analog circuit in general and comparator in specific without compromising the other parameters of the comparator such as propagation delay, offset, and resolution.

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REFERENCES

- [1] A. Firdous, M. Anand, and B. Rajan, "Design and implementation of enhanced leakage power reduction technique in CMOS VLSI circuits," *International Journal of Applied Engineering Research*, vol.12, no. 2, pp. 155-160, 2017.
- [2] K. Sridhara, G. S. Biradar and R. Yanamshetti, "Subthreshold leakage power reduction in VLSI circuits: A survey," *2016 International Conference on Communication and Signal Processing (ICCSP)*, 2016, pp. 1120-1124, doi: 10.1109/ICCSP.2016.7754326.
- [3] W. R. W. Ahmad, S. L. M. Hassan, I. S. A. Halim, N. E. Abdullah and I. Mazlan, "High speed with low power folding and interpolating ADC using two types of comparator in CMOS 0.18μm technology," *2012 IEEE Symposium on Humanities, Science and Engineering Research*, 2012, pp. 715-720, doi: 10.1109/SHUSER.2012.6268907.
- [4] J. Lu and J. Holleman, "A low-power high-precision comparator with time-domain bulk-tuned offset cancellation," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, no. 5, pp. 1158-1167, May 2013, doi: 10.1109/TCSI.2013.2239175.
- [5] N. B. Romli, K. N. Minhad, M. B. I. Reaz and MD. S. Amin, "An Overview of Power Dissipation And Control Techniques In CMOS Technology," *Journal of Engineering Science and Technology*, vol. 10, no. 3, pp. 364-382, 2015.
- [6] G. Karimi and A. Alimoradi, "MTSCStack: An effective technique to decrease leakage power in VLSI circuits," *2010 International Conference on Electronic Devices, Systems and Applications*, 2010, pp. 116-120, doi: 10.1109/ICEDSA.2010.5503090.

- [7] J. M. Carrillo, J. F. Duque-Carrillo, and G. Torelli, "Design considerations on CMOS bulk-driven differential input stages," *2012 International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD)*, 2012, pp. 85-88, doi: 10.1109/SMACD.2012.6339423.
- [8] M. Kummern, "0.4 V fully differential current conveyor using multiple-input bulk-driven MOST technique," *Microelectronics Journal*, vol. 90, pp. 96-104, 2019, doi: 10.1016/j.mejo.2019.05.019.
- [9] P. M. Krishnan and M. T. Mustaffa, "A low power comparator design for analog-to-digital converter using MTSCStack and DTTS techniques," *9th International Conference on Robotic, Vision, Signal Processing and Power Applications, Lecture Notes in Electrical Engineering*, vol. 398, pp.37-46, 2017, doi: 10.1007/978-981-10-1721-6_5.
- [10] Y. Kumar, "Analysis and design of high speed low power comparator in ADC," *International Journal of Recent Research Aspects*, vol. 2, no. 3, pp. 9-15, 2015.
- [11] S. M. Sharroush and Y. S. Abdalla, "Optimum sizing of the sleep transistor in MTCMOS technology," *AEU - International Journal of Electronics and Communications*, vol. 138, p. 153882, 2021, doi: 10.1016/j.aeue.2021.153882.
- [12] H. You, J. Yuan, W. Tang, Z. Yu and S. Qiao, "A low-power high-speed sense-amplifier-based flip-flop in 55 nm MTCMOS," *Electronics*, vol. 9, no. 5, p. 802, 2020, doi: 10.3390/electronics9050802.
- [13] M. Manoranjani and T. Ravi, "Multithreshold CMOS sleep stack and logic stack technique for digital circuit design," *ARPJ Journal of Engineering and Applied Sciences*, vol. 10, no. 10, pp. 4550-4556, 2015.
- [14] S. Radfar, *et al.*, "A sub-threshold differential CMOS Schmitt trigger with adjustable hysteresis based on body bias technique," *Electronics*, vol. 9, no. 5, p. 806, 2020, doi: 10.3390/electronics9050806.
- [15] F. Soleymani, Y. Bastan, P. Amiri and M. H. Maghami, "A 0.3–1.4 GHz inductorless CMOS variable gain LNA based on the inverter cell and self-forward-body-bias technique," *AEU-International Journal of Electronics and Communications*, vol. 113, p. 152974, 2020, doi: 10.1016/j.aeue.2019.152974.
- [16] N. Cheraghi Shirazi, A. Jannesari and P. Torkzadeh, "Self-start-up fully integrated DC-DC step-up converter using body biasing technique for energy harvesting applications," *AEU-International Journal of Electronics and Communications*, vol. 95, pp. 24-35, 2018, doi: 10.1016/j.aeue.2018.07.033.
- [17] H. Guo, J. Feng and Y. Lyu, "Highly-linear wide-range voltage-controlled delay element with body bias technique," *Microelectronics Journal*, vol. 96, p. 104695, 2020, doi: 10.1016/j.mejo.2019.104695.
- [18] P. Pritty, M. Kumar and M. Zunairah, "A body bias technique for low power full adder using XOR gate and pseudo NMOS transistor," *International Journal of Reconfigurable and Embedded Systems*, vol. 8, no. 3, pp. 162-168, 2019, doi: 10.11591/ijres.v8.i3.pp162-168.
- [19] N. Minwong, K. Sooksood and A. Thanachayanont, "A low dropout voltage regulated bulk-driven CMOS Current Mirror," *Procedia Computer Science*, vol. 86, pp. 95-99, 2016, doi: 10.1016/j.procs.2016.05.024.
- [20] S. Bano, G. B. Narejo and S. M. U. Ali Shah, "Power efficient fully differential bulk driven OTA for portable biomedical application," *Electronics*, vol. 7, no. 3, p. 41, 2018, doi: 10.3390/electronics7030041.
- [21] M. Kummern, F. Khateb and T. Kulej, "Extremely low-voltage low-power differential difference current conveyor using multiple-input bulk-driven technique," *AEU-International Journal of Electronics and Communications*, vol. 123, p. 153310, 2020, doi 10.1016/j.aeue.2020.153310.
- [22] Y. Wang, Q. Zhang, X. Zhao and L. Dong, "An enhanced bulk-driven OTA with high transconductance against CMOS scaling," *AEU-International Journal of Electronics and Communications*, vol. 130, p. 153581, 2021, doi: 10.1016/j.aeue.2020.153581.
- [23] A. Nejati, S. Radfar, P. Amiri and M. H. Maghami, "A bulk-driven differential CMOS Schmitt trigger with adjustable hysteresis for ultra-low-voltage operation," *Microelectronics Journal*, vol. 114, p. 105129, 2021, doi: 10.1016/j.mejo.2021.105129.
- [24] A. Nejati, Y. Bastan, P. Amiri and M. Maghami, "A low-voltage bulk-driven Differential CMOS Schmitt trigger with tunable hysteresis," *Journal of Circuits, Systems and Computers*, vol. 28, no. 7, p. 1920004, 2019, doi: 10.1142/S0218126619200044.
- [25] A. Kaur and E. P. S. Jassal, "Optimization and performance analysis of bulk-driven differential amplifier," *Journal of Engineering Research and Applications*, vol. 4, no. 4, pp. 352-356, 2014.

BIOGRAPHIES OF AUTHOR



Mohd Tafir Mustaffa received his B. Eng degree in electrical and electronic engineering from Universiti Sains Malaysia (USM), Penang in 2000. He was awarded a master's degree (M. Eng. Sc) in computer and microelectronic engineering from Victoria University, Australia in 2005 and was officially completed his Ph.D. degree in electrical engineering specializing in radio frequency integrated circuit (RFIC) in September 2009. He served as a system engineer at Data Acquisition System (M) Sdn. Bhd. and tutor in USM. He is now a senior lecturer at the School of Electrical and Electronic Engineering, USM, Engineering Campus. Dr. Mohd Tafir Mustaffa is a Senior Member of IEEE. He is actively involved with IEEE Circuits and Systems Society for the last few years as a committee member. He is the author and co-author of close to 50 technical papers in conferences and journals, books, and book chapters. He was a recipient of the IETE J C Bose Memorial Award in 2017. He is currently involved in the research of analog IC, RFIC, and RF MEMS design.