

Monolayer and bilayer graphene field effect transistor using Verilog-A

Nayana G. H., Vimala P.

Department of Electronics and Communication Engineering, Dayananda Sagar College of Engineering, Bengaluru, India

Article Info

Article history:

Received Aug 30, 2020

Revised Jan 26, 2021

Accepted Feb 15, 2021

Keywords:

Ballistic
Drift-diffusion
Field effect transistor
Verilog-A

ABSTRACT

Monolayer and bilayer graphene field effect transistor modeling is presented in this paper. The transport model incorporated, works well for both drift diffusive and ballistic conditions. The validity of the model was checked for various device dimensions and bias voltages. Performance parameters affecting operation of graphene field effect transistor in various region of operation are optimized. Model was developed to verify transfer characteristics for monolayer and bilayer graphene field effect transistor. Results obtained prove the ambipolar property in Graphene. MATLAB is used for numerical modeling for systematic performance evaluation of parameters in graphene. The tool used to simulate the characteristics is cadence Verilog-A which describe analog component structure.

This is an open access article under the [CC BY-SA](https://creativecommons.org/licenses/by-sa/4.0/) license.



Corresponding Author:

Nayana G. H.
Department of Electronics and Communication Engineering
Dayananda Sagar College of Engineering
Bengaluru, India
Email: nayana.gh.0109@gmail.com

1. INTRODUCTION

Over decades dynamic evolution is witnessed in semiconductor electronics industry following Moore's law. Continuous scaling of Silicon in MOSFETs was the key to this success, but further scaling leads to short channel effects reducing its efficiency. International roadmap of semiconductor (ITRS) has indicated that graphene as a potential material for future electronic devices. Graphene an allotrope of carbon with sp² hybridization is a zero band-gap material. Two-dimensional era started when Geim and Novoselov in 2004 were able to introduce this wonder material graphene detaching from graphite using a scotch tape method [1]. This path changing material lead to Nobel Prize in 2010 for the scientists who discovered it and gave a lot of impetus to the scientific community to look beyond silicon and germanium as materials in semiconductor industry. Since its inception in 2004, many researchers have tried to explore the potential capabilities of graphene. High carrier mobility, high carrier concentration and high velocity saturation are the exceptional properties of graphene which can outperform silicon in many higher end applications. But some of the limitations such as zero band-gap will result in lower Ion/Ioff, leading to lesser digital applications.

Any material's success depends on integration process in semiconductor industry which is complex and expensive. So, evaluating its performance in process, device and circuit level is a key requirement. We propose a numerical model to optimize performance parameters and also an analytical model approach to assess its capability accurately. We also prove that graphene has the capability of performing well at shorter channel lengths without affecting bipolarity nature.

Graphene is an excellent option beyond Silicon [2-4] for high frequency electronic devices where turning off the device is not a prime concern. The potential of graphene for radio frequency devices is well

demonstrated at shorter channel length and the intrinsic cutoff frequency as high as Giga hertz is demonstrated [5-7]. Capability of graphene field effect transistor for digital application is also emphasized [8, 9]. There are physical models developed from device physics for GFETs [10, 11]. The first Physics based model [12] provides a qualitative information about thermionic and tunneling transport in GFETs. The Drift-Diffusion model presented in [13, 14] shows kink effect in the characteristics of GFETs, Quasi analytical approach is employed for GFETs which has a large area [15]. Virtual source model is also developed for graphene field effect transistors [16], Large signal model is successfully implemented in [17, 18]. The main contribution for this work is from paper [19], where a compact model based on physics is developed using the concept of virtual source method. Carrier transport in both drift diffusion and ballistic is modeled considering Verilog-A to find the simulation results. This is done for a monolayer graphene field effect transistor. We also have implemented a bilayer graphene field effect transistor and the main contribution is from paper [20]. An accurate compact model is developed for a bilayer graphene FET. The model is based upon 2D density of states and is implemented in Verilog-A. This paper is organized as follows. Research method is discussed in Section II followed by results and discussion in Section III. Conclusion is provided in Section IV.

2. RESEARCH METHOD

The methodology followed for drain current modeling is shown in Figure 1. The steps followed are extraction of parameters using atomistic modeling [21] using MATLAB and then device modeling is performed using carrier transport mechanisms. Finally drain current model for monolayer and bilayer is developed and implemented in Verilog-A of cadence.

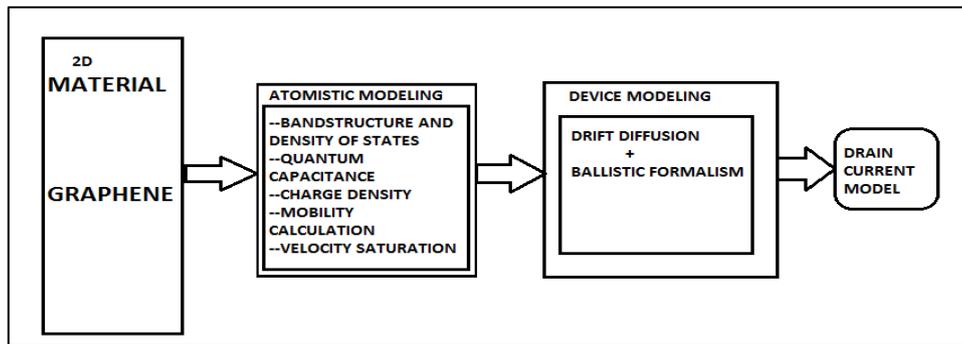


Figure 1. Bottom up approach methodology for modeling graphene field effect transistor

2.1. Atomistic modeling

2.1.1. Bandstructure and density of states

The structural energy band of conventional semiconductor is parabolic whereas that of graphene is cone shaped. It can also be seen in conventional semiconductors that there is a band-gap of size E_g between the valence and conduction band whereas graphene has a zero band gap as shown in the Figure 2. However, band-gap can be induced in many types of graphene based devices such as Bi-layer GFET and graphene Nano-Ribbon.

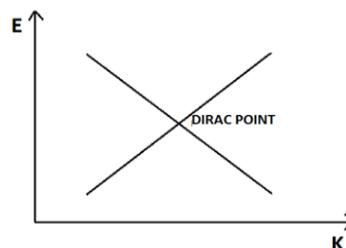


Figure 2. Bandstructure of graphene

Density of States(DoS) for graphene is different as it a two dimensional material and it is given by

$$D(E) = \frac{2|E - E_{cv}|}{\pi(\hbar v_f)^2} \quad (1)$$

Where D(E) is Density of States, \hbar is reduced plancks constant and v_f is Fermi Velocity.

2.1.2. Quantum capacitance

Quantum capacitance C_q is the intrinsic charge storage when a potential is applied most commonly small signal. Quantum capacitance is dependent on the channel potential which is numerically modeled and plotted using MATLAB. Exact equation of Quantum capacitance [22-23] is given by

$$C_q = \frac{2q^2 KT}{\pi(\hbar v_f)^2} \ln \left[2 \left(1 + \text{Cosh} \left(\frac{qV_{ch}}{KT} \right) \right) \right] \quad (2)$$

Approximation equation for graphene [16] used is as shown in

$$C_q = \frac{2q KT \ln(4)}{\pi(\hbar v_f)^2} \sqrt{1 + \left(\frac{qV_{ch}}{KT \ln(4)} \right)^2} \quad (3)$$

Where q is the electronic charge, KT Boltzmann constant, V_{ch} is the channel potential.

2.1.3. Charge density

Charge density is an important parameter for a semiconductor. Charge density is related to Density of States and Fermi Dirac probability and is explained in:

Electron density n is given by

$$n = \int_{E_{cv}}^{\infty} D(E) f(E) dE \quad (4)$$

Where D(E) is Density of States and $f(E)$ is a Fermi Dirac probability. Expression for electron(n) and hole density(p) is approximated as

$$n = \frac{2(KT)^2}{\pi(\hbar v_f)^2} \xi_1 \left(\frac{-qV_{ch}}{KT} \right) \quad (5)$$

$$p = \frac{2(KT)^2}{\pi(\hbar v_f)^2} \xi_1 \left(\frac{qV_{ch}}{KT} \right) \quad (6)$$

So the most important parameter modeled for a drain charge transport [24] is

$$Q_t = q(p + n) \quad (7)$$

2.1.4. Mobility calculation

The most fascinating property of graphene is its mobility. The mobility of holes is approximated with that of electrons in many works. As it is found experimentally that mobility of electrons is not equal to mobility of holes, we are considering distinct mobility. The mobility effectiveness μ_{eff} is given by.

$$\mu_{eff} = \frac{n\mu_n + p\mu_p + n_{pud}(\frac{\mu_n + \mu_p}{2})}{n + p + n_{pud}} \quad (8)$$

Where μ_n is the mobility of electrons, μ_p is the mobility of holes.

2.1.5. Velocity saturation

When a high electric field is applied to a graphene channel, the maximum drift velocity the charge carriers can attain is velocity saturation [25]. Velocity saturation is considered to be inversely proportional to channel potential and has proved to provide accurate results but at low channel potential velocity saturation is found to be extremely high.

2.2. Device modeling and developing drain current model

There are various categories to which we can classify graphene field effect transistors (GFET), starting from how graphene is prepared as either by process of exfoliation, CVD growth or epitaxial. We can also choose the type of GFET based on the applications it is used for. Large area monolayer graphene FET having zero bandgap can be used for RF applications. Logical applications require a minimum bandgap to operate; hence it is difficult to make use of monolayer GFET. So, efforts have been made to induce a bandgap between conduction band and valence band leading to other types of GFET namely Bilayer GFET and Graphene nanoribbons which can be again classified as armchair or zigzag based on its pattern.

2.2.1. Monolayer graphene field effect transistor

Carrier transport modeling is most of the times based on Drift Diffusion concept, but one of its prime limitations is that it is not valid for a short channel. At MIT, an alternate approach is developed called as virtual source concept for GFETs [19]. This type of model holds good for all regions of operation, both for unipolar and bipolar [19]. As we know that most of the times gradual channel approximation is considered, but here we rely on the charge sheet approximation, so that it is valid for large area as well as short channel. The carrier transport regime that it has to work is from drift diffusive to ballistic transport.

As per the approximation based on charge sheet, normalization by width is done for drain current, in case of MOSFET, the product of carrier velocity between the source and drain and density of charge gives the drain current [22].

$$I_d / W = Q_{ix0} V_{x0} \quad (9)$$

Where width of the channel is given by W and Q_{ix} are the concentration of electron and hole charges, V_{x0} is the carrier velocity.

The structure of monolayer GFET is shown in the Figure 3(a). On a wafer made of heavily doped silicon, a thick layer of SiO₂ is deposited, on this layer above, graphene channel is laid. As a contact to this graphene channel, source and drain electrodes are present. We know that the graphene channel conductivity depends on both holes and electrons and it can be changed by varying the voltage of back gate. The dielectric that is used for oxide of top gate is HfO₂ which controls charge density.

2.2.2. Bilayer graphene field effect transistor

The schematic structure of Bilayer GFET is as shown in Figure 3(b). Another type of GFET modeled is a dual gate Bilayer GFET. This is purely based on the physical mechanisms of graphene [20], considering both unipolar and ambipolar transport regimes. It makes use of the 2-dimensional Density of States of bilayer Graphene. The tuning mechanism is employed using back gate voltage. For Bipolar Graphene Field Effect Transistor only drift diffusive mechanism is considered.

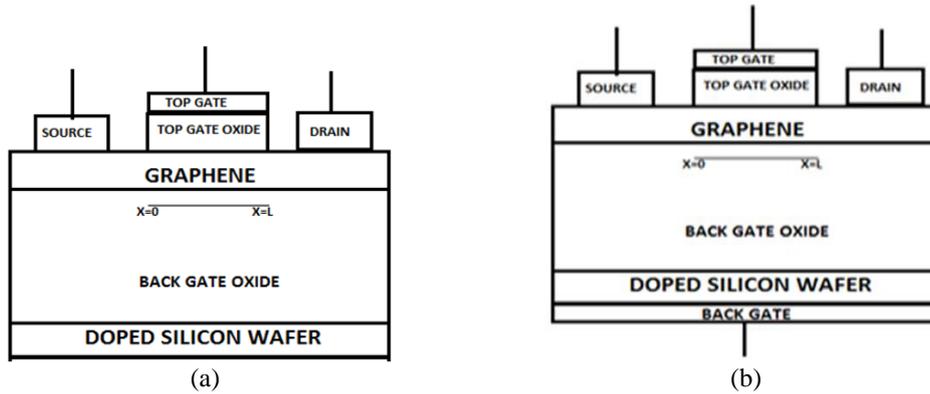


Figure 3. (a) Schematic of monolayer and (b) Bilayer graphene field effect transistor

$$I_{DS} = I_{DSp} + I_{DSn} \quad (10)$$

For the drain current, the contribution of electron (I_{DSn}) and hole concentration current (I_{DSp}) is based on the drift-diffusion equation [20].

3. RESULTS AND DISCUSSION

3.1. Quantum capacitance and charge density

Approximated and exact value of quantum capacitance for varying channel potential is observed in Figure 4. The approximated value is same as that of exact value for many values of channel potential and hence the relative error is very less indicating that approximated value can be used without affecting the accuracy. Exact equation for charge transport indicates the usage of charge density using Fermi-dirac integral. Figure 5 shows an accurate result for the operation of graphene field effect transistor without using electron hole puddles.

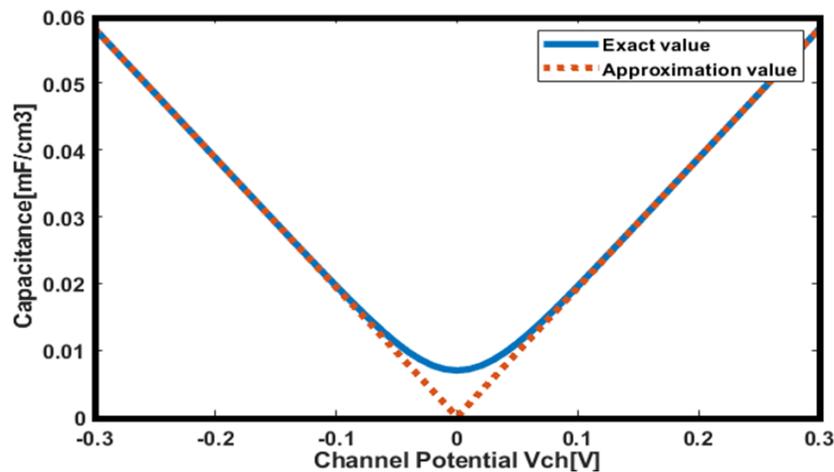


Figure 4. Quantum capacitance against varying channel potential

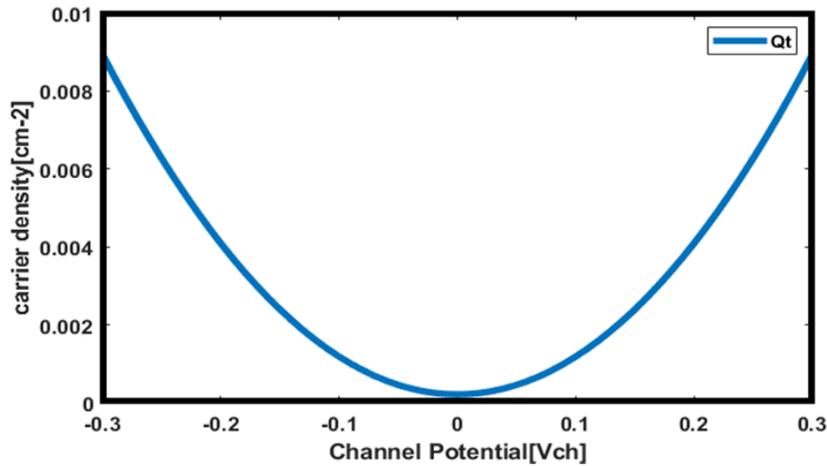


Figure 5. Charge density against varying channel potential

3.2. Transfer characteristics of monolayer graphene field effect transistor

Transfer characteristics obtained for GFET is different from that of SiMOSFET. The transfer characteristics I_D Vs V_{GS} , for various drain voltage V_{DS} for 50nm and 450nm channel length monolayer GFET is shown in Figure 6 and Figure 7 respectively. The Fermi level is in the conduction band when positive voltage V_{GS} is provided to the Graphene gate, this leads to conduction of charge carriers resulting in drain current. Whereas when the gate voltage is reduced, Fermi level is shifted downwards, and this decreases the electron concentration and hence the current. Fermi level position can neither be seen in conduction band nor in the valence band, at a certain voltage called Dirac point where the conduction and valence band encounter each other. We presume that current would be zero at this point, but it is not so, due to electron hole puddles causes residual conductivity. At the Dirac point, the conductivity type changes from n to p for negative value of V_{GS} . The current flow is because of holes instead of electrons. This phenomenon of Graphene is referred to as ambipolar conduction and this property is used in RF application. The drain current obtained for short channel 50nm is more for given V_{GS} compared to that of long channel 450nm.

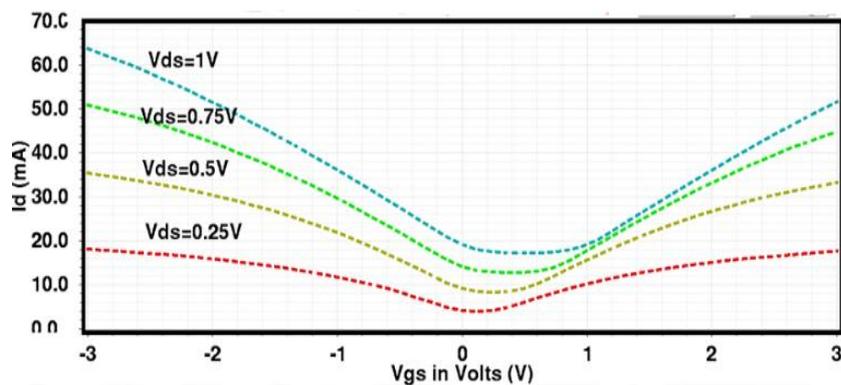


Figure 6. Transfer characteristics of I_D Vs V_{GS} GFET monolayer for a channel length $L_g=50\text{nm}$ for varying bias voltage V_{DS} from 0.25 V to 1V

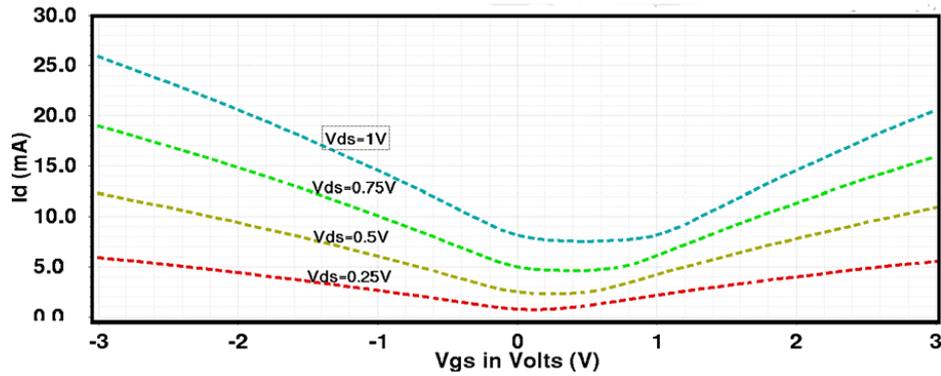


Figure 7. Transfer characteristics of I_D Vs V_{GS} GFET monolayer for a channel length $L_g=450\text{nm}$ for varying bias voltage V_{DS} from 0.25 V to 1V

3.3. Transfer characteristics of bilayer graphene field effect transistor

Inclusion of Back Gate results in better control of polarity in the device as shown in Figure 8 and Figure 9. Back Gate Bias varied is from -60 to 0V. In order to use the ambipolar property of graphene better tuning is required which is satisfied by bipolar graphene field effect transistor. For a short channel as the back gate bias is more negative, it attracts the positive charges towards it and so higher values of V_{GS} is required to obtain the current. Hence shifting of curves for various Back gate voltage can be observed.

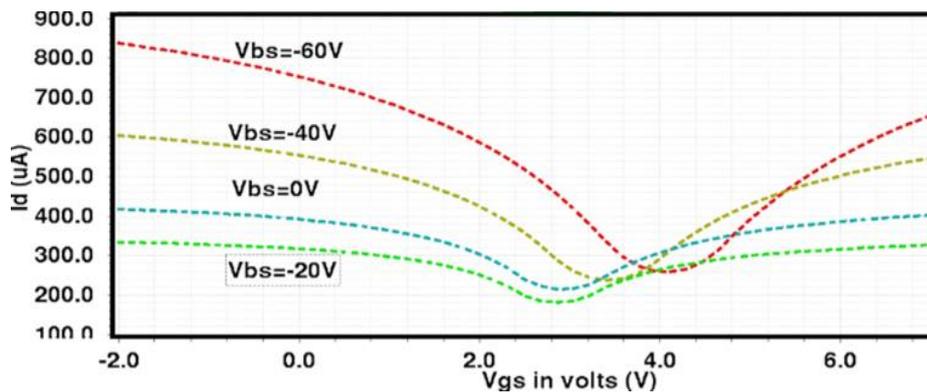


Figure 8. Transfer characteristics of I_D Vs V_{GS} GFET Bilayer for a channel length $L_g=50\text{nm}$ for varying V_{BS} from -60 to 0, $V_{DS}=2\text{V}$

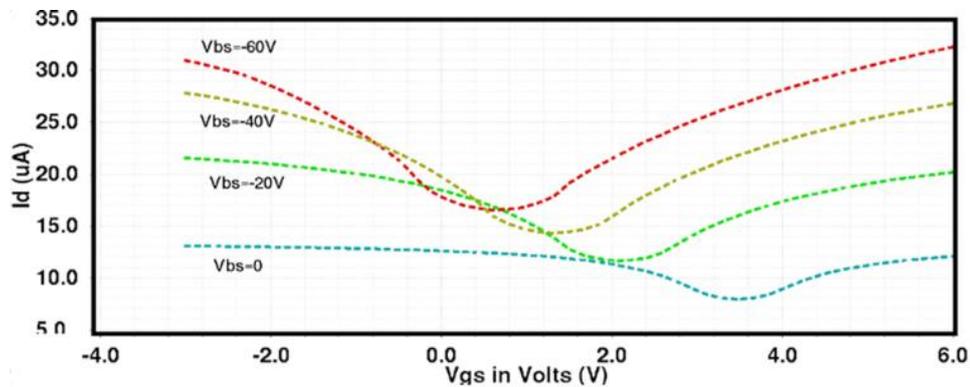


Figure 9. Transfer characteristics of I_D Vs V_{GS} GFET Bilayer for a channel length $L_g=450\text{nm}$ for varying V_{BS} from -60 to 0, $V_{DS}=2\text{V}$

4. CONCLUSION

Working of graphene field effect transistor in monolayer and bilayer is successfully modeled. Performance optimization of parameters in graphene as a channel material in Field Effect Transistor is presented. At device level the model works well for both short and large channel without degrading ambipolar property. Further work is required to show the improved current saturation and also the capability of GFET for digital applications. Comparison can also be done with other two dimensional materials.

REFERENCES

- [1] A. K. Geim and K. S. Novoselov, "The rise of graphene," *Nature Materials*, vol. 6, pp. 183–191, 2007.
- [2] F. Schwierz, "Graphene transistors: Status, prospects, and problems," *Proceedings of the IEEE*, vol. 101, no. 7, pp. 1567–1584, 2013.
- [3] H. Wang, H. Wang, A. Hsu, J. Wu, J. Kong, and T. Palacios, "Graphene-based ambipolar RF mixers," *IEEE Electron Device Lett.*, vol. 31, no. 9, pp. 906–908, 2010.
- [4] H.-Y. Chen, J. Appenzeller, "Graphene-based frequency tripler," *Nano letters*, vol. 12, no. 4, pp. 2067–2070, 2012.
- [5] Y. Wu, Yu-ming Lin, A. A. Bol, K. A. Jenkins, F. Xia, D. B. Farmer, Y. Zhu and P. Avouris., "High-frequency, scaled graphene transistors on diamond like carbon," *Nature*, vol. 472, pp. 74–78, 2011.
- [6] Y. Q. Wu, Y.-M. Lin; K. A. Jenkins, J. A. Ott, C. Dimitrakopoulos, D. B. Farmer, F. Xia, A. Grill, D. A. Antoniadis, Ph. Avouris, "RF performance of short channel graphene field-effect transistor," *2010 International Electron Devices Meeting*, 2010, pp. 9.6.1–9.6.3.
- [7] Y.-M. Lin, D. B. Farmer, K. A. Jenkins, Y. Wu, J. L. Tedesco, R. L. M.-Ward, C. R. Myers-Ward, D. K. Gaskill, C. Dimitrakopoulos, and P. Avouris, "Enhanced performance in epitaxial graphene FETs with optimized channel morphology," *IEEE Electron. Device Lett.*, vol. 32, no. 10, pp. 1343–1345, 2011.
- [8] S. K. Tiwaria, S. Sahoob, N. Wanga and A. Huczko, "Graphene research and their outputs: Status and prospect," *Journal of Science: Advanced Materials and Devices*, vol. 5, no. 1, pp. 10-29, 2020.
- [9] H. Abdollahi, R. Hooshmand, H. Owlia, "Graphene-based current mode logic circuits: a simulation study for an emerging technology," *International Journal of Electronics and Telecommunications*, vol. 65, pp. 381-388, 2019.
- [10] M. Cheli, G. Fiori, and G. Iannaccone, "A semianalytical model of bilayer graphene field effect transistor," *IEEE Transactions on Electron Devices*, vol. 56, no. 12, pp. 2979–2986, 2009.
- [11] S. Thiele and F. Schwierz, "Modeling of the steady state characteristics of large-area graphene field-effect transistors," *J. Appl. Phys.*, vol. 110, no. 3, pp. 034506-1–034506-7, 2011.
- [12] V. Ryzhii, M. Ryzhii, and T. Otsuji, "Thermionic and tunneling transport mechanisms in graphene field-effect transistors," *Physica Status Solidi (a)*, vol. 205, no. 7, pp. 1527–1533, 2008.
- [13] I. Meric, M. Y. Han, B. Ozyilmaz, P. Kim, and K. L. Shepard, "Current saturation in zero-bandgap, top-gated graphene field-effect transistors," *Nature Nanotechnology*, vol. 3, no. 11, pp. 654–659, 2008.
- [14] I. Meric, C. R. Dean, A. F. Young, N. Baklitskaya, N. J. Tremblay, C. Nuckolls, P. Kim, and K. L. Shepard, "Channel length scaling in graphene field-effect transistors studied with pulsed current-voltage measurements," *Nano Letters*, vol. 11, no. 3, pp. 1093–1097, 2011.
- [15] S. A. Thiele, J. A. Schaefer, and F. Schwierz, "Modeling of graphene metal–oxide–semiconductor field-effect transistors with gapless large area graphene channels," *Journal of Applied Physics*, vol. 107, no. 9, 2010.
- [16] H. Wang, A. Hsu, J. Kong, D. A. Antoniadis and T. Palacios, "Compact virtual-source current-voltage model for top- and back-gated graphene field-effect transistors," *IEEE Transactions on Electron Devices*, vol. 58, no. 5, pp. 1523–1533, 2011.
- [17] O. Habibpour, J. Vukusic, and J. Stake, "A large-signal graphene FET model," *IEEE Transactions on Electron Devices*, vol. 59, no. 4, pp. 968-975, 2012.
- [18] S. Frégonèse, N. Meng, H.-N. Nguyen, C. Majek, C. Maneux, H. Happy, and T. Zimmer, "Electrical compact modelling of graphene transistors," *Solid-State Electronics*, vol. 73, pp. 27 – 31, 2012.
- [19] Shaloo Rakheja, Yanqing Wu, Han Wang, Tomás Palacios, Phaedon Avouris and Dimitri A. Antoniadis., "An ambipolar virtual-source-based charge-current compact model for nanoscale graphene transistors," *IEEE Transactions On Nanotechnology*, vol. 13, no. 5, pp. 1005 - 1013, 2014.
- [20] Jorge-Daniel Aguirre-Morales, Sébastien Frégonèse, Chhandak Mukherjee, Cristell Maneux and Thomas Zimmer, "An accurate physics-based compact model for dual-gate bilayer graphene FETs," *IEEE Transactions on Electron Devices*, vol. 62, no. 12, pp. 4333-4339, 2015.
- [21] Biswapriyo Das and Santanu Mahapatra, "An atom-to-circuit modeling approach to all-2D metal–insulator–semiconductor field-effect transistors," *2D Materials and Applications*, vol. 2, no. 1, pp. 1-10, 2018.
- [22] T. Fang, A. Konar, H. Xing, and D. Jena, "Carrier statistics and quantum capacitance of graphene sheets and ribbons," *Applied Physics Letters*, vol. 91, no. 9, 2007.
- [23] J. Tian, A. Katsouraros D. Smith and Y. Hao "Graphene field-effect transistor model with improved carrier mobility analysis," *IEEE Transactions on Electron Devices*, vol. 62, no. 10, pp. 3433-3440, 2015.
- [24] K. N. Parrish, M. E. Ramón, S. K. Banerjee and Akinwande, D., "A compact model for graphene fets for linear and non-linear circuits," *IEEE 17th International Conference on Simulation of Semiconductor Processes and Devices, Denver*, 2012, pp. 75–78.
- [25] D. Jimenez and O. Moldovan, "Explicit drain-current model of graphene field-effect transistors targeting analog and radio-frequency applications," *IEEE Transactions on Electron Devices*, vol. 58, no. 11, pp. 4049-4052, 2011.

BIOGRAPHIES OF AUTHORS

Nayana G H is a Research scholar working under the guidance of Dr P Vimala in the Department of Electronics and Communication in Dayananda Sagar College of Engineering. She has around 10 years of teaching experience. Her research interests is in the field of nano scale device level modeling, VLSI Design and Embedded Systems.



Dr Vimala P is an Associate Professor in the department of Electronics and Communication, Dayananda Sagar College of Engineering, Bengaluru. Dr Vimala has more than 75+ publications in reputed international/national journals and conferences. She was awarded with “Women Scientist” scholarship for three years for her research work from Department of Science and Tecgnology, New Delhi, Government of India. Dr Vimal is currently working on 1 government funded project and guiding 5 PhD Scholars, graduate students on different research topic