

## Ultra high speed full adder for biomedical applications

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### ABSTRACT

In the field of biomedical engineering high performance CPU for digital signal processing plays a significant role. Frequency efficient circuit is a paramount requirement for the portable digital devices employing various digital processors. In this work a novel high speed one-bit 10T full adder with complemented output was described. The circuit was constructed with XOR gates which were built using two CMOS transistors. The XOR gate was constructed using 2T multiplexer circuit style. It was observed that power consumption of the designed circuit at 180nm with supply voltage 1.8V is 183.6 uW and delay was 1.809 ps whereas power consumption at 90nm with supply voltage 1.2V is 25.74 uW and delay was 8.245 ps. The observed Power Delay Product (PDP) in 180nm (at supply voltage 1.8V) is 0.33 and in 90nm (at supply voltage 1.2V) is 0.212. The work was extended by implementing a 32-bit Ripple Carry Adder (RCA) and was found that the delay at 180nm is 93.7ps and at 90nm is 198ps. The results were drawn at 180nm and also 90nm technology using CAD tool. The results say that the present work offered significant enhancement in speed and PDP compared with existing designs.

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## 1. INTRODUCTION

Advancement in VLSI technology given path to immense development in portable digital equipments like mobile handsets, tablets, PDA's etc. The compact sizes, low power, high speed of operations are the key features of these applications. However still research had been going on to improve the performances of the applications. Every time it is a challenge for the VLSI engineers to bring tradeoff among the design entities like power consumption, delay and area of VLSI chips. Since, addition is basic operation that is extensively used in most of the processors, this module plays important role in arithmetic operations like addition, multiplication, division and address formation [1, 2]. The power delay product (PDP) of the adder affects the total performance of the system. Considering this fact, the full adders are to be designed with high speed and less power [3].

Any digital processor consists of a full adder circuit at its initial levels of architecture. The full adder designs has the effect on the all the operations of processors like DSP architectures and microprocessors. The existing 28T full adder was designed using CMOS technology which consists of 28 transistors [4]. The demerits of 28 transistors CMOS full adder was its need of buffers and its high impedance and the merit is robustness against size of the transistors and scaling of voltage levels [5]. The output swing in complementary pass transistor (CPL) style full adder (32 transistors) was good but cannot be used for low

power circuits [6, 7]. The demerit of output degradation in CPL was eliminated in transmission gate adder (20 transistors). In the proposed circuit the full adder was constructed using only 10 transistors which promise full swing voltage levels at its outputs [8]. The proposed circuit produced complemented sum and carry outputs. It used basic building blocks where each block consists of 2 transistor multiplexer circuit which produced XOR output as shown in Figure 2(a). The sum and carry outputs generated were given to the inverter circuits to produce full swing complemented sum and carry outputs [9-12]. The main aim of the proposed design was to show efficiency in the delay, PDP and number of transistors compared to other existing full adders. The proposed design was implemented by varying the width of the transistors in order to achieve full voltage swing at 90 and 180nm technology using SPICE tool as shown in Table 1. The propagation delay of the proposed circuit was 8.245 ps and the power consumption was 25.74 uW at 90nm whereas propagation delay was 1.809 ps and power consumption was 183.6 uW at 180nm technology as shown in Table 2 and Table 3.

**2. RESEARCH METHOD**

The proposed design consists of five blocks: module 1, 2, 3, 4 & 5. Module 1, 2 & 3 consists of 2 transistor multiplexer circuit which produced XOR output as shown in Figure 1. Module 1, 2 & 4 generates the complemented sum and module 3 & 5 generates complemented carry. The width of the transistors in each module was varied such that the design entities like delay, area and PDP were optimized. The full logic swing of the output levels was obtained by varying the width of the transistors in the modules and placing the inverters at the outputs. These inverters will restore the logic levels resulted in complemented outputs. The carry output was constructed using 2 transistor multiplexer circuit only [13-15]. This carry output circuit consists of MP4 & MN4; the output of this carry module was connected to inverter to achieve complemented carry. The inverter connected at the output produces full swing logic levels.

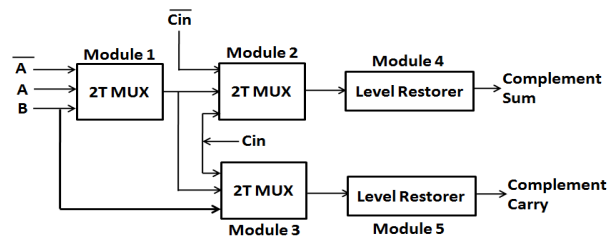


Figure 1. Block diagram of the proposed full adder design

**3. CIRCUIT OPERATION**

The module 1 consists of 2T XOR circuit which produced XOR output as shown in Figure 2(a). This 2T XOR (module 1) circuit consists of MP1 (PMOS) & MN1 (NMOS) transistors. But there was a voltage degradation problem in it. To overcome the problem the width of the transistors MP1 & MN1 are varied. Module 2 consists of 2T XOR where inputs were Cin and XOR output of module 1. The module 2 consists of MP2 & MN2 transistors whose channel widths were also varied as shown in Figure 2(b) [16, 17].

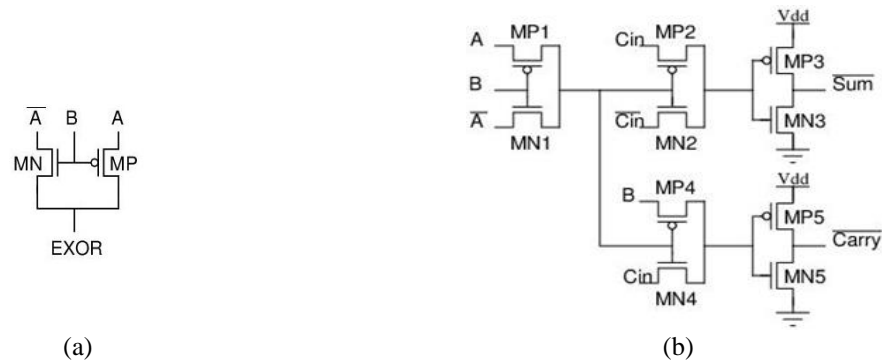


Figure 2. (a) 2T multiplexer circuit; (b) Proposed 10T fulladder

The sum output of module 2 was applied to inverter to give complemented sum output which has full swing voltage level. Module 3 also consists of 2T XOR whose inputs were Cin and B applied to MP4 & MN4 transistors where channel widths were also varied. The output of the module 3 was given to inverter which yielded complemented carry.

#### 4. PERFORMANCE OF THE PROPOSED DESIGN

The proposed full adder as shown in Figure 2(b) was designed at 90 and 180nm technology. The design entities like transistor count, average power and delay was compared with previous designs [18, 19]. It was observed that in this design the propagation delay was reduced by less the number of transistors in the circuit and also due to with of the transistors as shown in Table 1.

Full voltage swing was obtained by connecting the outputs to the voltage restoration circuit (inverter). The proposed adder was compared with other adders. The results were compared by simulating all the adders in 90 and 180nm technology. The performance parameters like PDP, power and operating speed with the supply voltage 1.8V and 1.2V are drawn at 180nm and 90nm respectively and compared with existing designs. The comparisons are shown in the Tables 2 and Table 3.

Table 1. Transistor channel widths of proposed full adder

Transistor Name	Width	Width
	(180nm Technology)	(90nm Technology)
MN1	200	120
MN2	200	120
MN3	200	120
MN4	200	120
MN5	200	120
MP1	200	120
MP2	200	120
MP3	200	120
MP4	200	120
MP5	200	120

#### 5. CALCULATION OF PROPAGATION DELAY AND POWER DISSIPATION

The propagation delay in an adder is governed by the overall speed of the entire arithmetic unit of the processors or in other words overall speed of the design can be calculated using propagation delay. In this design the carry was generated using 2T multiplexer logic circuit which acted like an XOR gate. The carry inputs (Cin) were given to this XOR gate (ie., module 2). To overcome the problem of voltage swing at the output the carry output was given to the inverter circuit which acted as level restorer. In this design the carry input was propagated through only one module ie., module 2 which acted as XOR gate as said above and hence leads to very less propagation delay [20]. However the widths of the transistors at 180nm and 90nm technology being changed to reduce the propagation delay [21].

Power consumption in VLSI circuits is due to switching of the transistors and short circuits.

The total power is given as

$$P_{total} = V_{dd} \cdot f_{clk} \cdot \sum_i V_{swing} \cdot C_{load} \cdot P_i + V_{dd} \cdot \sum_i I_{sc} + V_{dd} \cdot I_l$$

Where  $V_{dd}$  = supply voltage,

$V_{swing}$  = voltage swing at the output

$C_{load} = i$  load capacitance

$f_{clk}$  = frequency of operation

$I_{sc}$  = short circuit current

$I_l$  = leakage current.

The average power consumption was calculated for the proposed design at 180nm and 90nm technologies. The supply voltage at 180nm and 90nm technologies was 1.8v and 1.2v respectively. The widths of the transistors in the proposed design at 180nm and 90nm technologies were 200nm and 120nm respectively. The power of the design at two different technologies was given in the Tables 2 and Table 3. It was observed that average power consumption of the design at 90nm was less when compared to 180nm technology [22, 23].

Table 2. Simulation results at 180nm technology

Design	Avg Power (uW)	Delay (ns)	PDP (fJ)	Transistor Count	Reference
CMOS	6.2199	292.1	1.81683	28	[4,18]
Mirror	6.0797	281.61	1.71210	28	[18]
CPL	7.7198	183.97	1.42022	32	[5,6]
TFA	8.2491	287.1	2.36831	16	[21]
TGA	8.4719	293.9	2.8989	20	[7,8]
14T	12.721	381.7	4.85587	14	[10]
10T	14.344	132.59	1.90206	10	[24]
HPSC	6.3798	273.7	1.74615	22	[11]
Majority Based	6.3227	185.4	1.17222	--	[23]
24T	15.91	314.2	4.998	24	[1]
FA_Hybrid	5.978	252.3	1.508	24	[2]
FA_DPL	19.56	226.6	4.432	22	[19]
FA_SR-CPL	20.78	220.65	4.432	20	[19]
CMOS & TG	4.1563	224	0.931	16	[19]
<b>Proposed</b>	<b>183.6</b>	<b>0.001809</b>	<b>0.33</b>	<b>10</b>	<b>Present</b>

## 6. IMPLEMENTATION OF 32-BIT RCA

The work was extended by implementing a 32-bit RCA in 180 and 90 nm technologies. The sum and carry outputs of full adder in each stage depend on carry of previous stage which results in producing the final carry with more delay. In this circuit the delay was very less compared to other standard designs. Overall delay of the RCA adder can be minimized by implementing using the design. From the obtained results it is observed that the overall delay produced by the 32-bit RCA in 90nm technology (at 1.2V supply voltage) is 198.8ps and in180nm technology (at 1.8V supply voltage) is 93.7ps. 32-bit fulladder using 1-bit full adder multiplexer circuit as shown in Figure 3.

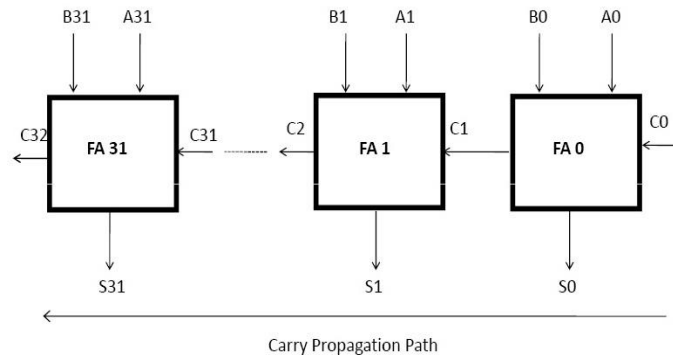


Figure 3. 32-bit fulladder using 1-bit full adder multiplexer circuit

Table 3. Simulation results at 90nm technology

Design	Avg Power (uW)	Delay (ns)	PDP (fJ)	Transistor Count	Reference
CMOS	1.5799	0.1269	0.2004	28	[4,18]
Mirror	1.5701	0.1226	0.1924	28	[18]
CPL	1.7598	0.0791	0.1392	32	[5,6]
TFA	1.7363	0.3198	0.5552	16	[21]
TGA	1.7619	0.2317	0.4082	20	[7,8]
14T	3.3297	0.3389	1.1284	14	[10]
10T	---	---	---	10	[24]
HPSC	1.56	0.2207	0.3442	22	[11]
Majority Based	1.5751	0.0939	0.1479	--	[23]
24T	7.707	0.1406	1.0836	24	[1]
FA_Hybrid	6.21	0.143	0.888	24	[2]
FA_DPL	7.34	0.254	1.864	22	[19]
FA_SR-CPL	7.4	0.167	1.235	20	[19]
CMOS & TG	1.17	0.0913	0.1074	16	[19]
<b>Proposed</b>	<b>25.74</b>	<b>0.008245</b>	<b>0.2122</b>	<b>10</b>	<b>Present</b>

**7. SIMULATION RESULTS**

In this work 15 different full adders were compared in terms of average power, delay and PDP .The simulation result of proposed 10T full adder was compared with different full adders viz 28T CMOS , 28T Mirror adder, 32T CPL, 16T TFA, 20T TGA, 14T Fulladder , 10T full adder, HPSC , majority based , 24 T Full adder, 24T FA\_Hybrid , 22T FA\_DPT, FA\_SRCPL, 16T CMOS & TG [24]. The simulation process was carried out by parametric analysis of the widths of the transistors so that proper voltage swing was obtained with less delay. The circuit design and simulation process was compromised in reducing the power consumption. However the delay of the circuit was greatly optimized when compared to all other designs. The power delay product (PDP) was also optimized due to very low propagation delay [25].

The proposed fulladder circuit was constructed using 10 transistors. The schematic of the fulladder was designed at 180nm and 90nm CMOS technologies using Cadence Virtuoso tool. Table 1 shows the widths of the transistors at 180nm and 90nm technologies. Tables 2 and 3 show the performance comparison regarding PDP, propagation delay and power consumption. From Table 2 it can be observed that the PDP was 35.4% efficient with the best design report at 180nm. Also from the Tables 2 & 3 the propagation delay was very less compared with all other circuits at 180 nm & 90nm technology as shown in Figures 5 and 6. The Figure 4 shows the comparison of PDP of various fulladders with the present work. In this paper a 32-bit RCA as shown in Figure 3 was implemented as an extension to the proposed work. In the implemented RCA only the delay was calculated. The performance evaluation was carried out at 180nm and 90nm technologies. The results shown that the overall delay produced by the 32-bit RCA in 90nm technology (at 1.2V supply voltage) is 198.8ps and in180nm technology (at 1.8V supply voltage) is 93.7ps.

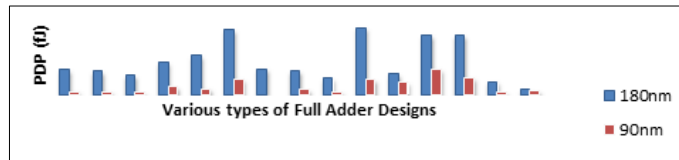


Figure 4. PDP of different full adder designs

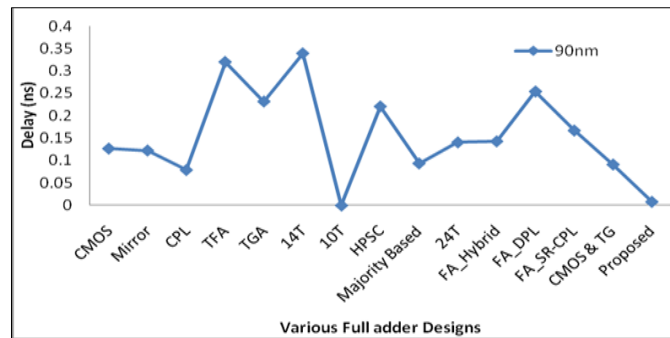


Figure 5. Delay of different full adder designs at 90nm technology

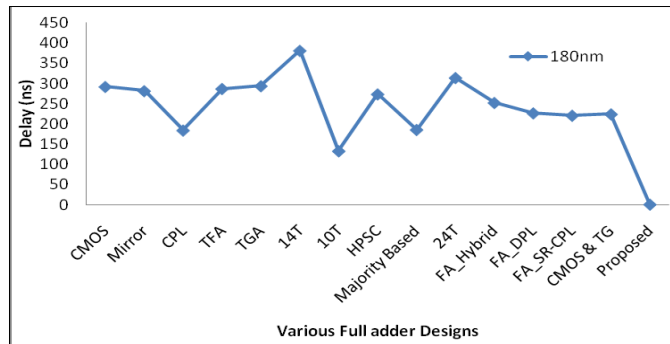


Figure 6. Comparison of delay of different full adder designs at 180nm technology

## 8. CONCLUSION

Here a delay efficient adder was introduced. The design was carried out using SPICE tool at 90 and 180nm technology. It was observed from the results that proposed circuit offers improved propagation delay & PDP. From simulations it can be said that the adder circuit is 35.4% efficient in PDP wrt best design at 180nm technology and 10.4% efficient in delay wrt best design at 90nm technology. The circuit was further used to implement a 32-bit RCA. The propagation delay of 32-bit RCA at 100MHz in 90nm technology (at 1.2V supply voltage) is 198.8ps and in 180nm technology (at 1.8V supply voltage) is 93.7ps.

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