

## Implementation of video surveillance system using embedded Blackfin processor

Sanket Dessai, Deepa Kannan, Shiva Prasad Yadav

Departement of Computer Engineering, M. S. Ramaiah University of Applied Sciences, Bangaluru, Karnataka, India

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### ABSTRACT

The video surveillance is critical system to track the people at the various places and to track and monitor the nuciencess bound to be happened. On the other side several studies have proved and showed the hit and miss nature of human intervention to spot change in a surrounding environment which increasing the designer challenges for the development of video surveillance system with the help of embedded processor. The designer faces a greater challenge to apply the principle of embedded systems and develop the system smart features with low power and cost for the required applications of VSS. System requirement specification (SRS), Hardware design document (HDD), Software design document and test procedure has been arrived and developed to achieve VSS system. Blackfin processor has high end video engines and is more suitable for development of video surveillance system (VSS). The VSS is designed and developed using ADSP BF533 Ez-kit lite board. Peripheral like parallel peripheral interface (PPI) is used to interface between camera and processor. Also, it is used for interfacing processor and TV. The master-slave communication is established between two Blackfin processors through SPORT to transfer the captured frame from camera to display on TV. Power management is also implemented to save the power of the system.

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### Corresponding Author:

Sanket Dessai

Departement of Computer Engineering

M.S. Ramaiah University of Applied Sciences

#470-P, Peenya Industrial Area, Peenya 4<sup>th</sup> Phase, Bangaluru-560058, Karnataka, India

Email: sanketdessai0808@gmail.com

## 1. INTRODUCTION

Video surveillance systems [VSS] are digital today due to advancement of processing cabailities of DSP compared to analog. Video surveillance technology is necessary and indispensable around the world for public safety and law enforcement control. The advantage of video surveillance is to monitor and provides the real-time protection for investigation and evidence preservation. Largely, it depends on the quality of the images transmitted by digital video surveillance cameras and networks. Image quality is paramount. Digital VSS provides various advantages such as viewing the video or images immediately as soon the incident captured by the VSS either near or remote locations. So, action for the captured incident will be address immediately to to apply intelligence and swift response [1-5].

VSS is a kind of any video surveillance technology which has features of enabling (videotapes, photographs or digital images) for continuous or periodic recording and viewing or monitoring of public areas. Monitoring and tracking will provide the safety for lives. A variety of applications are emerging to leverage the power of DSPs in products like video surveillance cameras and video servers. Video

surveillance is one of the major verticals that is witnessing exponential growth. The threat to security globally is the major driver for the growth in security surveillance market [5-7].

For a wide range of businesses providing security is challenging task so right from a a single camera and monitor to complex VSS with one to hundreds of cameras, operating multiple operators, and digital recorders. Movable camera covers larger area [8, 9]. The need and necessity of the market dynamic demands replacement of multi-channel video cards as compared to earlier to single-channel video cards. The market research had for to develop dual, quad, octal and even better and higher channel video count solutions. The density of video processing with lower cost and space design is achieved through the deployment of several channels of video capture on a single board. This several channel of video capture achieving increase in bandwidth for the data streams and provide better resolution on the I/O channel [5, 10, 11].

VSS are mostly and importantly used at the following areas of public place such as: waiting hall are key places where VSS is necessary to monitor for unknown people and what's the activities happening at the hall. At railway yards, railway station and other railway establishments it is necessary to have surveillance and monitoring of the employee and the passenger's movements by capturing images of the incident and have a quick analysis. At workshop it is necessary to have a close watch how one is working and associated with the instruments and machines. The places need monitoring of unknown activities for robberies and pick pocketing or criminal activities includes reservation counter, parking area, main entrance/ exit, platforms, foot over bridges. VSS made up of cameras for different application surveillance includes indoor and outdoor fixed cameras for home and industrial surveillance, indoor & outdoor P/T/Z dome cameras for applications of hospital and railways where the density of people moment is large. Indoor and outdoor IP cameras for industrial applications, single/multi channel video encoders for compression of the captured video, video management hardware and software for the development of VSS and control of the activities of the hardware through software functions. Recording servers are used to hold the huge images over servers. The other components are switches, color monitor for displaying the video for incident analysis. The other applications of VSS include airports tracking and monitoring for people movements and other smuggling and terrorist activities. Campus/university tracking and monitoring, military for defiance analysis and intrusion. Government offices for crimes monitoring and control, chemical plants for understanding the plants activities, corporate businesses for monitoring the employee activities. Banks to track the robberies and other terrorist attempt. Casinos to track people movements, hospitals need a through surveillance for the movement of the hospital staffs and the patients and their relative's movement need to be track, home Security and various others [11-14].

## 2. COMPONENT OF VIDEO SURVEILLIANCE SYSTEM

Amid advances in digital technology and society's concerns about the safety of people and property, the video surveillance market is ramping up quickly. Developers are pursuing a range of opportunities: Digital video recorder (DVR) solutions for small-to-medium enterprises and networks, digital video surveillance solutions for higher-end enterprise applications, and IP cameras for industrial and consumer use. Requirements are changing as digital video surveillance functionality comes to more end products [1, 15, 16].

- Demands in the VSS
- Higher video resolution
- Higher frame rates
- Multiple format support
- Camera display and control
- Network connectivity
- Video analytics

The VSS is designed with the help of embedded processors which include digital signal processing (DSP). The embedded system needs to be secure and protected through intellectual property while entering the video and picture for analysis. The VSS should support the embedded design cycle of low power dissipation, minimum cost, and better time to market.

The convergent MCU and DSP processing of the single core Blackfin architecture offers core frequency performance as high as 600 MHz (1200 MMACs). With support for multiple channels of audio, VGA/D1 video applications, and MPEG-4, H.264, and Windows Media® formats, Blackfin processors handle advanced video encoding and decoding in high resolution [6, 10, 16]. Because, these capabilities are implemented in software, different media formats and functions are supported simply by changing high level software. The convergent Blackfin processor speeds development by bringing together MCU and DSP functions in a single core. Development takes place using one unified set of software tools [1, 5]. Because programmability is a strong suit, changes and upgrades can be implemented quickly. An abundance of integrated peripherals saves time and cost that would otherwise be spent to build the peripheral circuit.

### 3. DESIGN AND IMPLEMENTATION

The image capturing is designed and implemented on embedded processor during the course. Further development of image capturing, video stream is designed on the Blackfin processor ADSP BF533, implemented and verified. Basically, it will convert the image stream into video frame. Master and slave concept are implemented to transfer the video frame. The captured video frame will be transferred to Television to display in the real time. The targeted of video frequency is 25fps (frame per second). It supports different video format like NTSC and PAL. The power management is implemented to save the power on embedded VSS [17-28].

#### 3.1. Block diagram of the system

The various parameters for VSS are analyzed, how it will be implemented on the embedded processor. ADSP Blackfin processor BF533 is suitable for the video application. It can be developed on BF533 at low cost and low power consumption. The VSS is designed based on available ADSP BF533 Ez-kit lite. The concept is developed and verified on the Ez-kit lite. The application video signal processing is facilitating and achieved through the parallel peripheral interface (PPI) of the Blackfin processor which is connecting to both of video encoder and video decoder in the Ez-kit lite. Hence, two boards are used to prove the real time design as master and slave transfer mode. The VSS block diagram is shown in the below Figure 1. It gives the concept of system at the top level and interconnection. Two BF533 Ez-kit lite boards are interconnected through SPORT to transfer the data. The detailed technical design is described in the next section.

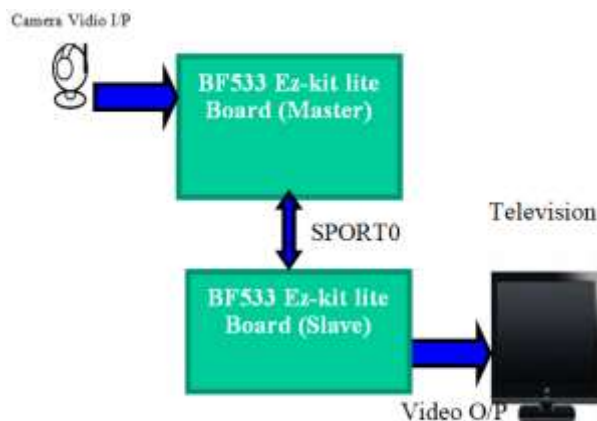


Figure 1. Block diagram of VSS

System on the BF533 Ez-kit lite board's features and how it is implemented. Also, it contains the block diagram, and flowchart representation for the design and implementation of the logic. The system architecture is discussed with the top-level block diagram. The board hardware configurations, setups and interfaces with respect to video processing are described though BF533 Ez-kit lite supports other features like Audio interface, UART. The basic configuration will be discussed for each section except Video interfaces. The Video interfaces will be discussed in detail as separate sections include memory and peripheral interfaces, power and clock signals, LED, pushbutton switch and video interfaces.

#### 3.2. Memory and peripherals interface

The instructions and data storage in ADSP-BF533 processor has stored in internal SRAM using hardware architecture. The external memory supporting for ADSP-BF533 EZ-KIT are of two types includes SDRAM and 2MB flash memory. The SDRAM size 32 Mbytes of (16Mx16-bit). The configuration of the SDRAM is performed through its three control registers of SDRAM which need to be initialized to used M48LC4M16ATG-75 16M x 16 bits (32 MB) SDRAM memory. To use the SDRAM registers are configured automatically through debugger when VisualDSP++ EZ-KIT lite session is opened in USB debug interface. SDRAM Clock frequency is configured to operate at high speed 133MHz. The address range of SDRAM memory is 0x0000 0000 0x07FF FFFF. A SDRAM is used for video frame buffer and data processing.

### 3.3. Power and clock signals

7.5Vdc Power supplies are required to operate the board. The DC power to the EZ-KIT lite board obtained the power supplies through power connector. The processor core voltage and the clock rate can be programmed on the fly through software. The input clock feed to the processor is 27 MHz and the real time clock (RTC) input of the processor is functioning at 32.768 kHz through crystal supply. The PLL registers are initialized to operate the core clock frequency at 594MHz in the design. PPI Clock can be selected either oscillator clock or video decoder clock for synchronization by Flash I/O register configuration. SPORT is initialized to operate at 160 MHz to transfer the data from master to slave.

### 3.4. Switches and I/O signals

The EZ-KIT lite is providing a support of four push buttons for switching activities and six LEDs for general- purpose IO control and testing. The labelling of the six LEDs is carried out as LED4 to LED9 and is accessible using general-purpose IO pins. The kit also provides four general purpose push buttons which are labelled as SW4 to SW7. A programmable flag (PF) input is provided for reading a status of each individual button from PF8 to PF11. When a corresponding switch is pressed-on a PF read 1, and when the switch is released, the PF reads 0. DIP switch SW9 is used to establish a connection between the push button and PF input. LED and Pushbuttons are used for power management.

### 3.5. Video interface

Video interface is divided into three major sections:

- Video input - interface with camera
- Communication-master and slave interface
- Video out-interface with TV

### 3.6. Video input

Figure 2 shows the camera interface with BF533 Ez-kit lite board. JMK Mini type camera has two outputs, video output and audio output. It is operating at 9V, 30mA. The video output from camera is connected to AVIN1 of video decoder ADV7183KST through RCA cable. The application video signal processing is facilitating and achieved through the PPI of the Blackfin processor which is connecting to both of video encoder and video decoder in the Ez-kit lite.

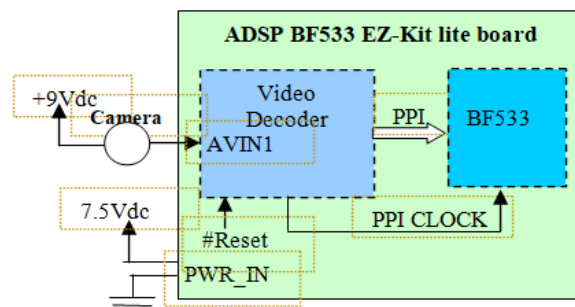


Figure 2. Showing the video input

ADV7183 video decoder has 12 analog video input and its resolution is 10-bit ADC. The video decoder converts the video signal of camera output into digital output and transfers the data to processor on PPI port. The characteristics of ADSP-BF533 processors PPI is a half-duplex, bi-directional which can accommodate up to 16 bits of data. The PPI interface is configured as input and the decoder's pixel data outputs P15-8 drive the PPI data (PPI3-0 and PF15-12). A video decoder supports different type of analog input formats; CVBS, S-video and YPrPb. VID-SEL register is used for selecting the video input format. By default, automatic video input will be selected upon reset. PF0 and PF1 are connected SDA and SCL of video decoder to initialize the register. I2C logic is emulated on PF0 and PF1.

### 3.7. Master-slave communications

Master-slave communication is established between two BF533 Ez-kit lite to transfer the captured video stream from master to slave to display on the TV through Serial Port 0 (SPORT0). The Figure 3 shows

the intercommunication connection between master and slave. The Table 1 shows the connection between master-slave communications. Master: a board which read the video data from camera and slave: a board which displays the video frame on TV.

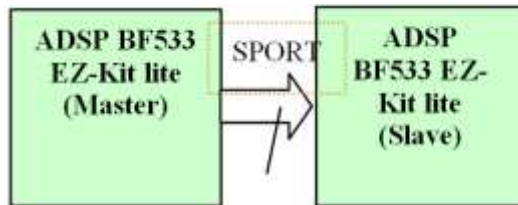


Figure 3. Master-slave communications

Table 1. Master-slave pin connections

5-pin	Signal from Master Board		Signal on Slave Board	
	Signal	Pin	Signal	Pin
1	DT0PR1	J2,38	DR0PRI	J2, 37
2	TFS0	J2, 40	RFS0	J2, 39
3	TSCLK0	J2, 42	RSLCK0	J2, 41
4	GND	J2, 88	GND	J2,87
5	NC		NC	

### 3.8. Video output

The on-board video encoder device ADV7171 is connected through PPI interface and configured as output through configuration registers. The ADV7171 encoder is having a feature for generating three Analog video channels on DAC B, DAC C, and DAC D outputs. It supports Composite, S-video and differential output. The encoder's pixel inputs are connected through PPI data connects to P7-0. The input clock requirements of encoder's PPI are 27 MHz, which is in phase with CLK IN of the processor. The encoder's synchronization signals, HSYNC and VSYNC, to be configured as inputs or outputs and the video blanking control signal is at level 1 is achieved. The HSYNC and VSYNC signals can connect the multiplexed sync pins of the processor and the on-board ADV7183 video decoder via the SW3 switch. DACB (composite video) out put is connected to TV. The Figure 4 shows the video output interface.

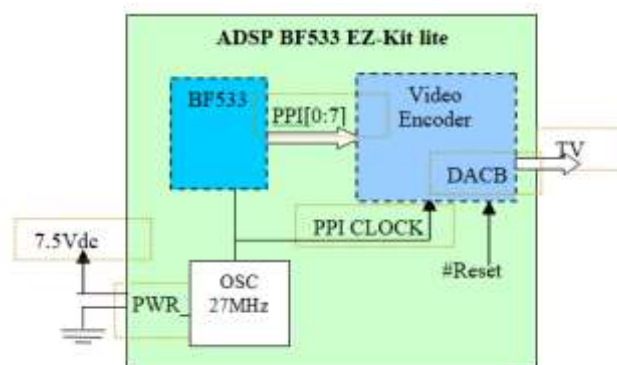


Figure 4. Video output interface

## 4. IMPLEMENTATION

PLL registers is initialized to operate at high frequency. Flags, interrupts, external bus interface unit and registers should be initialized at the starting of the program. PPI port, video decoder/encoder and video frame buffers to capture & process the video frames are also to be initialized in the main program. SDRAM, interrupts and PF pins are also initialized. The system registers are initialized for the following configurations for both master and slave operation

PLL: Initialize to operate at Core Clock – 594MHz, SCLK – 120MHz

EBIU: Write access time - 7 cycles, read access time - 11 cycles, no ARDY, hold time - 2 cycles, setup time - 3 cycles, transition time - 4 cycles and enable all memory bank

Interrupts: DMA0 for PPI & DMA2 for SPORT

SDRAM: Enable refresh mode; CAS - 2 clock cycle; RAS - 2 cycle

Flash Port A: Output direction; Flash port B – Output direction and make D0 – 1 for LED4 to be ON

NUM\_OF\_BUFFERS: 2 to allocate two set of circular buffers

#### 4.1. Master mode initialisation

In the master (collect video frames from camera), #Reset and PPI\_CLK of video decoder are connected to Flash port A. #OE is connected to Flash port C. Flash port A and C are configured as output port. Initialize all above three signals make it '1' to initialize video decoder. By default, it supports composite video input CVSB.

#### 4.2. Slave mode initialisation

In slave (display on TV), #Reset of video encoder is connected to flash port A. Initialize #Reset to '1' to reset the video encoder.

#### 4.3. Capturing and transferring video frames

PPI is initialized with the following configuration to read the data form the camera. Before PPI initializing, DMA0 must be initialized and enabled.

*\*pPPI\_FRAME - 576;*

*\*pPPI\_CONTROL - PORT\_EN / FLD\_SEL / PACK\_EN / DLEN\_8;*

DMA0 and DMA2 are initialized as descriptor mode to implement the circular buffer to avoid the data loss. The structure of the buffer has been discussed in the system initialization section. The destination Buffers are used for DMA0 descriptor to capture the frame and 'SportBuffers' is used for DMA2 descriptor to transfer the video frame to Slave mode. DMA0 is used to read the video frames from the camera and store in the circular Buffer 1. Once, the Buffer 1 is filled, DMA0 buffer and count will be initialized with Buffer 2 upon DMA0 interrupt from the destination structure. After filling Buffer 2, DMA0 will be initialized with Buffer 1 address upon DMA0 interrupt. Similarly, DMA2 is used to read from the buffers and transfer the data to Slave. The data structures of DMA flex descriptors are of variable size and the contents are loaded into DMA parameter register of the processor. In ADSP-BF533 processor the length of the descriptor is completely programmable and the sequence of registers in the descriptor (data structure) is essentially fixed (among three similar variations). The DMA channel registers are ordered so that the registers that are most reloaded per work unit are at the lowest MMR addresses. The Figure 5 shows the buffer configuration.

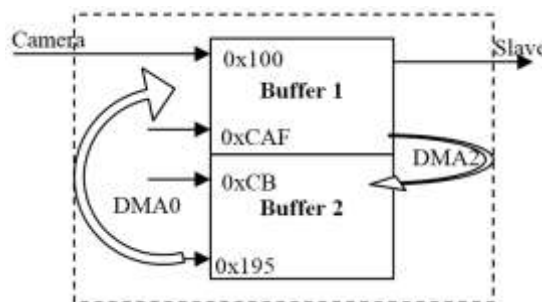


Figure 5. Video output interface

#### 4.4. Transferring the frames

SPORT0 is used to transfer the data from master to slave. SPORT0 is initialized with 32 bytes length, transmit frequency and Frame sync. It is configured for half duplex communication.

$\text{SPORTx\_TCLK frequency} = (\text{SCLK frequency}) / (2 \times (\text{SPORTx\_TCLKDIV} + 1)) = 120\text{MHz} / (2 * 0+1) = 120\text{MHz}$

$\text{SPORTxTFS frequency} = (\text{TSCLKx frequency}) / (\text{SPORTx\_TFSDIV} + 1) = 120\text{MHz} / (0+1) = 120\text{MHz}$

Hence, the transfer rate - 120MHz / 8 bit - 24MHz /byte.

#### 4.5. Displaying on TV

ADV7171 encoder will be initialized NTSC output by default. Hence, the Mode 0 will be configured for PAL format output using I2C emulation on PF pins. Mode 0 register will be initialized with '1' to support PAL output mode from default setting. After receiving video frame form the master, the blanking signal is to be inserted each & every line. The resolution has reduced to 525-line length where the camera line length is 576 to match PAL M System. The Figure 5 shows the blanking signal insertion between two lines data. It consists of EAV code, Ancillary data and SAV code.

#### 4.6. Power management

In VSS power management is most critical activities and need to develop modes and its software. The processor had four operating modes, with each mode having unique features for performance and control the power saving of the VSS. In software the power management is synchronized with the PLL control state. The status of the DPMC/PLL is determined by accessing and reading the PLL status register. The processor code can execute instructions in all modes but not in sleep and deep sleep mode. The processor can also go into idle mode in all modes, in case if the processor is in idle state, it can be awakened. The SCLK frequency is determined by the SSEL specified ratio to VCO in all modes expect Active Mode. In Sleep mode, the core clock is disabled, SCLK continues to run at the specified SSEL ratio. Video Surveillance System supports power management as this is playing important features in the market. By default, the system will be 'Full On' mode ie all are active. The power management can be selected by pressing the switch 'SW4'.

#### 5. CONCLUSIONS

The implementation has shown the feasibility of VSS on embedded processor. To implement practically, it is clear that a few issues must be addressed. The most critical one is installation and configuration. From results, it can be concluded that video surveillance system provides extended security services and implemented with one camera input and one TV output. The system supports PAL video format for both Input and output. The master-slave communication ie two processor communication is established through SPORT and transferred the video frame from master to slave board. It can be concluded that the master-slave communication established successfully and achieved the expected results.

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