

Effect of integrated power and clock networks on combinational circuits

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ABSTRACT

Reduction of power consumption is necessary in a system on chip. To achieve this, power and clock networks can be integrated. This leads to a significant reduction in power consumption in a circuit. This paper explores the effect of such a network on various combinational circuits and compares the power consumption of these circuits with conventional combinational circuits. The combinational circuits which are powered by the proposed circuit consume lesser power as compared to conventional combinational circuits.

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1. INTRODUCTION

As integrated circuits become more complex, the power consumption increases and the performance also increases. The continuous scaling of transistors and the increase in their frequency of operation has led to an increase in the overall power consumption of the chip. This increase in the complexity of the chip, in accordance with the Moore's Law, has also led to increased power densities within the Integrated circuit. A primary consumer of power on-chip is the Clock Distribution Network or the Clock Tree. Traditionally, it consumes anywhere between 30% to 50 % of the total dynamic power [1-5].

Complex integrated circuits have higher performance and lower power utilisation. With limited on-chip resources circuit designing becomes a complex task. These resources are majorly used by the three main lines of clock, ground and power in a IC. Characteristics of a circuit differ from one another and the net result is heavy utilisation of existing on-chip resources [6-8].

With limited on-chip resources it becomes necessary to design circuits which reduce the power consumption. One such circuit is an integrated power and clock distribution circuit which reduces power consumption significantly by around 60% The effectiveness of this designed circuit has been tested on various combinational circuits [9-15].

The research articles which have been published on GIPAC [1] include various methods for decreasing energy usage in circuits. Earlier literature had tried merging power and clock signals throughout the chip. The combined signals were filtered and two signals were obtained from the GIPAC [1] network.

Higher frequency signal is the clock signal and the signal with a constant dc value is V_{cc} or the power signal. Hence filtering the signals into two separate components is plausible.

Another literary work explores the possibility of eliminating the whole CDN [2], totally by merging the two networks. Newer literature on combinatorial wire-wireless clock distribution networks [3] suggests a combined circuit consisting of wired and wireless clock networks. Here circuits were designed using transmitters and receivers, and generated a clock signal which was wireless in nature. The circuit used On-Off-Keying (OOK) transceivers[3] which were used for reduction in propagation delay, increase power efficiency and reduce the complexity of the circuit. This circuit had a propagation delay lower than a normal clock circuit. The circuit also had a reduced clock skew [16-21].

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Another literary work explores the possibility of eliminating the whole CDN[2], totally by merging the two networks. As the clock network consists of a clock grid driven by a global h-tree, the metal lines implemented both horizontally and vertically would require at least four metal layers. If a similar power network is considered throughout the chip then a total of 6 metal layers would be used [22-25].

If the clock and power networks were to be merged then a total of four metal layers would be required thus saving two metal layers. Comparing typical resonant networks with these circuits, a signal generated by this circuit has a swing of 400 mV around V_{dc} . The usual resonant clock networks [11] generate a full swing clock signal from 0 to V_{DD} .

The output of the IPCDN [2] circuit can be directly connected to the power line of the entire circuit. This helps to eliminate local clock networks [9] and also the use of filter circuits. Also, the voltage swing of 400mV for the generated signal is quite low as compared to the traditional clock networks. But in a IPCDN [2] circuit needs a clock buffer to convert the generated signal into a full swing clock signal, which is necessary to operate the sequential circuits.

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2. RESEARCH METHOD

This paper explores a CMOS oscillator circuit which generates a combined signal used to run a combinational circuits. The designed circuit was tested on an inverter, NAND and a NOR gate for its effectiveness.

The designed circuit is a transistor based CMOS oscillator circuit and when simulated, the circuit [12] generates a 415mV swing. The generated signal is the *pwr_clk* signal and has a dc component along with a sinusoidal swing. The generated signal can be directly connected to run an Inverter, NAND and a NOR gate.

The designed circuit can be used to integrate power and clock network signals and can be used to drive the digital part of a chip, as the analog part of the circuit is vulnerable to fluctuations in the power supply. The proposed circuit is as shown in Figure 1. The signals generated are of opposing polarity to each other.

The generated *pwr_clk* signal can be connected directly to run an Inverter, NAND and NOR gate, but to connect to a sequential circuit, a full swing clock signal is necessary and this calls for a clock buffer circuit.

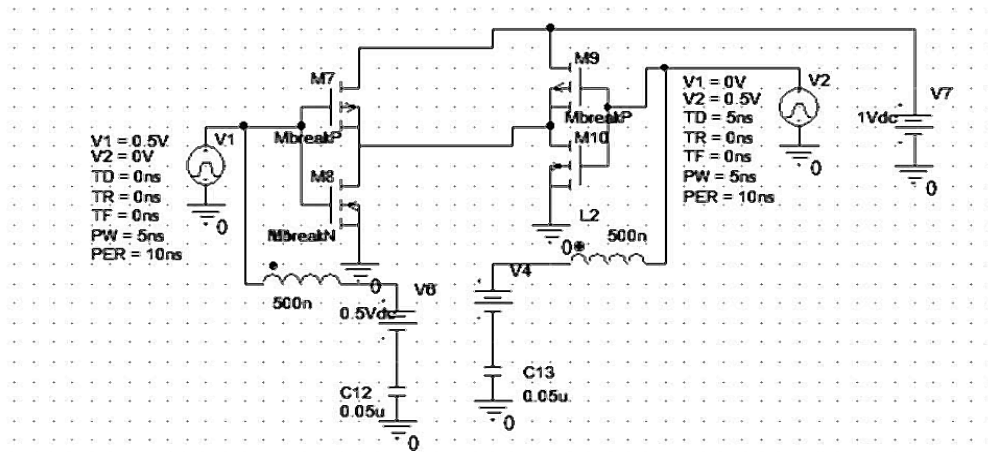


Figure 1. Proposed CMOS oscillator circuit

3. RESULTS AND DISCUSSION

To simulate the designed circuit, SPICE CIS lite version 17.2 was used. The simulation results show the circuit of a CMOS oscillator implemented on a NAND gate as shown in Figure 2. The CMOS oscillator implementation on an inverter circuit is shown in Figure 3. Figure 4 shows the implementation of a CMOS oscillator circuit on a NOR gate. Figure 5 shows the simulation output for a NAND gate. The Voltage transfer characteristics of an inverter implemented with a CMOS oscillator is shown in Figure 6. Simulation output of an inverter with a CMOS oscillator is shown in Figure 7. Figure 8 shows the simulation output of a NOR gate.

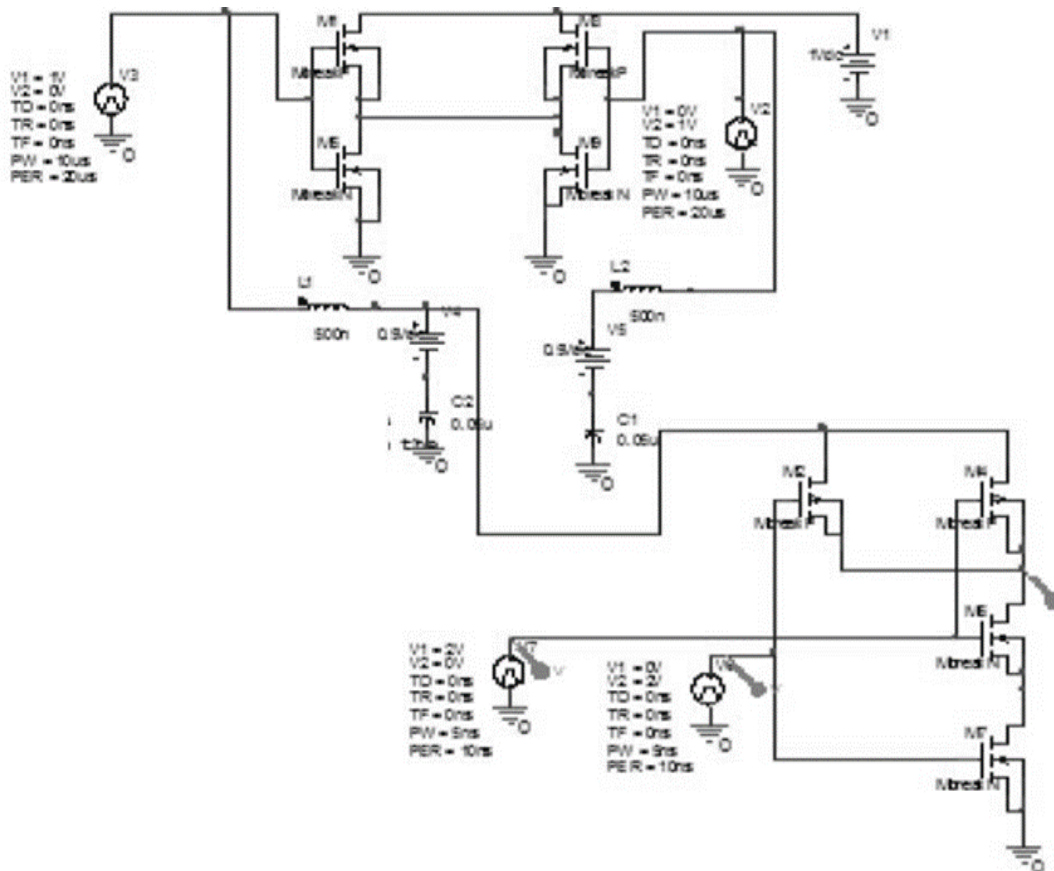


Figure 2. CMOS oscillator circuit with a NAND gate

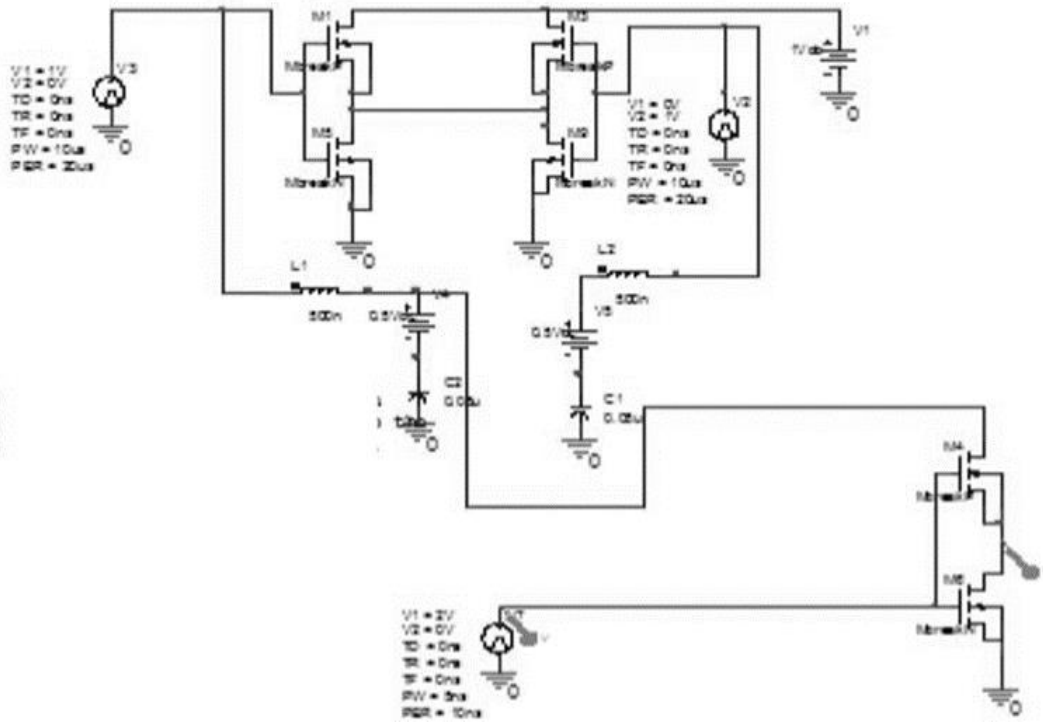


Figure 3. CMOS oscillator with a inverter

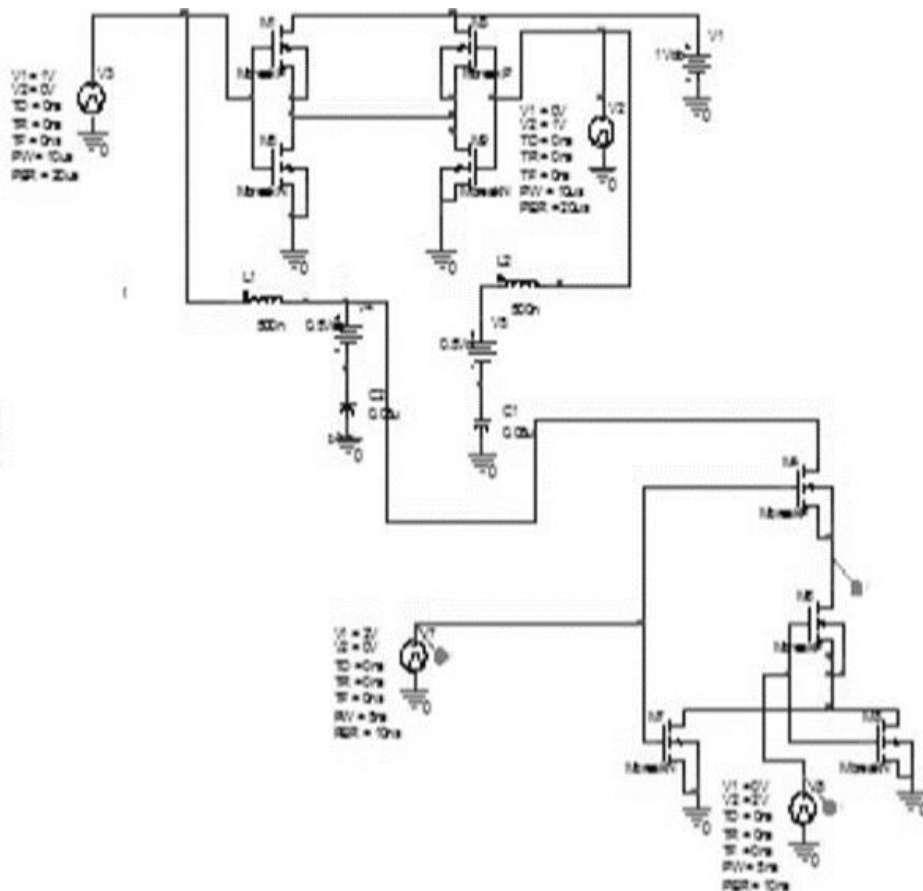


Figure 4. CMOS oscillator with a NOR gate

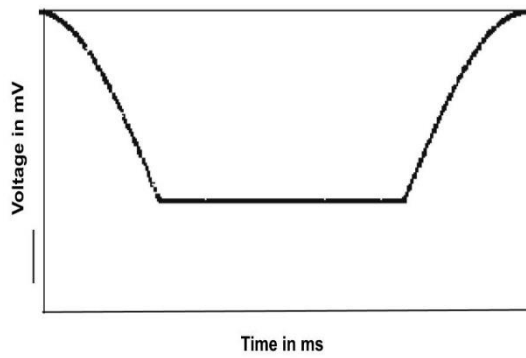


Figure 5. Simulation output for NAND gate

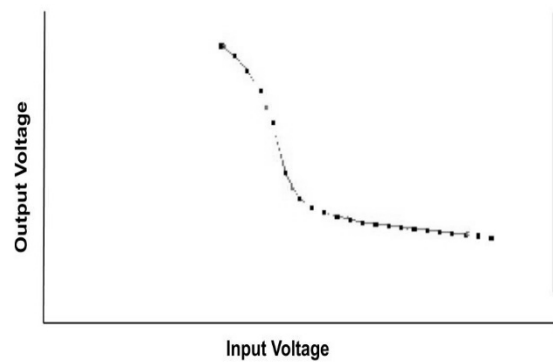


Figure 6. VTC characteristics of inverter with CMOS oscillator

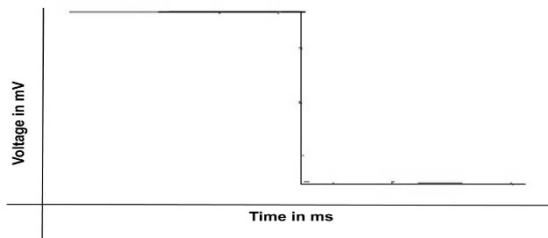


Figure 7 Simulation output of inverter with IPCDN

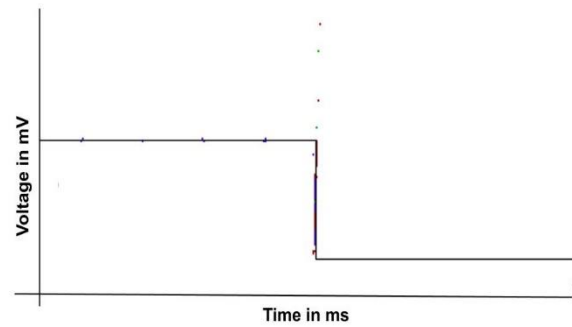


Figure 8. Simulation output of NOR gate with IPCDN

Table 1 shows the comparison of Voltage swing for GIPAC, IPCDN circuit and the designed CMOS oscillator circuit. Table 2 shows the comparison for power dissipation and transistor count for IPCDN and designed CMOS oscillator circuit. Table 3 shows comparison of power consumption for inverter with CMOS oscillator circuit and a typical inverter circuit. Table 4 shows comparison of power consumption in NAND gate with CMOS oscillator and a normal NAND gate. Table 5 shows comparison of power consumption in NOR gate with and without the CMOS oscillator circuit.

Table 1. Comparison of voltage swing for various methods

Sl.No	Methods	Voltage swing (mV)	Supply Voltage Vdd (V)
1	GIPAC [1]	100	1.2
2	IPCDN [2]	400	1
3	CMOS Oscillator circuit	415	1

Table 2. Comparison for power dissipation and transistor count

Sl.No	Methods	Power dissipation in μ W	No. of transistors
1	IPCDN [2]	6.4	18
2	CMOS Oscillator circuit	2.5	10

Table 3. Comparison of power consumption for inverter

Sl.No	Power consumed by inverter with CMOS Oscillator in μW	Power consumption in a normal Inverter in μW
1	73.51	200

Table 4. Comparison of power consumption in NAND gate

Sl.No	Power consumed by NAND gate with CMOS oscillator in fW	Power consumption in a normal NAND gate in fW
1	550	5000

Table 5. Comparison of power consumption in NOR gate.

Sl.No	Power consumed by NOR gate with CMOS oscillator in pW	Power consumption in a normal NOR gate in pW
1	3	1790

4. CONCLUSION

In this paper, the proposed circuit have successfully designed to generate a combined signal. Results of simulation show signals upto 5 GHz an be generated. Implemented circuit has been tested on combinational circuits like Inverter, NAND and NOR gate and it is found that these gates consume 10 times lesser power with the proposed circuit as compared to conventional NAND , NOR and NOT gates.

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