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Approximate arithmetic circuits

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ABSTRACT

Low power consumption is the necessity for the integrated circuit design in CMOS technology of nanometer scale. Recent research proves that to achieve low power dissipation, implementation of approximate designs is the best design when compared to accurate designs. In most of the multimedia applications, DSP blocks has been used as the core blocks. Most of the video and image processing algorithms implemented by these DSP blocks, where result will be in the form of image or video for human observing. As human sense of observation is less, the output of the DSP blocks allows being numerically approx- imate instead of being accurate. The concession on numerical exactness allows proposing approximate analysis. In this project approximate adders, approximate compressors and multipliers are proposed. Two approximate adders namely PA1 and PA2 are proposed which are of type TGA which provides better results like PA1 comprises of 14 transistors and 2 error distance, achieves reduction in delay by 64.9 % and reduction in power by 74.33% whereas the TGA1 had 16 transistors and more power dissipation.PA2 comprises of 20 transistors and 2 error distance. Similarly, PA2 achieves delay reduction by 51.43%, power gets reduced by 67.2%. PDP is reduced by 61.97 % whereas TGA2 had 22 transistors. Approximate 4-2 compressor was proposed in this project to reduce number of partial product stages. The compressor design in circuit level took 30 transistors with 4 errors out of 16 combinations whereas existing compressor design 1 took 38 and design 2 took 36 transistors. By using the proposed adder and compressors, approximate 4x4 multiplier is proposed. The proposed multiplier achieves delay 124.56 (ns) and power 29.332 (uW) which is reduced by 68.01 % in terms of delay and 95.97 % in terms of power when compared to accurate multiplier.

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1. INTRODUCTION

Digital Signal Processing (DSP) blocks are most commonly used in multimedia applications whose output is in the form of image for human recognition [1, 2]. The output image need not to be numerically accurate for human sense. This allows us to perform approximate computation to reduce power consumption over conventional designs. As Adders and multipliers are main components in an ALU, those arithmetic circuits will be responsible for overall performance of processor. So in order to achieve better performance and reduced power consumption design of approximate arithmetic circuits is needed. Various high-speed conventional adders such as carry look ahead adders (CLAs) and multipliers like Wallace tree multipliers,

Dadda and Vedic multipliers have been widely utilized. However, conventional arithmetic circuits that perform exact operations may lead to difficulties in performance improvement and requires more power consumption. Approximate arithmetic circuits that allows relaxation in accuracy and reduce the critical path delay of a circuit. Since most approximate designs have reduced complexity by simplifying logic in various abstraction levels like behavioral level, gate level and transistor level. This tends to have a reduced power consumption and area overhead. Thus, approximate designs are suitable approach to improve the area, power and speed of a processor.

This paper proposes two new transmission gate based adders (PA1 and PA2) in comparison with [3]. Transmission gate is the best alternate technology for pass transistor with high voltage swing. Also this paper proposes approximate 4-2 compressor with reduced no. of transistors in comparison with [4]. The proposed compressor is used in design of approximate multiplier design. Delay, area, Error Distance (ED),power and power-delay product were calculated and compared with accurate adders, compressors and multipliers. This paper is organized as follows. Section II describes brief literature survey. Section III proposes circuit level imple- mentation of PA1 and PA2, approximate 4-2 compressor and approximate multiplier designs. Section IV represents results and Discussions. Section V concludes the paper.

2. LITERATURE SURVEY

Few works that had been carried out on reducing logic com- plexity by approximating adder designs in transistor level. In [1, 2] bit by bit addition took place by modifying the mirror adder circuit. Five different approximation of mirror adder have been proposed with removal of certain transistors from conventional mirror adder, ensuring less errors in full adder circuit. Image and video compression algorithms are presented using proposed approximate circuit designs and output quality was measured. In [5] pass transistors are used in XOR/XNOR based approximate adders. New approximate adders (AXAs) were designed using multiplexer based XOR/XNOR gate in pass transistors topology. AXA1 has more static power dissipation with better performance in carry propagation delay. AXA2 has small dynamic power dissipation. AXA3 achieves reduction in energy consumption.However, these designs suf- fers from signal degradation. In [3] Transmission Gate based adders were proposed to overcome signal degradation. Two new TGA based approximate adders were designed. The adder consists of three modules in which first and second modules consists of XOR gate for producing sum and third module consists of multiplexer for producing carry. TGA 1 uses 16 transistors with 2 errors in carry and 2 errors in sum. Similarly TGA2 uses 22 transistors with same error count. Delay, power and power-delay product were calculated for proposed designs. Even though increase in transistor count, the TGA based adders achieves better voltage swing and has less delay and power consumption when compared to AXAs. Various error metrics like ED, MED and ER were calculated for the TGA based approximate adders. The design in [3] achieve better delay and power consumption when compared to other existing designs. In [6] low power area efficient 10-transistor one bit full adder cell (10TD) is designed and its performance is compared with Transmission Gate based full adder [3]. One bit 10TD cell achieved 30% more speed than TGA based adder. Similarly the 10TD cell achieves 50% more power savings than TGA. For 32 bit RCA using 10TD, speed is 44% more than 32 bit RCA using TGA. The proposed 32 bit RCA in [6] operates at frequency of 330 MHz and also uses less number of transistors when compared to TGA based FA cell. In [7] powerless XOR and groundless XNOR gates were proposed. Instead of providing VDD and VSS, the terminals are connected to inputs. Full adders design consists of three modules, in which module 1 and 2 can be XOR/XNOR gates and module 3 is multiplexer which provides carry output.Total 41 new 10 transistor full adder cells were proposed using novel XOR/XNOR gates. Among all adders in [7], 9B adder achieves consistently low power. Adders 9A and 13A achieve better critical path delay. The design in [7] achieves 10% less power and better delay compared to 10TD FA cell. [8] a novel 10 transistor full adder design has been proposed with high speed and with low power-delay product. This paper uses complementary and level restoring carry logic to avoid multiple threshold losses in carry chain by proper level restoring. The XNOR circuit used in this paper is realized by 2-1 multiplexer which can be used as level restorer logic. The output of level restorer is then connected to MUX 2 and MUX 3 to generate sum and carry. This logic achieves less threshold voltage loss compared to existing designs. The design in [8] uses lower power supply to minimize the power consumption. The goal of the proposed design is to achieve reduced complexity and to achieve faster cascade operation. In [9, 10] various terminologies were explained in detail which is used in approximate computations like overall error (OE), Mean Error Distance (MED), Accuracy (ACC) and Error Rate (ER) etc. In [9] the arithmetic addition is done by dividing input bits into two parts. Conventional part consists of MSBs and approximate part consists of LSBs. The design in [9] is especially used for multiple bit addition to ensure that the design has minimal errors and to retain better output quality. In 2x2 approximate multiplier was proposed and this design achieves average power savings when compared to accurate 2x2 multiplier. The approximate multiplier got

only one error out of seven possible inputs. The modified K-Map is presented with change in one output bit of an accurate 2x2 multiplier. From the approximate multiplier complexity of the design is reduced and also critical path is reduced when compared to accurate multiplier. In [11] discuss about novel multiplier design which involves multiplication of group of coefficients in DSP blocks. 4x4 modified array multiplier with reduced switching activity is proposed. The proposed multiplier in uses new adder blocks by adding multiplexers to the existing blocks. The design achieves 50% less power con- sumption when compared to conventional multiplier. In [12] 4x4 conventional array and vedic multipliers were proposed and performs spice simulations. Simulation results shows that vedic multiplier achieves 29% reduction in power when compared to array multiplier. Hardware complexity of array multiplier is more when compared to vedic multiplier. In [4] two novel approximate 4-2 compressors were implemented. The accurate 4-2 compressor requires 52 transistors which is implemented in [13] and existing approximate compressors requires 38 and 36 for compressor 1 and compressor 2 respec- tively. The proposed compressors in [4] were implemented in circuit level using transmission gate based technology in hspice tool. The approximate compressors uses very less number of transistors, achieves less critical path delay and also power consumption is very less when compared to exact 4-2 compressors. The compressors were used as main block in implementing approximate dadda multiplier. Two dadda multiplier designs were implemented in [4]. In one of the multiplier design compressor 1 is used in LSBs and in other design compressor 2 is used in LSBs. Normalized Error Distance (NED) is calculated for the dadda multipliers and compared with other multipliers. The application of these multipliers in image processing is presented by multiplying two images.

In [14] error tolerant multiplier was proposed, in this method input bits are divided into multiplier and non-multiplier parts, the multiplier part consists of MSBs and the non-multiplier part consists of LSBs. The size of the error tolerant multiplier is 12 bits. Accuracy, area and power of conventional 12 bit multiplier and 12 bit error tolerant multiplier were compared and tabulated. Various new terminologies like Minimum Ac- ceptable Accuracy (MAA) and Acceptance Probability (AP) were used in [14]. For MSBs normal multiplication method is applied, whereas for LSBs a new method is applied in which no partial products were generated and carry propagation path is removed. From simulation results the 12 bit error tolerant multiplier drastically reduces power from 52% to 94% depending on input transitions and also reduces the area overhead. In [13] designed low power 4-2 and 5-2 compressors. The accurate 4-2 compressor and accurate 5-2 compressors both can operate at low supply voltage of 0.6v. The 4-2 compressors consist of three XOR-XNOR blocks, two MUX blocks and one XOR block. The transistor count of 4-2 compressor is 52. Similarly the 5-2 compressors consist of five XOR-XNOR blocks, three MUX blocks and one XOR block. The compressors were implemented in transmission gate based technology and compared with the existing compressors which were implemented in CMOS style, simulation results shows that the compressors 4-2 and 5-2 in [13] achieves low power dissipation and less hardware complexity. In [15, 16] analysis and design of three new approximate 4-2 compressors were proposed by changing logic in accurate compressor for use of those compressors in multiplier. The design had reduction in power dissipation and transistor count compared to exact design. The compressor achieves better accuracy when com- pared to accurate compressor. An 8 bit approximate dadda multiplier is implemented in [15] in which both approximation and truncation methods were used for reducing the partial product stages. The multiplier design in such a way that 4 bits in LSB is truncated and the next four bits uses approximate compressors. For the MSBs accurate compressors were used. Hence in total the approximate multiplier uses 9 accurate, 8 approximate compressors, 3 full adders and 2 half adders. The use of approximate and truncation compressors reduces power dissipation and area overhead when compared to accurate multiplier.

3. PROPOSED METHOD

This section deals with working of PA1, PA2, proposed approximate 4-2 compressor and proposed 4*4 approximate multiplier.

3.1. Proposed adder design 1 (PA1)

As transmission gate passes strong 0 and strong 1 it is used as alternate style to pass transistor. PA1 consists of TGA based multiplexer for designing of XOR/XNOR modules and also consists of inverters. In [5] the Sum and Carry expressions of TGA1 is given as

$$sum = (X \circledS Y)c_{in} + X\bar{Y} \quad (1)$$

$$carry = Y \quad (2)$$

In PA1 the sum and carry expression is modified as

$$sum = (X \textcircled{S} Y)C_{in} \quad (3)$$
$$carry = X \quad (4)$$

In sum expression the second term $(X\bar{Y})$ is removed and carry expression is connected to input X for PA1. The total number of transistors used are 14 were 2 transistors less when compared to existing TGA1 in [5]. The error table of PA1 is shown in Table 1.

Table 1. Error table of PA1

X	Y	c_{in}	sum	carry	Error Distance (ED)
0	0	0	0	0	0
0	0	1	1	0	0
0	1	0	0	0	1
0	1	1	0	0	1
1	0	0	0	1	1
1	0	1	0	1	0
1	1	0	0	1	1
1	1	1	1	1	0

From Table 1 we can observe that the PA1 have 2 errors in sum and 2 errors in carry. we observe that when inputs X and Y are 1 the carry will get error output, when X and Y are 1 and 0 respectively the sum will get error. When both X and Y are 0 the sum and carry both gets error output. The circuit level implementation of PA1 is shown in Figure 1.

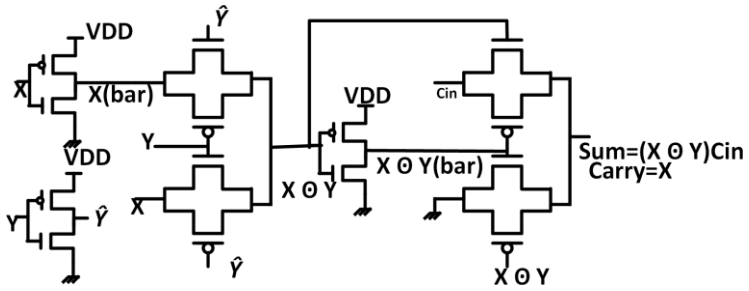

Figure 1. Schematic of PA1

3.2. Proposed adder design 2 (PA2)

In [5] the sum and carry expressions of TGA2 is given as

$$sum = (X \textcircled{S} Y)C_{in} \quad (5)$$
$$carry = X + Y \quad (6)$$

The PA2 requires 20 transistors which is less than that of TGA2 in [3]. The sum and carry expressions of PA2 is given by

$$sum = \overline{carry} \quad (7)$$
$$carry = XY + (X + Y)C_{in} \quad (8)$$

The carry expression of PA2 is same as exact full adder carry expression. Hence there are zero errors in carry. The sum is obtained by inverting carry. The error table of PA2 is shown below. From Table 2 when X and Y are 0s then we will get error at sum. When X and Y are 1 and 0 respectively then sum output has error. Carry output has zero errors. The circuit level implementation of PA2 is shown in Figure 2. It contains transmission gate-based multiplexer for implemen- tation of carry and one inverter for implementation of sum output.

Table 2. Error table of PA2

X	Y	C_{in}	sum	carry	Error Distance (ED)
0	0	0	**1**	0	1
0	0	1	1	0	0
0	1	0	1	0	0
0	1	1	0	1	0
1	0	0	1	0	0
1	0	1	**0**	1	1
1	1	0	0	1	0
1	1	1	0	1	0
0	0	0	**1**	0	1

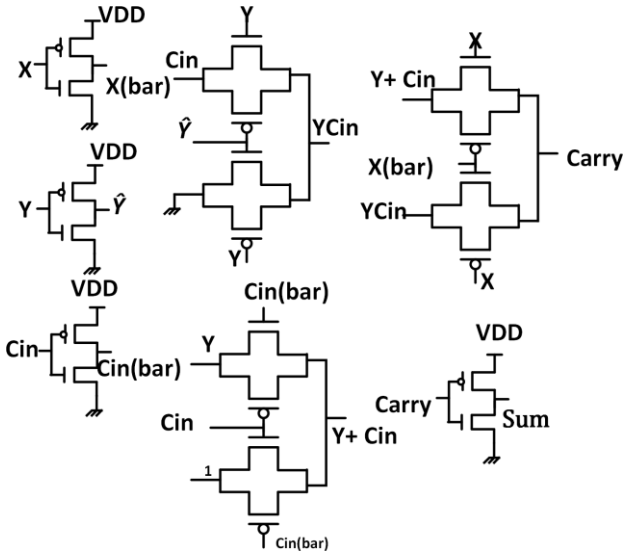

Figure 2. Schematic of PA2

3.3. Proposed approximate 4-2 compressor

In [13] exact 4-2 and 5-2 compressors were implemented. The exact 4-2 compressor have five inputs and three outputs. The four inputs X1, X2, X3, X4 and output sum have same weight. The output carry size is one bit more. The 4-2 compressor receives an input Cin from the last cell which is of one bit size lower, and produces an output Cout to the later stage compressor cell which is of size higher. The different forms of 4-2 compressor follows the fundamental equation given by:

$$X_1 + X_2 + X_3 + X_4 + C_{in} = sum + 2(carry + c_{out}) \quad (9)$$

The conventional 4-2 compressor composed of two serially connected full adders. It mainly composed of six modules. Two modules are 2-1 mux, one module is XOR and three modules are XOR-XNOR. The circuit level implementation of 2-1 mux comprises of 8 transistors, for XOR-XNOR circuit 10 transistors and for XOR circuit 6 transistors. So totally 52 transistors for implementing exact 4-2 compressor in transmission gate based technology. The sum, carry and cout expressions of exact 4-2 compressor is given by:

$$sum = X_1 \oplus X_2 \oplus X_3 \oplus X_4 \quad (10)$$

$$c_{out} = (X_1 \oplus X_2)X_3 + (X_1 \circledS X_2)X_1 \quad (11)$$

$$carry = (X_1 \oplus X_2 \oplus X_3 \oplus X_4)C_{in} + \overline{(X_1 \oplus X_2 \oplus X_3 \oplus X_4)}X_4 \quad (12)$$

In order to reduce the no. of transistors and to reduce the power consumption the approximation of compressors were implemented in [4, 15] with relaxation in accuracy. Two approximate 4-2 compressors were designed in [4] by reducing the transistors to 38 and 36 respectively. The design 1 has 12 errors out of

35 combinations has error. The design 2 has 4 errors out of 16 combinations. But there was drastic reduce in power consumption. The presence of errors in approximate designs will not affect the image clarity and also for human perception there is no need of exactness of image. In this paper new approximate 4-2 compressor is implemented. The proposed circuit level compressor took only 30 transistors which is very much less when compared to existing with same number of errors. The expression of sum and carry for existing design 1 in [4] were given by:

$$sum = \overline{C_{in}}(\overline{(X_1 \oplus X_2)} + \overline{(X_3 \oplus X_4)}) \quad (13)$$

$$c_{out} = \overline{\overline{X_1X_2} + \overline{X_3X_4}} \quad (14)$$

$$carry = C_{in} \quad (15)$$

For design 2 compressor the sum and carry expressions in [14] were given by:

$$sum = \overline{(X_1 \oplus X_2)} + \overline{(X_3 \oplus X_4} \quad (16)$$

$$carry = \overline{\overline{X_1X_2} + \overline{X_3X_4}} \quad (17)$$

In proposed approximate 4-2 compressor the sum expres- sion and carry expression is modified in such a way that num- ber of transistors is reduced to 30. sum and carry Expressions for proposed 4-2 compressor is given by:

$$sum = (X_1 \oplus X_2) \oplus (X_3 \oplus X_4) \quad (18)$$

$$carry = (X_1 + X_2)(X_3 + X_4) \quad (19)$$

The proposed compressor does not have Cin and Cout, which were present in existing compressors [4, 13 15]. The circuit level implementation of proposed design in shown in Figure 3. In above diagram two blocks comprises of XOR circuit which took 10 transistors for implementing each block. The next two blocks is OR function which took 8 transistors and it is implemented by MUX based transmission gate technology. The last block will perform AND function. Hence the above proposed design is implemented with 30 transistors less than that of [4, 13 15]. The error table for proposed approximate 4-2 is shown Table 3.

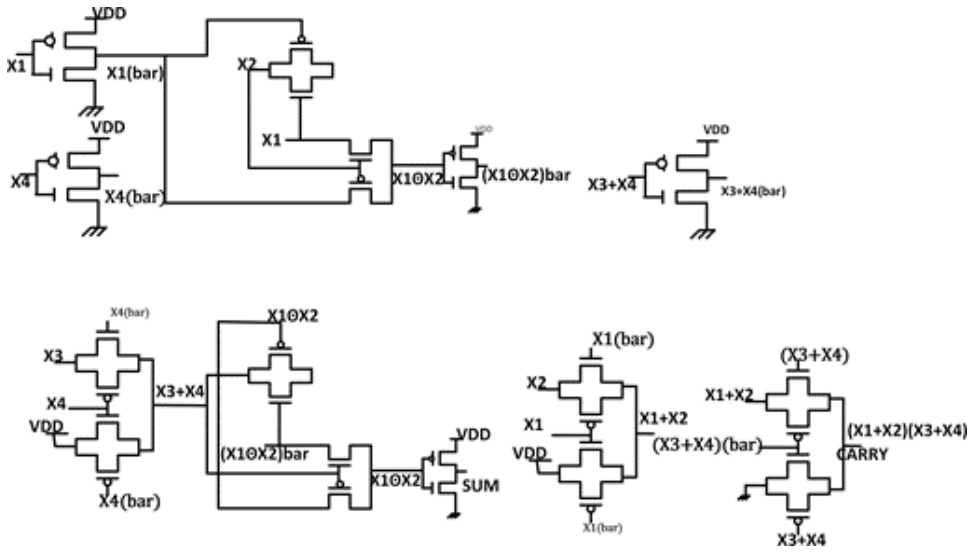

Figure 3. Schematic of 4-2 approximate compressor

Table 3. Error table of approximate 4-2 compressor

X_1	X_2	X_3	X_4	sum	carry	difference
0	0	0	0	0	0	0
0	0	0	1	1	0	0
0	0	1	0	1	0	0
0	0	1	1	0	0	0
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	1	0	1	1
1	0	0	0	1	0	0
1	0	0	1	0	1	0
1	0	1	0	0	1	0
1	0	1	1	0	1	1
1	1	0	0	0	0	1
1	1	0	1	1	1	0
1	1	1	0	1	1	0
1	1	1	1	1	1	1

From Table 4 we can observe that there are 4 errors out of 16 combinations which is same as we observed in existing approximate 4-2 compressor but the main advantage in the proposed method is the reduction of transistors is achieved. If the inputs are 0111 then its output will be equal to 11 but the output we get is 10, so difference is 1. Similarly for remaining three cases the actual output is not equal to the output obtained from the proposed design. The error table for proposed approximate multiplier is shown below in Table 4.

Table 4. Error table of approximate multiplier

A[3 : 0]	B[3 : 0]	Accurate product	Approx. product	ED
0000	0000	00000000	0000**111**0	3
0101	0111	00100011	0010**111****0**	3
1111	1111	11100001	11100**11**1	2
1111	1011	10111101	1011**001**1	3
1011	1001	01100011	0110**110**1	3
1010	1101	10000010	1000**111****1**	3
1110	1101	10100100	10100**01**0	2
0110	1000	01110010	0111**11**10	2
0100	1000	01000000	0100**111**0	3
0001	0100	00000010	00000**1**10	1

3.4. Proposed approximate 4x4 multiplier design

In literature various multiplier designs in circuit level is implemented namely array multiplier, vedic multiplier and dadda multiplier. All the exact multiplier design process too place in three stages:

- An CMOS logic style based AND gate is used for generating the partial products is the first stage.
- Use of exact/approximate 4-2/5-2 compressors to deduce number of partial product stages in multiplier design.
- Using accurate half adder, accurate full adder or any other approximate adder designs like PA1/PA2 to add the partial products and to generate the final output.

In [17] 2x2 multiplier were implemented and error were intro- duced in the design by manipulating its logic function. The K-Map is modified in such a way that when all inputs were 1 the output product usually it will be equal to 1001 (9), but modified this result to 111(7), it results in reduction of critical path by two gates compared to accurate 2x2 multiplier. With [17] as reference in this paper approximate 4*4 multiplier has been proposed. In this design the proposed approximate adder and approximate compressor are used as basic blocks. The multiplier shown in 4 is of size 4 bits. There are 2 inputs A, B each of size 4 bits and output product out of size 8 bits. The circuit level of proposed 4*4 array multiplier is implemented with accurate 1 bit transmission gate based half adder, PA1,PA2 and approximate 4-2 compressor. The total possible input combinations were tabulated in error table. The most of the errors were found in LSBs. Out of 256 combinations 32 combinations were found error according to error table. The circuit level implementation of proposed multiplier design is shown in Figure 4.

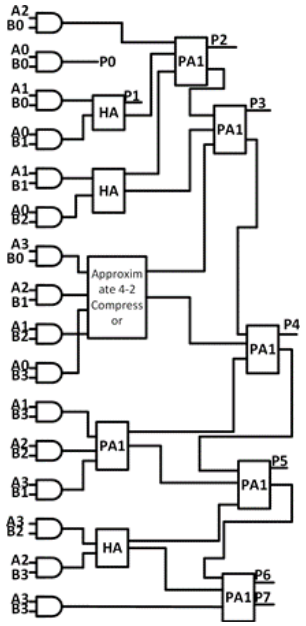

Figure 4. Schematic of 4x4 approximate multiplier

Some metrics which are commonly used in this paper:

Error Distance : Error Distance is denoted by (ED). It is defined as difference between result obtained by approximate adder and result obtained by accurate adder.

$$ED = |E_C - E_R| \tag{20}$$

were E_C is the result obtained by approximate adder and E_R is the result obtained by accurate adder.

Error Rate : Error Rate is defined as ratio of incorrect output values to all possible outputs.

$$ER = \frac{\#of\ incorrect\ outputs}{total\ possible\ outputs} \tag{21}$$

Pass Rate: Pass Rate is defined as ratio of number of correct outputs to all possible output values.

$$PR = \frac{\#of\ incorrect\ outputs}{total\ possible\ outputs} \tag{22}$$

Accuracy: Accuracy of an adder defines how much percent- age is the output of an approximate adder for an particular input. The value ranges from 0% to 100%.

$$ACC = \left(1 - \frac{ED}{E_R}\right)^{\Sigma} x100\% \tag{23}$$

4. RESULTS AND DISCUSSION

The proposed approximate adders (PA1, PA2), approximate 4-2 compressor and proposed approximate multiplier were implemented in circuit level in Cadence Virtuoso tool in gpdk 90nm technology. The results obtained is compared with existing adders, comparators and multipliers and observed that the proposed PA1 and PA2 requires less transistors with minimal errors in sum and carry expressions. As transistor number reduces the power of PA1 and PA2 also reduces when compared to existing adders. In proposed approximate 4-2 compressor the no. of transistors requires is reduced by modifying the sum and carry expression logic in circuit level. Th no. of transistors required is reduced to 30 as compared to existing compressors in [4] which requires 38 for existing compressor 1 and 36 for existing compressor 2. As transistor count is reduced to 30, power consumption also reduces drastically. As the proposed approximate multiplier uses PA1, PA2 and approximate 4-2 compressor, the transistor count of proposed multiplier also reduces by large number when compared to accurate multilplier.

4.1. Proposed adder design (PA1)

The schematic of PA1 consists of 14 transistors. The circuit level of PA1 is implemented in cadence virtuoso tool in gpdk 90nm technology.

From Figure 5 we can observe that transmission gate based xnor circuit and AND gate were implemented to get sum output. The carry output is obtained by directly connecting to input X.

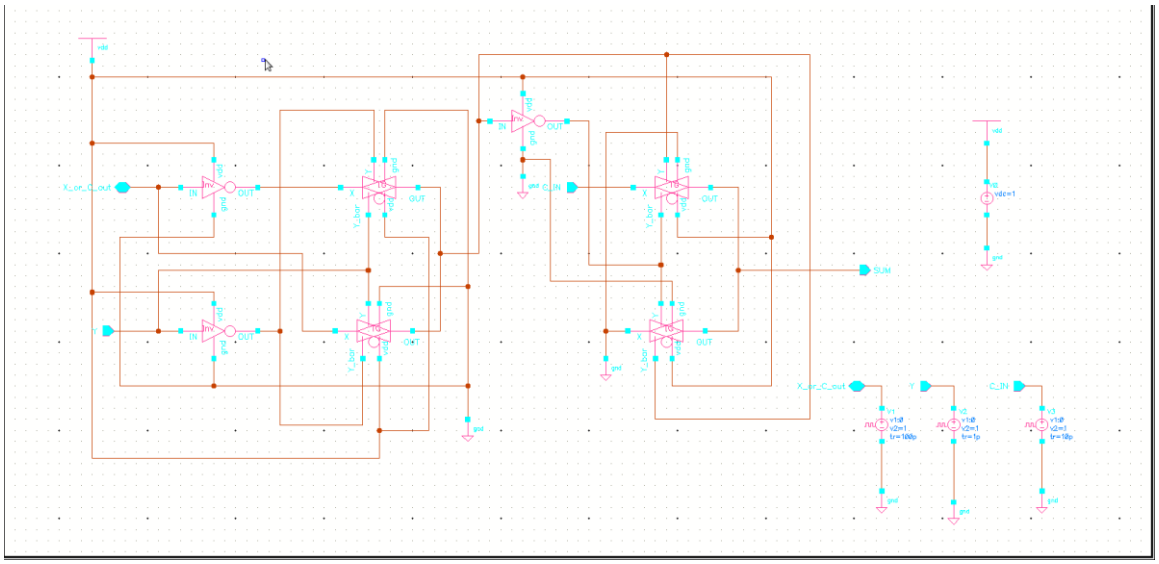

Figure 5. Schematic of PA1

From Figure 6 we can observe that inputs of PA1 are X, Y and C_{in}. The outputs were Sum and Carry. The waveform of PA1 varies according to inputs with the help of Sum and Carry expressions. From 6 the proposed design got two errors in carry and two errors in sum at X=0, Y=0, C_{in} =1, X=1, Y=0, C_{in} =0 and X=1, Y=1, C_{in} =0. The ED is shown in Table 1.

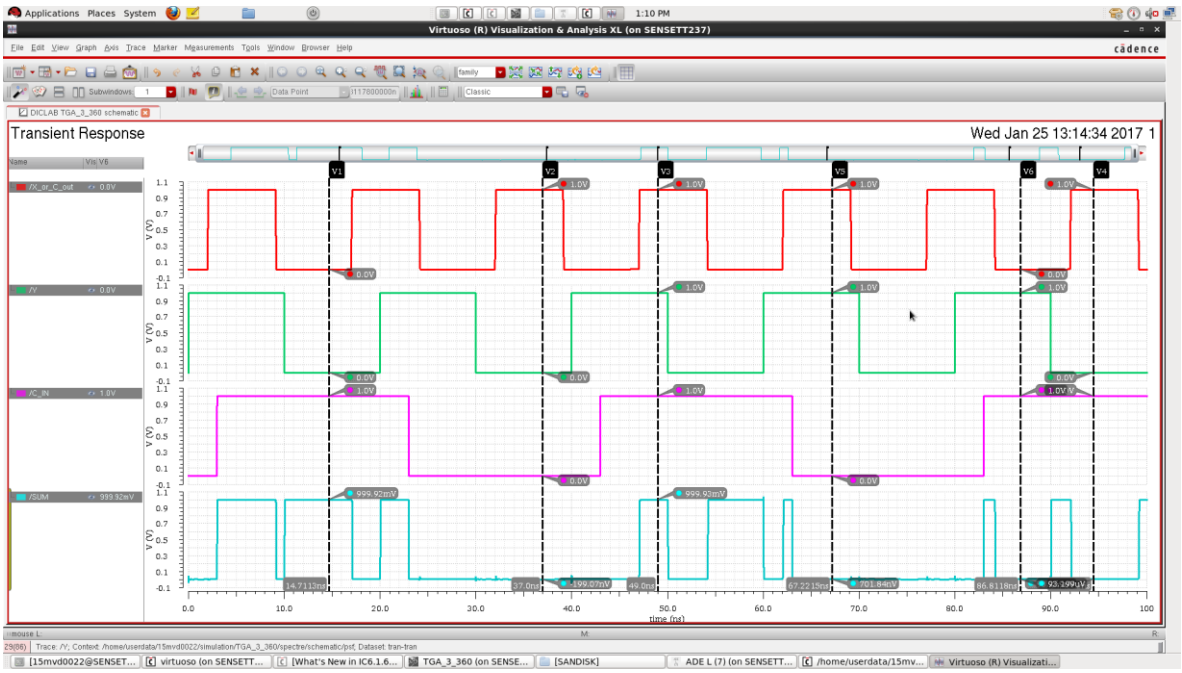

Figure 6. Waveform of PA1

4.2. Proposed adder design (PA2)

The PA2 comprises of 20 transistors which is less than existing design 2 adder in [3] which requires 22 transistors. The circuit level of PA2 is implemented in cadence virtuoso tool in gpdk 90nm technology. The schematic on Figure 7 consists of MUX based OR and AND function for implementing carry expression and sum is inverted output of carry. PA2 also implemented in transmission gate based technology.

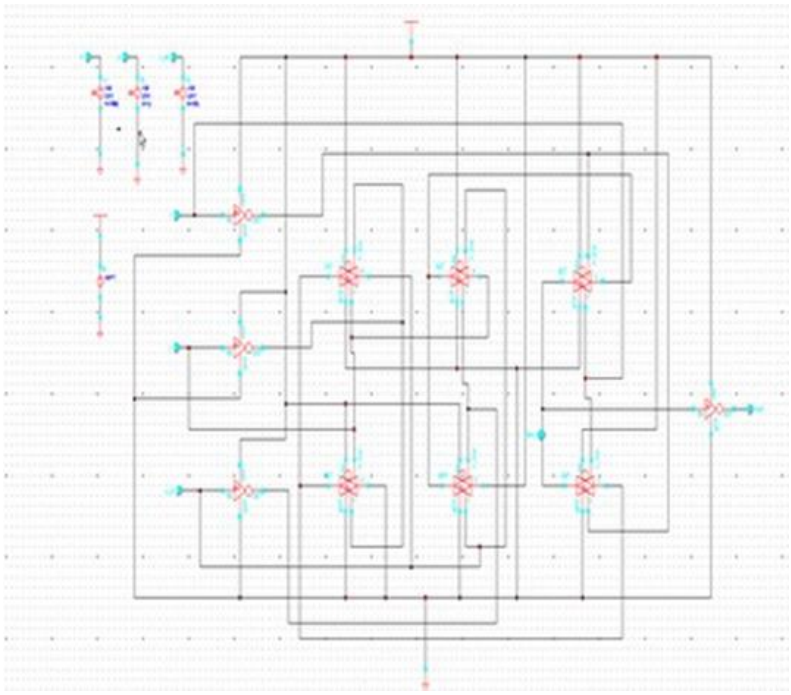

Figure 7. Schematic of PA2

From Figure 8 we can observe that inputs of PA2 are X, Y and C_{in}. The outputs were Sum and Carry. The waveform of PA2 varies according to inputs with the help of Sum and Carry expressions. From Figure 8 the proposed design got zero errors in carry and two errors in sum at X=0, Y=0, C_{in} =0 and X=1, Y=0,C_{in} =1. The ED is shown in Table 2.

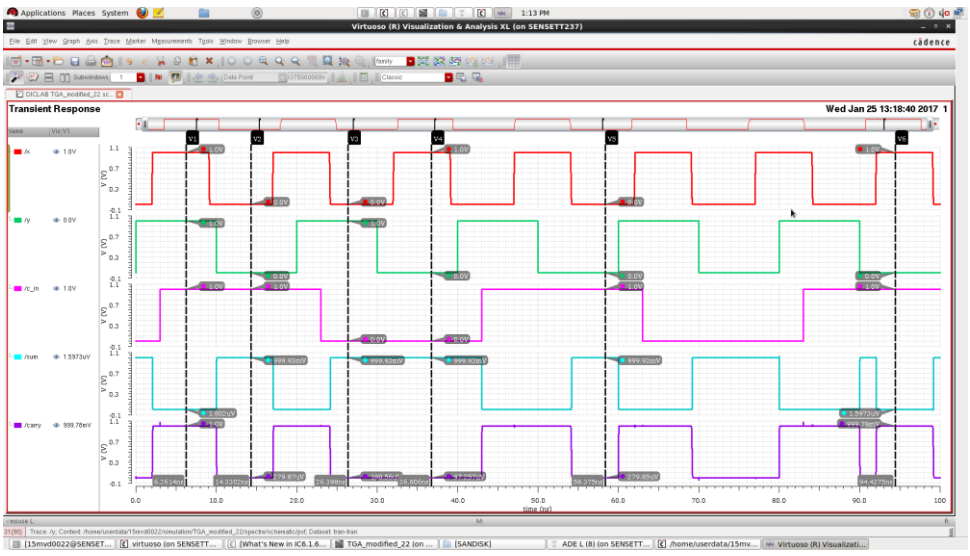

Figure 8. Waveform of PA2

4.3. Proposed approximate 4-2 compressor

The proposed compressor comprises of 30 transistors im- plemented in transmission gate based technology. The circuit level implementation of approximate compressor is shown in Figure 9. It consists of four inputs and two outputs. The compressor consists of XOR, OR and AND logic functions which were implemented with MUX based transmission gate technology. The circuit level is implemented in cadence virtuoso tool in gpdk 90nm technology.

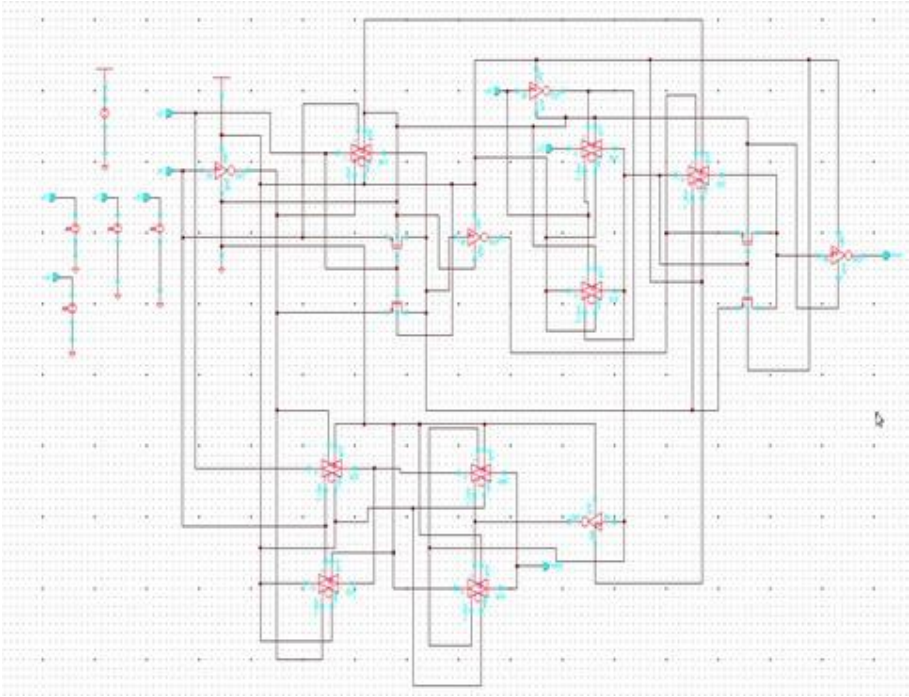

Figure 9. Schematic of approximate 4-2 compressor

The inputs of the proposed compressor are X_1, X_2, X_3 and X_4. The outputs were sum and carry. The waveform of proposed compressor varies according to inputs with the help of Sum and Carry expressions. From Figure 10 the proposed design got 4 errors out of 16 combinations with 30 transistor count. Whereas in [4] the compressor design 2 has same 4 errors but with transistor count of 36.

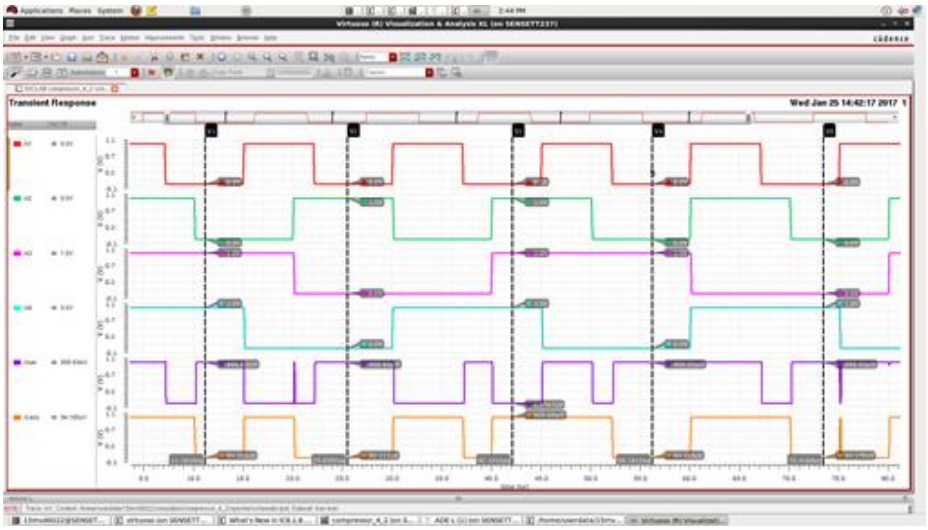

Figure 10. Waveform of approximate 4-2 compressor

4.4. Proposed approximate 4 bit ripple carry adder using PA1

By using proposed adder design (PA1), 4 bit ripple carry adder is proposed. The proposed 4 bit adder is compared with accurate ripple carry adder. From Figure 12 we observed that more number of errors were present at LSBs than im MSBs. The circuit level of 4 bit RCA using PA1 is implemented in cadence virtuoso tool in gpdk 90nm technology. The transistor count of proposed 4 bit RCA is 56. Power consumption of proposed design is reduced when compared to accurate ripple carry adder. The schematic of proposed RCA is shown in Figure 11.

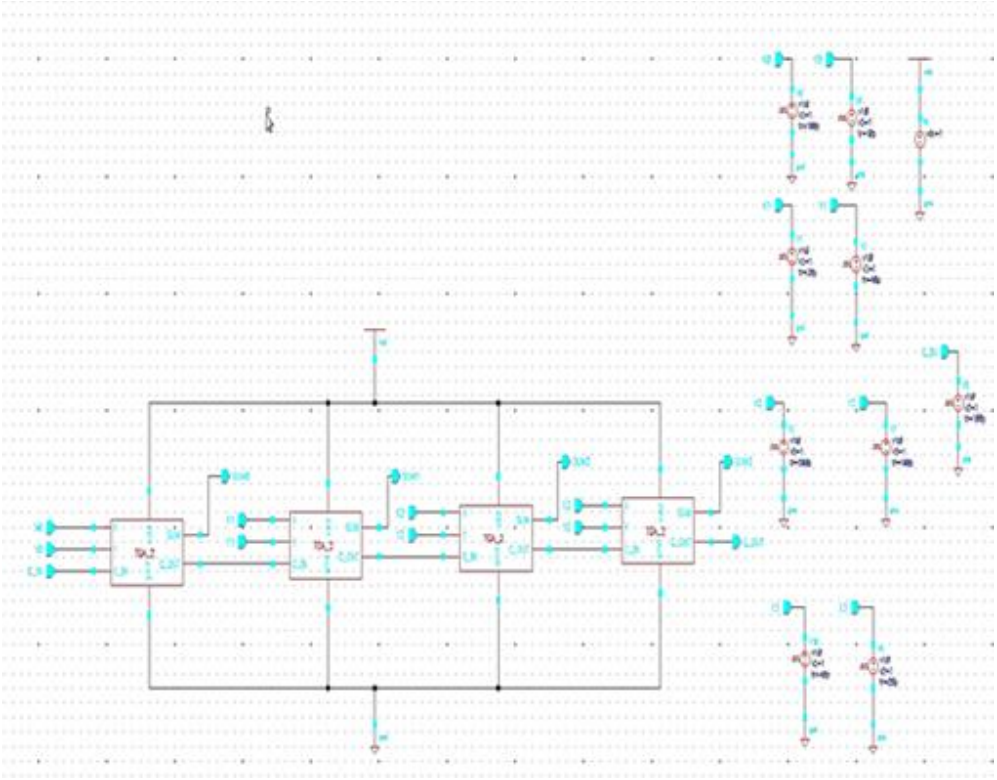

Figure 11. Schematic of approximate 4 bit RCA using PA1

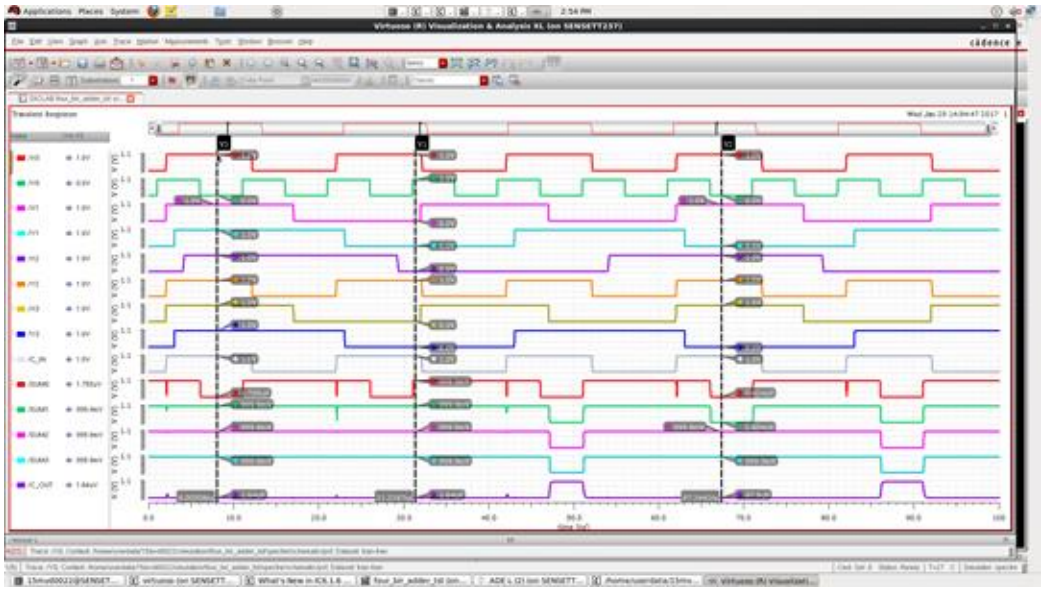

Figure 12. Waveform of approximate 4 bit RCA using PA1

4.5. Proposed approximate 4 bit ripple carry adder using PA2

By using proposed adder design (PA2), 4 bit ripple carry adder is proposed. The proposed 4 bit adder is compared with accurate ripple carry adder. From Figure 14 we observed that more number of errors were present at LSBs than in MSBs. The circuit level of 4 bit RCA using PA2 is implemented in cadence virtuoso tool in gpdk 90nm technology. The transistor count of proposed 4 bit RCA is 80. Power consumption of proposed design is reduced when compared to accurate ripple carry adder. The schematic of proposed RCA is shown in Figure 13.

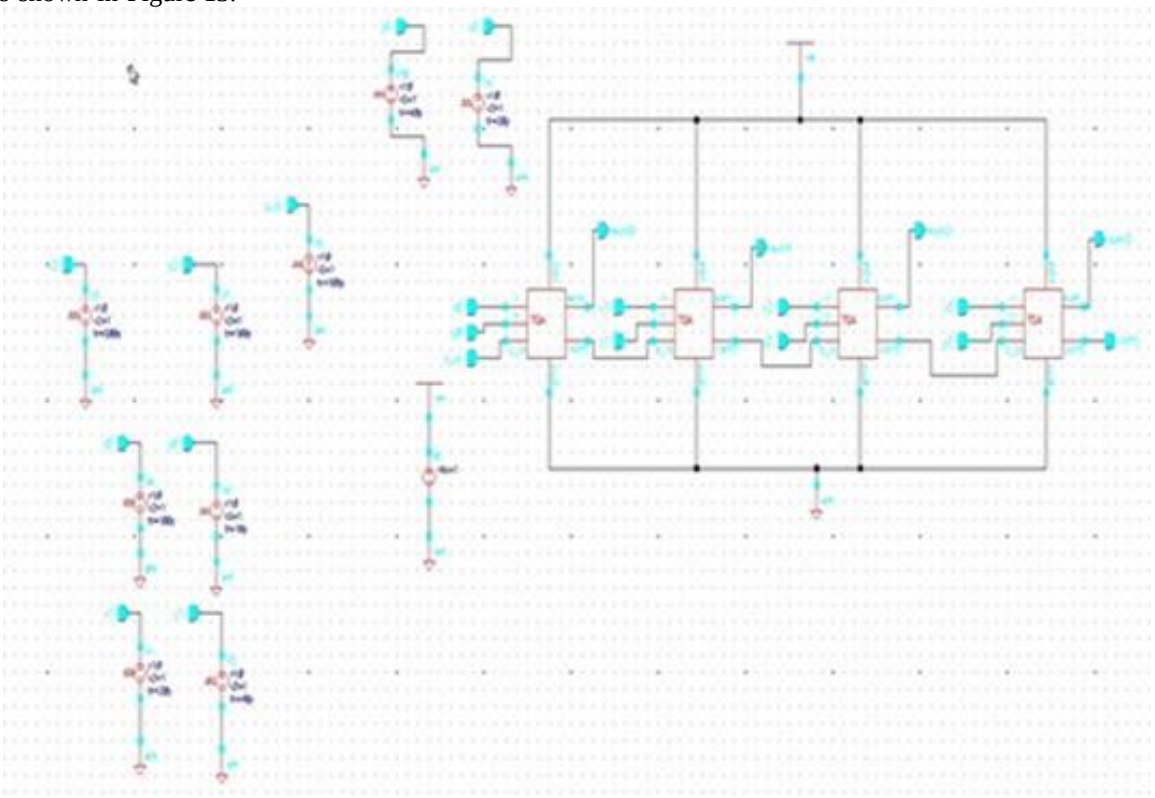

Figure 13. Schematic of approximate 4 bit RCA using PA2

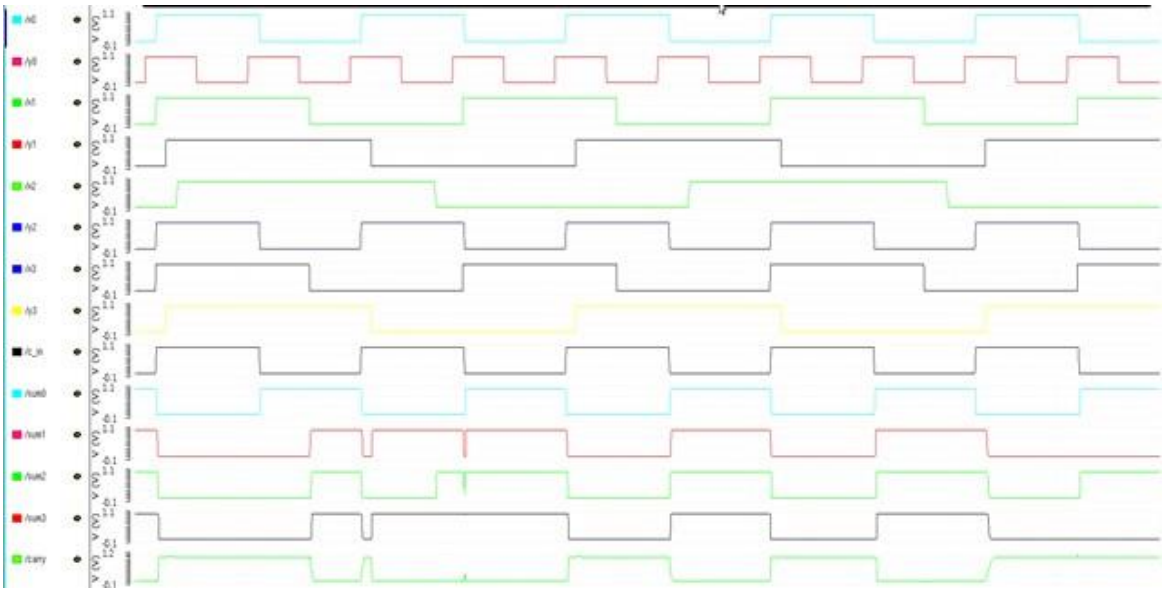

Figure 14. Waveform of approximate 4 bit RCA using PA2

4.6. Proposed approximate multiplier using PA1 and compressor

The proposed approximate multiplier is of size 4*4. The proposed multiplier consists of accurate half adder, proposed transmission gate based approximate adder design (PA1) and proposed approximate 4-2 compressor as the main blocks. The circuit level implementation of the proposed multiplier is shown in Figure 15. The design is implemented in cadence virtuoso tool in 90nm technology. The design consists of two inputs A and B with size of 4 bits and product of size 8 bits. From error table we observed that from total 256 combinations, errors were found in 32 combinations. Most of the errors were found in LSBs.

The waveform of approximate multiplier using PA1 is shown in Figure 16. The inputs of the design are A and B each of size 4 bits. The output is product with size 8 bits. From Figure 16 observed that most of the errors were present in LSBs so that the proposed design does not affect the image quality and also accuracy does not get affected. The transistor count of proposed design is 246 which is huge less than that of accurate multiplier, and also power reduces significantly in approximate multiplier.

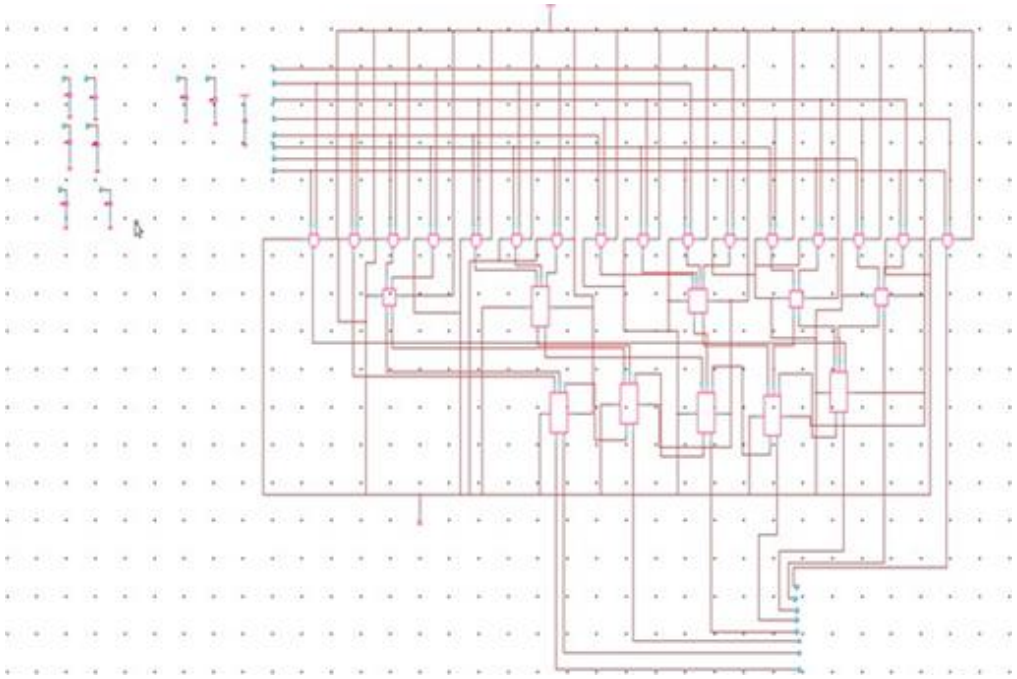

Figure 15. Schematic of approximate multiplier using PA1

Figure 16. Waveform of approximate multiplier using PA1

4.7. Proposed approximate multiplier using PA2 and compressor

The proposed approximate multiplier is of size 4*4. The proposed multiplier consists of accurate half adder, proposed transmission gate based approximate adder design (PA2) and proposed approximate 4-2 compressor as the main blocks. The circuit level implementation of the proposed multiplier is shown in Figure 17. The design is implemented in cadence virtuoso tool in 90nm technology. The design consists of two inputs A and B with size of 4 bits and product of size 8 bits. From error table we observed that from total 256 combinations, errors were found in 32 combinations. Most of the errors were found in LSBs.

The waveform of approximate multiplier using PA2 is shown in Figure 18. The inputs of the design are A and B each of size 4 bits. The output is product with size 8 bits. From Figure 18 observed that most of the errors were present in LSBs so that the proposed design does not affect the image quality and also accuracy does not get affected. The transistor count of proposed design is 282 which is huge less than that of accurate multiplier, and also power reduces significantly in approximate multiplier.

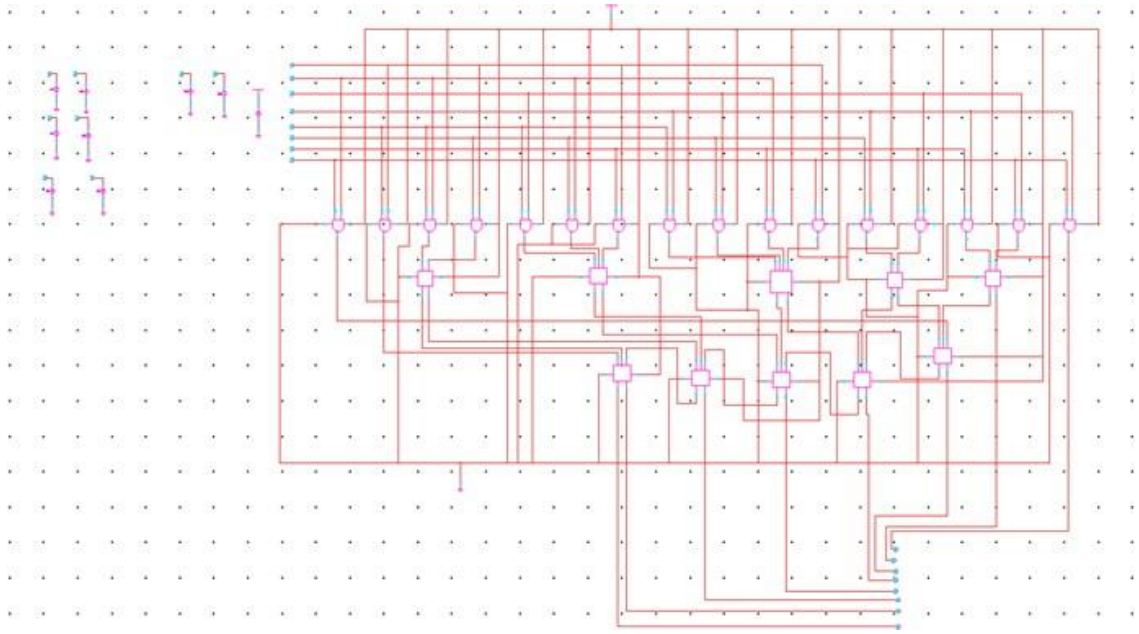

Figure 17. Schematic of approximate multiplier using PA2

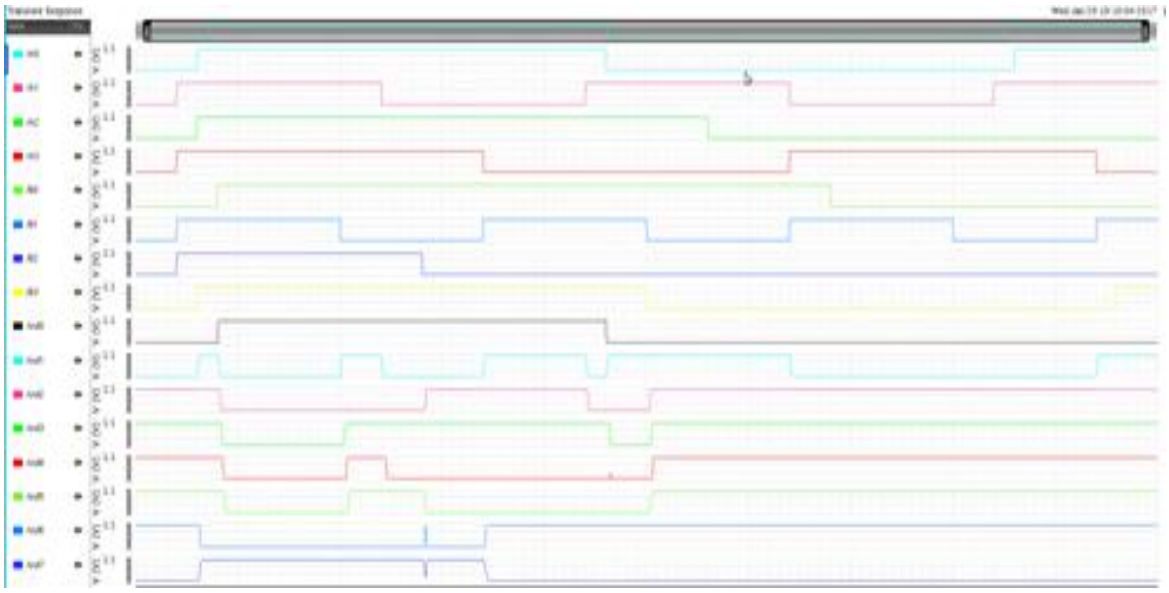

Figure 18. Waveform of approximate multiplier using PA2

4.8. Comparison with existing designs

The proposed adders, compressors and multipliers were compared in terms of number of transistors, power, delay and Power Delay Product (PDP).

4.8.1. Comparison of Number of Transistors for proposed designs

From Table 5 we can observe that [3] proposes adder based on transmission gate based technology, were TGA [1] uses 16 and TGA [2] uses 22 transistors with 2 error distance. Similarly in this paper also uses transmission gate based technology but with reduced number of transistors when compared to [3] or adders in which there is more voltage drop for cascading stages.

Table 5. Comparison table of no. of transistors for adders

Design	No. of transistors	Error Distance
TGA1 [4]	16	2
TGA2 [4]	22	2
AMA1 [1]	16	2
AMA2 [1]	14	2
AMA3 [2]	11	3
AMA4 [2]	11	3
AXA1 [3]	8	4
AXA2 [3]	6	4
AXA3 [3]	8	2
PA1	14	2
PA2	20	2

From Table 6 we can observe that [13] implemented circuit level exact compressor design which consists of XOR-XNOR module, MUX and XOR blocks. In total exact 4-2 compressor requires 52 transistors. In [4] two approximate designs were implemented in which design 1 requires 38 transistors with C_{in} and C_{out} and design 2 requires 36 transistors without C_{in} and C_{out}. The proposed design modifies the sum and carry expression in transistor level and reduces the transistor count to 30.

Table 6. Comparison table of no. of transistors for compressors

Design	No. of transistors	Error Distance
Exact compressor [16]	52	0
Design 1 [14]	38	12
Design 2 [14]	36	4
Proposed Design	30	4

4.8.2. Comparison of delay, power and PDP

The proposed approximate adders (PA1, PA2), approximate 4-2 compressor and proposed approximate multiplier were implemented in circuit level in Cadence Virtuoso tool in gpdk 90nm technology. The results obtained is compared with existing adders, comparators and multipliers in terms of power, delay and PDP as shown in Table 7, Table 8 and Table 9.

Table 7. Comparison table of approximate adders

Design	Delay (ns)	Power (uW)	PDP (10^{-15}J)
TGA1 [4]	1.245	1.97	2.45
TGA2 [4]	1.247	2.28	2.84
AMA1 [1]	1.378	2.79	3.84
AMA2 [1]	1.409	2.74	3.86
AMA3 [2]	1.468	2.55	3.74
AMA4 [2]	1471	2.53	3.72
PA1	0.755	1.13	0.85
PA2	0.824	1.32	1.08

Table 8. Comparison table of accurate and approximate compressors

Design	Delay (ns)	Power (uW)	PDP (10^{-15}J)
Exact compressor [16]	160.36	2.98	0.477
Design 1 [14]	158.32	2.27	0.359
Design 2 [14]	144.35	2.14	0.308
Proposed Design	87.36	1.06	0.092

Table 9. Comparison table of accurate and approximate multipliers

Design	Delay (ns)	Power (uW)	PDP (10^{-12}J)
Accurate Multiplier	389.45	729.47	284.09
Approximate Multiplier	124.56	29.332	3.653

5. CONCLUSION

From literature we conclude that mirror adders and pass transistors have signal degradation problem. To achieve high voltage swing with reduced number of errors we proposed approximate adders based on TGA. Also in this paper approx- imate multipliers were proposed. In order to reduce partial product stages in approximate multiplier, approximate 4-2 compressors were implemented. The proposed designs were simulated in cadence virtuoso tool in 90nm technology. The simulation results shows that the PA1 and PA2 uses less no. of transistors i.e. PA1 with 14 and PA2 with 22 transistors which is less when compared to existing adders like TGA1 and TGA2 in [14] with same error rate and achieves reduced delay and power consumption. The PA1 achieves delay of 0.755 (ns), power consumption is 1.13 (uW). The PA2 achieves delay of 0.824 (ns) and power gets reduced to 1.32 (uW). The proposed compressor uses 30 transistors and achieves delay of 87.36 ps and power consumption is 1.06 uW. The proposed approximate multiplier achieves less area with 282 transistors, delay of 124.56 ns and power consumption is 29.332 uW. Area, delay and power of proposed multiplier is very less when compared to accurate array multiplier. The proposed adders and multipliers are widely used in multimedia applications whose output image does not need to be numerically exact. The power reduction will be achieved by using approximate designs.

REFERENCES

[1] Vaibhav.Gupta, Debabrata Mohapatra, Anand Raghunathan, and Kaushik Roy, "Low-power digital signal processing using approximate adders," *IEEE Transactions on Computer- Aided Design of Integrated Circuits and Systems*, vol. 32, no. 1 pp. 124-137, 2013.

[2] Vaibhav.Gupta, Debabrata Mohapatra, Sang Phill Park, Anand Raghunathan, and Kaushik Roy, "impact: im- precise adders for low-power approximate computing," *IEEE Trans- Actions on Computer-Aided Design of Integrated Cir- Cuits And Systems*, vol. 30, no. 7, pp. 409-414, 2011.

[3] Zhixi Yang, Jie Han, and Fabrizio Lombardi, "Transmission-Gate based Ap- proximate Adders for inexact computing," *IEEE International Symposium on Nanoscale Architectures (NANOARCH)*, pp.145-150, 2015.

[4] Amir Momeni, Jie Han, Paolo Montuschi, and Fabrizio Lombardi, "Design and Analysis of Approximate Compressors for Multiplication," *IEEE Transactions on Computers*, vol. 64, no. 4, pp. 984- 994, 2015.

[5] Zhixi Yang, Ajaypat Jain, Jinghang Liang, Jie Han and Fabrizio Lombardi, "Approximate XOR/XNOR-based adders for inexact computing," *Proceedings of the 13th IEEE International Conference on Nanotechnology*, pp.690-693, 2013.

[6] Hanan A. Mahmoud and Magdy.A. Bayoumi, "A 10-transistor low- power high-speed full adder cell," *IEEE International Con- ference on Nanotechnology*, vol. 1, pp. 43-46, 1999.

[7] Hung Tien Bui, Yuke Wang, and Yingtao Jiang, "Design and Analysis of Low-Power 10-Transistor Full Adders Using Novel XORXNOR Gates," *IEEE Transactions on Circuits and Systems* II*: Analog and Digital Signal Processing*, vol. 49, no. 1, pp.25-30, 2002.

[8] Jin-Fa Lin, Yin-Tsung Hwang, *et al.*, "A novel high-speed and energy efficient 10- transistor full adder design," *IEEE Transactions on Circuits and Systemsi: Regular Papers*, vol. 54, no. 5, pp. 1050-1059, 2007.

[9] Ning Zhu, Wang Ling Goh, Weija Zhang, Kiat Seng Yeo, and Zhi Hui Kong, "Design of Low-Power High-Speed Truncation-Error-Tolerant Adder and Its Application in Digital Signal Processing," *IEEE Transactions on Very Large Scale Integration (Vlsi)Systems*, vol. 18, no. 8, pp. 1225-1229, 2010.

[10] Chia-Hao Lin and Ing Chao Lin, "High accuracy approximate multiplier with error correction," IEEE Transactions on Circuit and Systems-I, vol. 52, no.11, pp. 33-38, 2005.

[11] Sangjin Hong, Suhwan Kim, Marios C. Papaefthymiou, *et al.*, "Low power parallel multiplier design for dsp applications through coefficient optimization," IEEE International Conference on VLSI Design, pp. 286-290,1999.

[12] V Jayaprakasan, S Vijayakumar, V S Kanchana Bhaaskaran, "Evaluation of the conventional vs. ancient computation methodology for energy ef- ficient arithmetic architecture," in *2011 International Conference on Process Automation, Control and Computing*, pp. 1-4, 2011.

[13] Chip-Hong Chang, Jiangmin Gu, and Mingyan Zhang, "Ultra low-voltage low-power cmos 4-2 and 5-2 compressors for fast arithmetic circuits," *IEEE Transactions on Circuits and Systems-I: Regular Papers*, vol. 51, no. 10, pp.1985-1997, 2004.
[14] Khaing Yin Kyaw, Wang Ling Goh, and Kiat Seng Yeo "Low-power high-speed multiplier for errortolerant application," *IEEE International Conference of Electron Devices and Solid-State Circuits (EDSSC)*, pp. 1-4, 2010.
[15] Zhixi Yang, Jie Han and Fabrizio Lombardi, "Approximate compressors for error-resilient multiplier design," *IEEE Transactions on Circuit and Systems-I*, vol. 63, no. 11, 2014.
[16] Naman Maheshwari, Zhixi Yang and Jie Han, Fabrizio Lombardi, *"A design approach for compressor based approximate multipliers," IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 24, no. 11, 2013.
[17] Parag Kulkarni, Puneet Gupta, Milos Ercegovac, "Trading Accuracy for Power with an Underdesigned Multiplier Architecture," *IEEE Computer Society,24th Annual Conference on VLSI Design*, pp 346-351, 2011.

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