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Modern design approach of faults (toggling faults,bridge faults and SAT) of reduced ordered binary decision diagram based on combo & sequential blocks

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ABSTRACT

In this Research we are going to develop ROBDD (Reduced Ordered Binary Decision Diagram) designs to detect toggling faults, bridge faults and SAT (Stuck at Fault), Here we are going to develop sequential blocks using ROBDD and applying to the mux to detect stuck at faults and also connecting the combo & Sequential blocks to find the toggling faults by connecting or using automatic test pattern generator. In this research we are going to develop the bridges between the blocks of ROBDD designs and converting them to and or logic to find the bridge faults of the design. Finding bridge and toggle faults are more difficult in logic designs, here we use an advance technique to find the faults of the design by calculating the path delays of the individual blocks of the design. More concentrating on the path delays by using basic stuck at faults methods to refer the faults (toggling and bridge faults) at mux output. In our research the basic design modules are ROBDD circuit of both combinational and sequential blocks are designed and tested using Multiplexer and K-map Simplification Methods. The main purpose of the research to find the faults at all levels of all logic designs which involves in both combinational and sequential blocks of the design.

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1. INTRODUCTION

Structure and test include an essential cost fragment during the time spent chip creating. During the time test arranged research has contributed on a very basic level in constraining test age effort and in the meantime achieving needed test results. Generally current scenario of the test cases is to be written to follow single stuck at faults. Assumption is that the SSAF test will effect the other failures, for instance, various stuck at and traverse issues with alluring incorporation. To consider tip top insufficiency representations further SSAF will provoke large test estimation times. A test circuit consider with fixed no ofn-nets ,will detect 3n-1 different multiple stuck faults(Multiple stuck at faults). It indicates unrealistic number to gather tests for. Various systems had been projected to give full different issue consideration to fan-out designs, irredundant multilevel circuit designs, and inward fan-out circuit designs [1-2]. Actuality designs have inside re-joined fan outs. Various works revolve aroundmultiple stuck at faults from the SSAF's [3-5].

Basically by the availability of SSAF test planto distinguish Multiple stuck at faults may diminish age effort of the test. By testing single stuck at faults we can observer approximately 80% of multiple stuck at faults .scientists observe the MSAF incorporation. Recently work done by [6] incorporates faults based definition for Automatic Test Patten Generator of circuits having tremendous of faults. Especially SAT figured critical situations are recognized by the faults in any case the relating prerequisites are not dropped. This empowers them to deal with the comprehending methodology all around viably. [7] Have proved that single accuse fault test is slight expansion for the multiple stuck at fault test, they use various branch computation to perceive MSAFs are not distinguished by not multiple test adhered to accuse tests. In any case, these proposed designs test circuit designs with everything taken into account for MSAFs inciting exponential test age unusualness.

Ensuring all out Single and multiple stuck at faults, and concede insufficiency testability through setup reduction in the setup stage configuration age time. This moreover prompts least structure modifications if there ought to emerge an event of forbidden issue consideration at a future stages. On to the other side, there had been a couple of plan philosophies bring up in the composition to improve design testability. Most of such systems Reduced Ordered Binary Decision Diagram (ROBDD) based circuit structure. For a Reduced Ordered Binary Decision Diagram based execution, every inside ROBDD center point is displaced either by a MUX design circuit or an IAX (invert and xor) sub-circuit. These amalgamation procedures offer maximum 99% percent testability towards SSAF and way concede weaknesses.

The strategy prefers more data, however slight compositional changes are being done to execute the additional information. In most the testing multiple stuck at faults designs uses a testing by ROBDD included muxes to be explored. Intensive design under testing equally covers complex inadequacies together with MSAFs and traverse weaknesses; in any case it may rise to ridiculous. A sensible method named Pseudo intensive testing was implemented by formal proposal by McCluskey et.al [8-10].Their suggestion was away for random number generation tests for eg: BIST models. Pseudo intensive testing framework had a very strong relevance to a ROBDD construct structure, normally detached in means of naturality. Test vectors age for this circumstance contains a polynomial equalized test age multifaceted nature. This endeavor displays a totally deferment and structure of testable MSAF design circuit areas. The huge duties of this research paper are:

A pseudo extensive test method to recognize every MSAFs includes ROBDD based circuit designs which consists of immaterial test age effort as shown in Figure 1. All non terminated inadequacies of the circuit under design for test are exhibited.

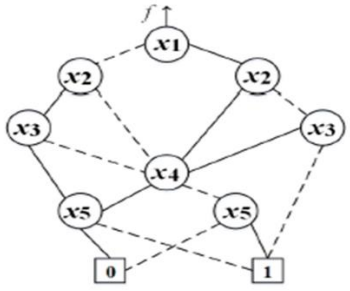


Figure 1. Boolean function representation using ROBDD

It is understood that test for all various stuck-at inadequacies at the passage posts is the one of high gauge yet the test can't be gotten by distinguishing proof of all of various defects. It is possible to avoid list only for special circuits. For example the circuit lead must be delineated with a course of action of irredundant wholes of things (prime includes of limits setting up the system) sought after utilization of stunned association methodology to such structure. For this circumstance the length of the test for all unique stuck-at inadequacies at the passage posts of the circuit gained isn't more than the amount of literals in the system and the amount of consequences of the structure. Different tests for stuck-at insufficiencies of the circuit are clearly gotten from the structure as shown from the Figure 2 and problem is we cannot reuse the same structure for finding multiple faults for sequential blocks more information briefed in literature survey of this paper. In this paper we found credibility to made test for all different stuck-at lacks at the CLBs (Configurable Logic Blocks) shafts (without tally of issues) for circuits surmised with covering Shared ROBDDs by CLBs in the packaging of FPGA development.

The rest of the research paper is structured as follows. Briefly elaborated related design works withproblems in Section II, Coming to the Section III explores an overview of the proposal method. The proposed techniques along with required hardware design structures and their resulted analysis are explored in Section IV. In Section V, the efficient outputs for high performance in detecting faults are compared with those of existing approaches. Finally, this research is closed in Section VI.

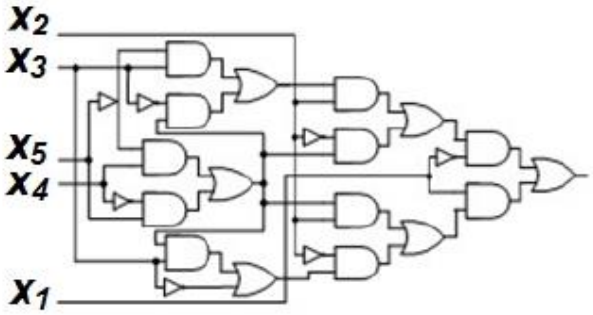


Figure 2. Or-based representation using ROBDD

2. LITERATURE SURVEY

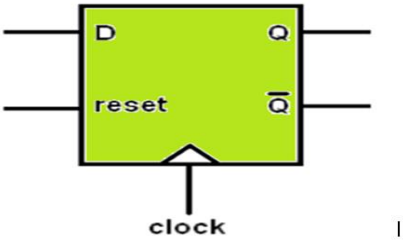
Most of the techniques are presented to detect small defects of fault detection using an extent of 2 level networks and mostly design experiments for detection of faults in multilevel networks also and with the same concept is redefined in this research shows that it contributes in developing the experiments and it enables to convert from one to another network which are seems to be same, by this it is easier to find the faults by developing experiments of fault detection. Now a days the problem of finding more faults is more critical and by our experiments it is very complicated to find faults , in this scenario , corresponding sum of products is not considered .most of the critical situations a fault table is preferred and tried to decrease the no of columns to decrease the memory to be stored in table, to create this experiment more strong for networks with large amount of inputs, a different techniques is used for reduction of no of rows in table, a brief table proves and used for detection of faults easily by understanding and detection of small amount of paths which re-converges every time. Once the re-converging paths are tested, then the only part remaining to be tested are inputs [11].Major disadvantage of the present synthesis technique is drop in coverage delay of the path in circuits. Various objective functions are calculated for BDD to decrease hardware complexity; these are evaluated by testing existing circuit design patterns. With respect to the PDFM is proved that by reduction of paths in BDD can decrease the testing patterns for testing the circuit. Considering a variable objective functionalities are used to consider more than one hit during synthesis and to get compromised e.g. between size and no of test patterns are used.as far we discussed about drawback of current synthesis is due to the delay in circuits of coverage delay paths. Focus is to combine the proposed system design work with the multiplexer design circuits, which guarantees 100% testing to be done under PDFM and SAFM within the cost of added inputs [12]. Major drawback is the drop in the stuck at faults & delays fault coverage for some circuits. ATPG techniques for detection of multiple stuck-at faults with hidden representation of faults are listed. The algorithm is essentially doing the same as the techniques, any how the targets are different. Problems are solved with applications of SAT repeatedly but the problems are solved naturally expressed as QBF,a quantified Boolean formula used to solve the problem in natural way.During the research determined that problems can be called as incrementing SAT problems instead of using as QBF which is easy to understand. We don't a large amount of test vectors to test either multiple or single stuck at faults ,an easier way to test is to take top set of the test vector for finding the faults ,this has proven in research analysis.In the research areas it proves that by applying or changing some formulas at ATPG level we can find the faults ,which is easier way to represent single stuck at faults along with this we can detect other faults like toggling faults and bridge faults. Many other faults also detected by these experiments. The limitation of the research is to make synthesizable its more complexes and the design has to be added with more combinational blocks. In this research a different method as described for initial BDD circuits. From this resulted Circuits are fully testable under SAFM and robust PDFM. Mainly one alternation is needed to develop as program of MuTaTe [13] by adding and additional input and an inverter to reduce the binary decision diagrams.

3. PROPOSAL

The basic plan of the research method is to design and test a sequential circuit using ROBBD technique by applying few test vectors for cor ner cases of design.

4. PROPOSED TESTING METHOD

Let us consider a simple Sequential circuit DFF as shown in Figure3 and also shown an example of simplification of an equation into binary decision diagram in Figure 4.With the same process convertion of Figure 3 to binary decision diagram is shown in the Figure 5.



Input			Output
D	reset	clock	Q
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0

Figure 3. Sequential block with truth table

Q=D.(~R).Clock

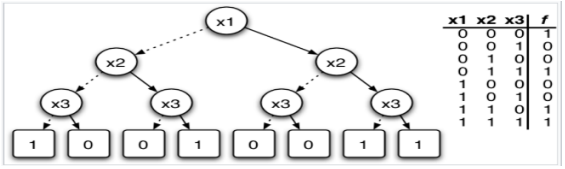


Figure 4. Simplification to binary decision diagram

F=x1~x2x3

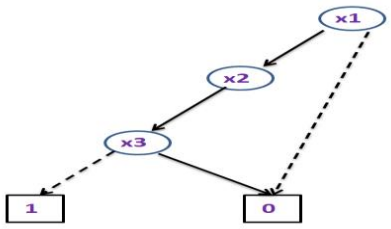


Figure 5. Simplification to reduced ordered binary decision diagram

A sequential circuit [14] is resolved with covering the most ideal Shared ROBDD by CLBs in the packaging of FPGA development. Single stuck-at defects at the CLBs shafts and various insufficiencies set up from such single stuck-at issues are considered. It is exhibited that the test structure as for single adhered to fault so for different issue there reliably exists. The test structure for a various lack is the unprecedented test plan for the exceptional single adhered to accuse forming the distinctive one. Test for all of different issues is gotten from any test for all single stuck-at issues. The length of the various defects test is immediate limit of the single inadequacies test length. A different insufficiency test is the one of high bore. Explicitly SEU and framework imperfections may show themselves as different weaknesses at the CLBs posts. Deciding test for all of different lacks was executed for the particular seat marks. For them the length of the various inadequacies test is about the twice length of the single insufficiencies test.

Consider a master slave edge triggered flipflop design and calculating faults of the designs with the control signals and shown the normal mode of operation is shown in the Figure 6 with the required settings.

– Normal Mode: pC1=0, pC2=1, nC1=0 and nC2=1.
– pC1=0, pC2=1-> Copies the output of the positive enable D latch
– Used for avoiding fanout issue
– nC1=0, nC2=1-> copies the output of the negative enable D
– used for avoiding fanout issue

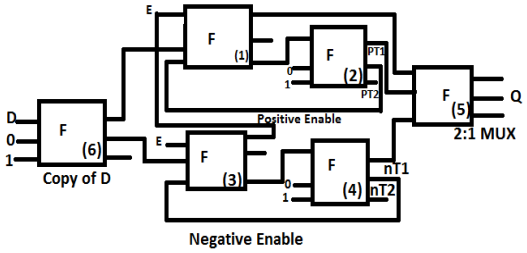


Figure 6. Normal mode operation

Test Mode:Figure 7 points the test mode operation 1 which performs the operation based on below configuaration.
All 1s Test Vectors:
pC1=1,pC2=1,nC1=1 and nC2=1.
pC1=1 and pC2=1-> Breaks the feedback of the positive enable D latch
nC1=1 and nC2=1-> Breaks the feedback of the negative enable D

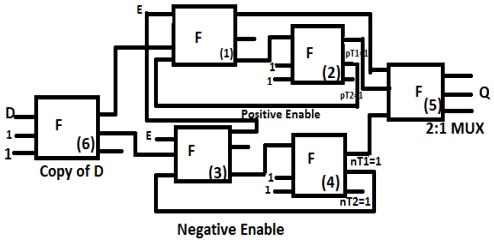


Figure 7. Test mode operation 1

Test Mode: Below configuaration settings are used to perform test mode operation 2 which is shown in Figure 8.
All 0s Test Vectors:
pC1=0,pC2=0,nC1=0 and nC2=0.
pC1=0 and pC2=0-> Breaks the feedback of the positive enable D latch
nC1=0 and nC2=0-> Breaks the feedback of the negative enable D

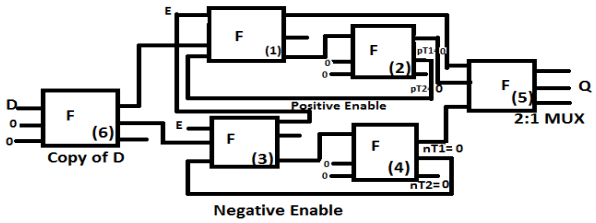


Figure 8. Test mode operation 2

f 1=$\bar{A}$B+AC ,f2= AB+$\bar{A}$C,When A=0,B=1,f1=1,f2=1

When control signals are 1's and 0's can be used to detect stuck at faults and final results based on test mode configuarations are shown in Table 1.

Table 1. Final results taken from the test mode operation 1 &2

D	E0	E1	PT1	PT2	nT1	nT2	Q
0	0	1	0	0	0	0	0
1	0	0	0	0	0	0	1
0	1	1	1	1	1	1	0
1	1	0	1	1	1	1	1

As development scales, close to nothing and thick geometries, and strategy assortments present flaws, routinely not perceived by testing levels at stuck at faults of single. To develop disfigurement consideration, expanding the single clung at testing methods of various tests to detect various stuck-at fault issues. This research paper brings all about testing a sequential design circuit for finding the faults of MSAF using ROBDD usage .The circuits are investigated at the center points of the ROBDD with DFF (2X1 multiplexers). We exhibit that for each single sub design circuit which goes about a fragment, the various adhered to accuse by four vectors for single tests set .Besides it shows different adhered to accuse set of tests. In which circuits consists of 3N test vectors for the Upper bound , N represents the exact centered point for addressing ROBDD design circuit.

A sequential circuit is resolved with covering the most ideal Shared ROBDD by CLBs in the packaging of FPGA development. Single stuck-at blemishes at the CLBs shafts and various lacks built up from such single stuck-at issues are considered. It is shown that the test plan as for single adhered to fault so for different issue there reliably exists. The test structure for a various inadequacy is the remarkable test plan for the phenomenal single adhered to accuse forming the distinctive one. Test for all of different issues is gotten from any test for all single stuck-at issues. The length of the various blemishes test is immediate limit of the single inadequacies test length. A different lack test is the one of high bore. Explicitly SEU and framework [15-18] imperfections may show themselves as different inadequacies at the CLBs posts. Deciding test for all of different insufficiencies was executed for the particular seat marks. For them the length of the various weaknesses test is about the twice length of the single inadequacies test.

As the colossal multiplexers need not be execute as it disappoints the act of speed and these are very expensive. As proven ROBDD based experiment it addresses a 2 fold tree structure ,a no of added multiplexerscan be decreased.As shown in the below Figure 9, each of the centered point is executed using sub design circuit as we preferred as multiplexer,it proves that mux is a trade mark for the entire design circuit for testability.From the point of the fundamentals ,multiplexer inputs and it moves to the respected circuit that must improve and must and should provide faults.by this mux is will completes it's process fully. ROBDD centered execution are surrounded with all the things to be testable for the weakness designs, producing and improving must to be ensured in either way. Drives the basic inputs from the mux of test vectors so as to detect and improve the insufficient inputs to design and make the design equivalent to the required improvement.

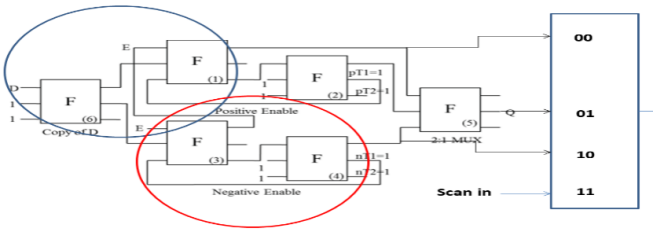


Figure 9. Identified test patterns in the design

Stuck at fault

An adhered to particular fault weakness design used with issue test frameworks along with themodified test configuration age (ATPG) gadgets to copy a collecting distortion inside a consolidated design. Separate banner and sticks are believed to be stuck at Logical values (1,0,x). Considering with an

example, a data is connected to a steady state ,particularly the test age to ensure that a gathering distortion with that sort of lead could be collected with particular test plan. In like way the data could be connected to an intelligible 0 to model direct of a effected design that can't do any kind of adjustment its yield stick. Everything may not be issues could be examined by the adhered to accuse design. Pay for hazards which are to be static, specifically growing sign, may rise to untestable design using the main design usage. Furthermore, abundance design circuit can't be had a go at particular design, thereby arrangement no alteration in no yield as a outcome of a solo blemish.

Line at the Single stuck

Line at single stuck is a lack model present in automated designs. Most of designs used for after the testing, not an arrangement test. The modern design acknowledge single line or center point in the propelled stuck at design by method of reasoning huge or justification medium. Blemish indicates that when at a particular stuck happens at a line.

4.1. Mechanized designs disconnected further more to:

a. Small designs level or sequential designs have no limitations (locks and also flipflop disappointments) yet just doors like DFF, TFF, MSFF etc.
b. Sequential designs contain an amassing.

An issue design [19] applies to gateway level design blocks, or a square of a back to back design can be disconnected with the limit segments. Preferably an entryway level design might be totally attempted by adding each and every conceivable information and watching that they gave the right yields, anyway this is absolutely preposterous: a snake to incorporate two 32-bit valued nums need 264 = (0.8+1)*1019tests needed, taking 68 years at 0.1 ns/t. The adhered to accuse model acknowledge that particular commitment on one entryway to be broken without a moment's delay, expecting that are imperfect, a required test can perceive any non multiple issues, may be easily find different inadequacies.

To prefer this weakness modeled design, every data stick every entryway therefore, is believed to be stuck, and a test path is made to exhibit the design is broken. The test path of the vector is a social event of vectored bits to add to the design's wellsprings of information, and a group of bits predictable at the designs yield. The gateway stick below idea is grounded, test vectorassociated with the design, in any occasion any of the yield bit's won't decide with the looking at yield vector bits of the test. In the wake of getting the test vectors are applied for the pins which are grounded , every stick is related in this mannered method of reasoning one to the next course of action of test vectors used for detect issues happening under these circumstances . All of these inadequacies is known as a lone stuck at faults (1,0) weakness, independently.

Presented design worked well for TTLmethod of reasoning (Transistor Transistor Logic), it was the justification of optimal during the earlier generation(1980s), that producers broadcasted howthey have attempted with their designs by number called "adhered to accuse incorporation", which addressed the degree at all likely stuck at faults inadequacies with the testing strategy would have find. With respect to a comparative testing modeled design starts sensibly well for C Metal Oxide Semiconductors, then it can't recognize all possible CMOS lacks. This is in light of the fact that semiconductor may find or detect a mistake mode known as a SOD "stuck-open defect", it can't constantly perceived by one test and requires additional test vectors to be associated progressively. The designs once fails to recognize crossing weaknesses among neighboring sign lines, arising in pins that determination transport affiliations which group structures. Incidentally, single stuck at fault imperfections are extensively preferred and with few more tests has empowered manufacturing send an agreeable to no of horrendous circuits. Testing subject to this modeled design is helped to a couple of items:

a. Test delivered to singular adhered to defect as frequently as possible detects incalculable further stuck at defects.
b. Course of action of scenario's for stuck at faults issues oftentimes, just to the extent karma, detect incalculable various inadequacies, for instance, stuck-open issues. This is now and again called "advantage" lack incorporation.
c. Different kind of scenario of test to be called as IDDQ gauges the path wherein the PS current of a cmos joined design reflects when couple of emerging test vectors is associated. Since MOS attractions for an amazingly low power then it wellsprings of data are unique, further development in power shows a reasonable potential issue.

Another system that uses various and single issues reenactments to break down different adhered to fault in sequential circuits is depicted. This strategy has the doubt that all estimated inadequacy are also likely in the defective circuit, different issue multiplications are performed. Inadequacies are incorporated or removed from a particular course of action of suspect insufficiencies, is depended upon the diverse imperfection reenactment results that the basic yield regards have agreed with the watched characteristics or

not. Insufficiencies which are incorporated or ousted from the ser of suspected inadequacies are settled using single issue proliferation. The technique is suitable of examination has been evaluated by test driven on benchmark circuits, which achieves few theorized lack by clear getting ready. This procedure will be profitable for preprocessing period of investigation using the electron column analyzer.

For the Figure 10 design apply different test vectors inputs . By the control signals as mentioned in the Figure 7 & Figure 8 test cases find faults and also applied ROBDD simplification to mux ,When mux indicates values as 1 indicates fault occurred at some level as expected '0' as resultant as from the Figure 10 blue rectangle box indicates faults as an example part of the design. Vectors applied for the design as per the design requirements to be verified.

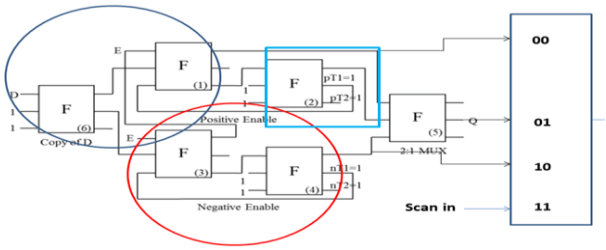


Figure 10. Identified test patterns in the Design for detection of the faults using different test vectors

5. RESULTS AND DISCUSSION

In the Figure 11a, waveform it shows normal operation of dff without any control signals to be considered and it shows effective result of D-FF and Figure 11b, waveform shows occurrence of stuck at faults

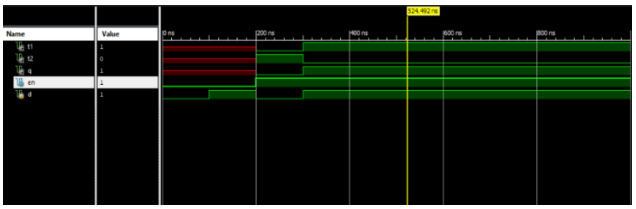


Figure 11a. Normal operation of DFF

Figure 11b. Stuck at '1' operation of DFF

From the Figure 11c, when there is loss of connection between the bridges the result shows as below waveform in which expected result is not equivalent to the outcome.

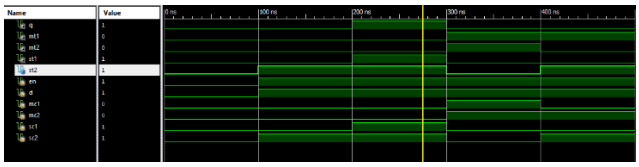


Figure 11c. Bridge fault (loss of connection)

From the Figure 11d waveform, when the resultants are toggle for the expected results ,it shows there is fault as toggle fault which is proven from the circuit with control signals

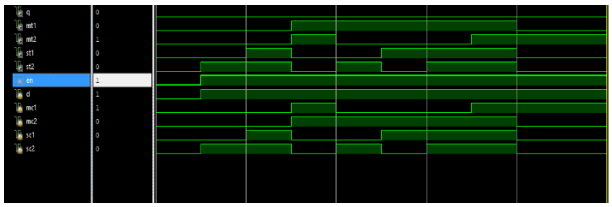


Figure 11d. Toggle fault waveform

From the Figure 12 it shows the area of the spartan6 fpga ,which is very less compared to the existing design under tests and also we can see the CLB part which covered in FPGA from the Figure 12 a.

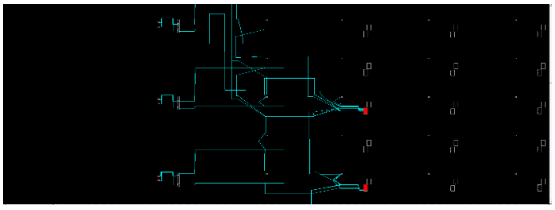


Figure 12. Area covered using configuarable logic blocks

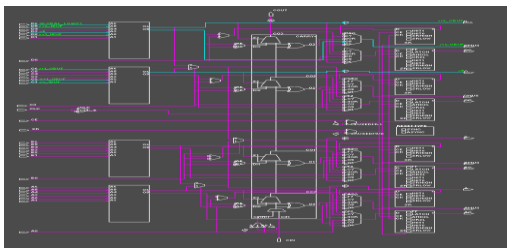


Figure 12 a.Routed design in FPGA

From the Table 2 it shows that by using ROBDD techniques we can find the faults more ,can detect and probably correct it at initial stage before reaching to the tapeout of the design.

Table 2.Comparision of various testing methods

Method	GATE count	Delay(ns)	Faults	Approx.Efficiency
DET [20]	10	1.508	1	80%
MS Mode[20]	14	0.923	2	80%
Stuck at 0[20]	6	0.832	1	90%
Stuck at 1[20]	8	0.930	1	90%
Normal mode [20]	17	1.702	1	95%
ROBDD	15	0.859	>2	95%

6. CONCLUSION

According to the modified research, modern tests for stuck at fault detections are unsatisfactory to detect the faults in multiple stuck at faults, bridge faults and also toggling faults.(MSAF,BF&TF) signs and in this research came across finding the faults for MSAF,TF&BF.ROBDD based synthesized circuit to be consider for testing single stuck at faults with delay fault detection and shown the comparison with different techniques in Table 2.By partitioning we can find the faults in toggling and bridge faults also using an additional component into the design as 2x1 multiplexer. The partitioned tests set consists of eight test vectors at the resultant polynomial time limit. Considering 4N as the length of test, N represents internal nodes of the top design (ROBDD) which describes circuit behavior. As far we know the test bring up effort at MSAF, TF&BF's, all faults are automatically covered. Hence we can reduce area compare to the existing research of ROBDD.

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