ISSN: 2089-4864, DOI: 10.11591/ijres.v9.i2.pp116-124

# Design and analysis of different full adder cells using new technologies

Nandhaiahgari Dinesh Kumar<sup>1</sup>, Rajendra Prasad Somineni<sup>2</sup>, CH. Raja Kumari<sup>3</sup>

Department of Electronics and Communication Engineering, Vallurupalli Nageswara Rao Vignana Jyothi Institute of Engineering and Technology (VNR VJIET), India

#### **Article Info**

#### Article history:

Received Nov 21, 2019 Revised Jan 31, 2020 Accepted Mar 03, 2020

#### Keywords:

CNTFET
Delay and HSPICE Tool
Full Adder Cell(FAC)
GNRFET
MN modified mux
Power dissipation
TG modified mux

#### **ABSTRACT**

CMOS transistors are most widely used for the design of computerized circuits, when scaling down the nanometer technology these devices faces the short channel effects and causes I-V characteristics to depart from the traditional MOSFETs, So the researchers have developed the other transistors technologies like CNTFET and GNRFET. Carbon nanotube field effect transistor is one of the optimistic technologies and it is a three terminal transistor similar to MOSFET. The semiconducting channel between the two terminals called source and drain comprises of the nano tube which is made of carbon. Graphene nano ribbon filed effect transistor is the most optimistic technology here the semiconducting channel is made of graphene. When contrasted with barrel shaped CNTFETs, GNRFETs can be prepared in situ process, transfer-free and silicon compatible, thus have no passage related and alignment problems as faced in CNTFET devices. This paper presents different 1-bit Full Adder Cells (FACs) like TG MUX-based FAC (TGM), MN MUX-based FAC (MNM), proposed TG Modified MUX-based FAC (TGMM) and another proposed MN Modified MUX-based FAC (MNMM) are designed using different technologies like CNTFET and GNRFET at 16nm technology with supply voltage of 0.85v and simulation is done by using Synopsys HSPICE Tool and the proposed designs are best when compared to the TGM and MNM FACs in terms of Static and Dynamic powers Dissipations and Delay.

This is an open access article under the <u>CC BY-SA</u> license.



116

#### Corresponding Author:

Nandhaiahgari Dinesh Kumar,

Department of Electronics and Communication Engineering,

Vallurupalli Nageswara Rao Vignana Jyothi Institute of Engineering and Technology (VNR VJIET),

Telangana, India.

Email: dineshkumarnandhaiahgari@gmail.com

#### 1. INTRODUCTION

The booming demand for low power in very largescale integration (VLSI) can be seen at distinctive block levels, such as process technology, circuit, structure, and the layout level. The FACs are the fundamental building blocks of the ALU circuits. CMOS transistors are most widely used for the design of computerized circuits, when scaling down the nanometer technology these devices faces the short channel effects and causes I-V characteristics to depart from the traditional MOSFETs, so the researchers have developed the other transistors technologies like CNTFET and GNRFET. By using the CMOS technology the values are not optimal and by using the CNTFET and GNRFET technologies the optimal values can be observed. The different FACs are designed by using the multiple threshold voltages for different transistors in the design [1]. Majority function or threshold function it gives output as logic '1' when more number of inputs are '1' based on the logic level the multiple threshold voltages are obtained. The diameter of the CNT

Journal homepage: http://ijres.iaescore.com

is controlled by varying the chirality vector based on the diameter the threshold voltage could be varied [2]. GNRs can be prepared in situ process, transfer-free and silicon compatible, thus have no passage-related and alignment problems as faced by CNTFET devices [3].

The proposed designs are designed by using the CNTFET and GNRFET technologies with transmission gate logic in TGMM FAC and Majority function logic in MNMM FAC and here the Dynamic and Static power dissipation's and Delays are low. In the proposed design the modification is made in the MUX logic circuitry.

The TGM FAC [4] is designed by using the 25 transistors, MNM FAC [5] is designed by using the 26 transistors, proposed TGMM FAC is designed only by using the 23 transistors and another proposed MNMM FAC is designed only by using the 18 transistors. This paper is structured as follows Section-2 presents the Review of CMOS, CNTFET and GNRFET. Section-3 tells about the design of different FACs. Section-4 shows the comparative analysis of different FACs. Section-5 is done with the conclusion of the paper.

# 2. REVIEW OF CMOS, CNTFET AND GNRFET

The CMOS transistor are the basic and most widely used for the design of computerized circuits, As nano meter of the transistor is decreasing, chip thickness and working frequency is enlarged, making power utilization in battery-worked handy devices a significant concern. CNTFET show a considerable advantage over the CMOS. Both P and N type CNTFET transistors have the analogous mobility. Sizing of transistors in complex advanced devices based on CNTFETs would be simple compared to CMOS devices. Considering the properties like electrical characteristics, for example, ballistic transport and low Off-Current of CNTFETs empowers rapid and low power circuit structures [6].

In CNTFETs the edge potential of the transistor is relying upon the width of the CNTs by varying the chirality vector the threshold voltage can be altered. CNTs play a vital role in the design of the integrated circuits in the future due to their uncommon electrical and mechanical properties as compared with CMOS devices. CNT transistors are divided into 2 types single wall (SWCNT) and multi wall (MWCNT) [7]. Single wall CNTFET consists of one barrel whereas the multi wall has more than one barrel. The structure of the CNTFET is shown in the Figure 1. The carbon nanotubes materials are quiescent devices to substitute si in the low power.

Channel length of a CNTFETs could be decreased to five nano meters before tunneling temperature brings a undesirable drop in currents. Diameter of a CNTFET is similar to arrangement of the amount of tubes [8]. Graphene is a two-dimensional layer of carbon atoms having 2D honey-comb lattice. The most attractive feature of Graphene is high carrier mobility which renders faster switching times and GNRs are ultra-thin sheets of graphene support one-dimensional ballistic transport of charge carriers. Graphene is categorized into 2 types monolayer, bilayer or multilayer Graphene. In the bilayer Graphene band-gap can be induced to make it semi-conducting.

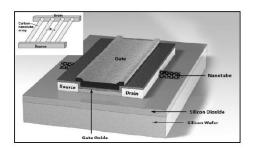


Figure 1. CNTFET transistor structure

GNRFET have emerged to replace the traditional silicon transistors in scaled technologies[9], Since these devices are very small and effect of course variation on the circuit performance is very large. The most researched are carbon nano-tube FETs (CNTFETs) and Graphene nano-ribbon FETs (GNRFETs), When contrasted to barrel shaped CNTs, GNRs can be prepared in situ process, transfer-free and silicon compatible, thus have no passage-related and alignment problems as faced by CNTFET devices. The GNRFET transistor structure is shown in the Figure 2.

In GNRFET number of dimmer lines determine the width. There are two sorts of GNRFETs Schottky barrier (SB) GNRFET and MOS like GNRFET [10]. SB type uses metal to shape contacts along

118 🗖 ISSN: 2089-4864

these lines keeping away from fundamental extra doping. In any case, the SB type GNRFETs offer particularly less Ion to Ioff proportion when contrasted and the MOS type GNRFET.

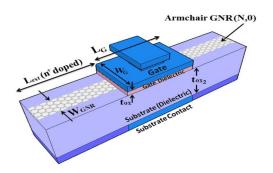


Figure 2. GNRFET transistor structure

# 3. DESIGN OF DIFFERENT FAC'S USING NEW TECHNOLOGIES

This section discusses the design of different 1-bit FACs like TG MUX-based FAC (TGM), MN MUX-based FAC (MNM), proposed TG Modified MUX-based FAC (TGMM) and another proposed MN Modified MUX-based FAC (MNMM) are designed using different technologies like CNTFET and GNRFET.

#### 3.1. TG MUX-based FAC (TGM)

The TGM 1-bit FAC is designed using the CNTFET and GNRFET technologies. Here the FAC consists of transmission gates. The circuitry consists of different levels, in the first level NOT logic operation, the second level AND and OR logic operation to them A, B inputs are given, the third level will be having XOR/XNOR logic operation and finally fourth level MUX's logic operation, to the MUX's logic C is given as input and output from the MUX's are SUM and CARRY. The CNTFET design parameters are pitch: 6nm, tubes: 3, Kox: 16, Hox: 4nm, Lg: 16nm, Cb: 100nm and Efo: 0.6.

The TGM 1-bit FAC is designed by using the GNRFET technology with the GNRFET transistors. The different design parameters for GNRFET technology are nRib: 6, N: 6, Tox: 0.6nm, dop: 0.001, L: 16nm and Tox2:20nm. The total numbers of transistors used for the design are 25. The TGM 1-bit FAC in GNRFET technology is shown in the below Figure 3.

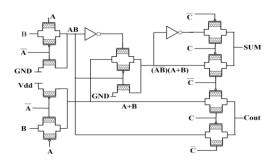


Figure 3. TGM 1-bit FAC in GNRFET technology

# 3.2. Proposed TG modified MUX-based FAC (TGMM)

The block diagram describes the implementation of the FAC, the block diagram is shown in the below Figure 4. The FAC is implemented in different levels, in the first level NOT logic operation, the second level AND and OR logic operation, the third level will be having XOR/XNOR logic operation and finally fourth level MUX's logic operation. In this proposed design the modification is made in the MUX design.

The Proposed TGMM 1-bit FAC is designed using the CNTFET and GNRFET technologies. Here the FAC is implemented by transmission gates. The circuitry consists of different levels, in the first level

NOT logic operation, the second level AND and OR logic operation to them A, B inputs are given, the third level will be having XOR/XNOR logic operation and finally fourth level MUX's logic operation, to the MUX's logic C is given as input and output from the MUX's are SUM and CARRY. Design parameters for the Proposed TGMM CNTFET 1-bit FAC are pitch:6nm, tubes:3, Kox:16, Hox:4nm, Lg:16nm, Cb:100nm and Efo:0.6.

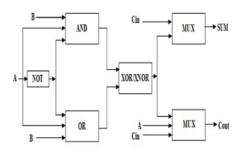


Figure 4. Block diagram of proposed TGMM 1-bit FAC

The Proposed TGMM 1-bit FAC is designed by GNRFET technology with the GNRFET transistors and the design parameters are nRib: 6, N: 6, Tox: 0.6nm, dop: 0.001, L: 16nm and Tox2:20nm. The total numbers of transistors used for the design are 23. The Proposed TGMM 1-bit FAC in GNRFET technology is shown in the below Figure 5.

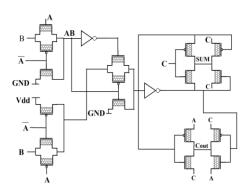


Figure 5. Proposed TGMM 1-bit FAC in GNRFET technology

#### 3.3. MN MUX-based FAC (MNM)

The MNM 1-bit FAC is designed using the CNTFET and GNRFET technologies, The MNM 1-bit FAC is shown in the below Figure 6. The operation of the MNM 1-bit FAC have majority function or threshold function it gives output as logic '1' when more number of inputs are '1' based on the logic level the multiple threshold voltages are obtained. The circuitry consists of different levels, in the first level Majority logic operation to them A, B inputs are given, the second level NAND logic operation, the third level will be having XOR/XNOR logic operation and finally fourth level MUX's logic operation, to the MUX's logic, A and C is given as input and output from the MUX's are SUM and CARRY. Here the total numbers of transistors used for the circuit design are 26. The CNTFET design parameters are pitch: 6nm, tubes: 3, Kox: 16, Hox: 4nm, Lg: 16nm, Cb: 100nm and Efo: 0.6.

The MNM 1-bit FAC is designed by GNRFET technology with the GNRFET transistor. The different design parameters for GNRFET technology are nRib: 6, N: 6, Tox: 0.6nm, dop: 0.001, L: 16nm and Tox2:20nm.

120 ISSN: 2089-4864

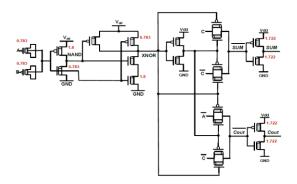


Figure 6. MNM 1-bit FAC in CNTFET Technology

#### 3.4. Proposed MN modified MUX-based FAC (MNMM)

The block diagram describes the implementation of the Proposed MNMM 1-bit FAC, the block diagram is shown in the below Figure 7. The operation of the proposed FAC have the majority function or threshold function it gives output as logic '1' when more number of inputs are '1' based on the logic level the multiple threshold voltages are obtained. The first level is majority logic operation, the second level NAND logic operation; the third level will be having XOR/XNOR logic operation and finally fourth level MUX's logic operation. In this proposed design the modification is made in the MUX design.

The MNM 1-bit FAC is designed using the CNTFET and GNRFET technologies. The Proposed MNM CNTFET 1-bit FAC is shown in the below Figure 8. The operation of the FAC have the first level is majority logic operation to which A, B inputs are given, the second level NAND logic operation, the third level will be having XOR/XNOR logic operation and finally fourth level MUX's logic operation, A and C is given as input and output from the MUXs are SUM and CARRY. Here the total numbers of transistors used for the circuit design are 18. The CNTFET design parameters are pitch: 6nm, tubes: 3, Kox: 16, Hox: 4nm, Lg: 16nm, Cb: 100nm and Efo: 0.6.

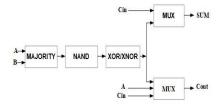


Figure 7. Block diagram of Proposed MNM 1-bit FAC

The Proposed MNM 1-bit FAC is designed by GNRFET technology with the GNRFET transistor and the design parameters for GNRFET technology are nRib: 6, N: 6, Tox: 0.6nm, dop: 0.001, L: 16nm and Tox2:20nm.

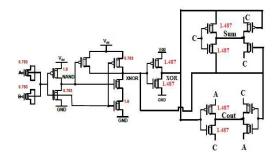


Figure 8. Proposed MNM 1-bit FAC in CNTFET Technology

#### 4. COMPARATIVE ANALYSIS OF DIFFERENT 1-BIT FAC'S

This section discusses the comparative analysis of different 1-bit FACs like TG MUX-based FAC (TGM), MN MUX-based FAC (MNM), proposed TG Modified MUX-based FAC (TGMM) and another proposed MN Modified MUX-based FAC (MNMM) are designed using different technologies like CNTFET and GNRFET. These designs are simulated using Synopsys HSPICE tool at 16 nm technologies with 0.85V supply and the performance parameter values of propagation delay, dynamic and static powers are tabulated in Table 1.

# 4.1. TG MUX-based FAC (TGM)

The analysis of TGM 1-bit FAC with CNTFET and GNRFET technologies which are discussed in section 3 are simulated and analyzed. Simulation results of TGM GNRFET 1-bit FAC are shown in Figure 9. The operation of the circuit is obtained as per the functionality of the FAC truth table.

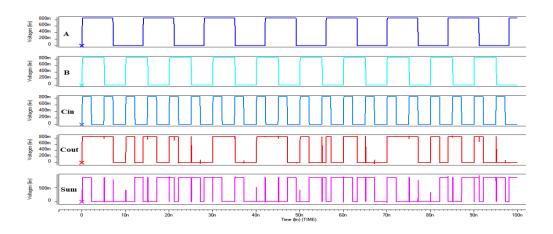


Figure 9. Simulation waveform for TGM GNRFET 1-bit FAC.

# 4.2. Proposed tg modified MUX-based FAC (TGMM)

The analysis of Proposed TGMM 1-bit FAC with CNTFET and GNRFET technologies which are discussed in section 3 are simulated and analysed. Simulation results of Proposed TGMM GNRFET 1-bit FAC are shown in Figure 10. The operation of the circuit is obtained as per the functionality of the FAC truth table.

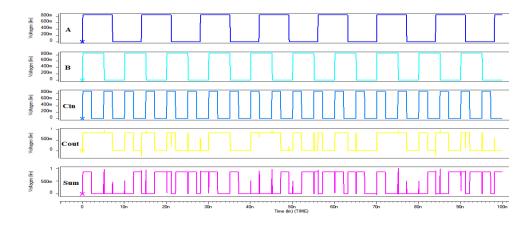


Figure 10. Simulation waveform for Proposed TGMM GNRFET 1-bit FAC.

122 ISSN: 2089-4864

#### 4.3. MN MUX-based FAC (MNM)

The analysis of MNM 1-bit FAC with CNTFET and GNRFET technologies which are discussed in section 3 are simulated and analysed. Simulation results of MNM CNTFET 1-bit FAC are shown in Figure 11. The operation of the circuit is obtained as per the functionality of the FAC truth table.

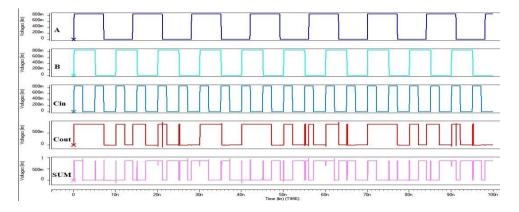


Figure 11. Simulation waveform for MNM CNTFET 1-bit FAC.

#### 4.4. Proposed MN modified MUX-based FAC (MNMM)

The analysis of MNMM 1-bit FAC with CNTFET and GNRFET technologies which are discussed in section 3 are simulated and analysed. Simulation results of MNM CNTFET 1-bit FAC are shown in Figure 12. The operation of the circuit is obtained as per the functionality of the FAC truth table.

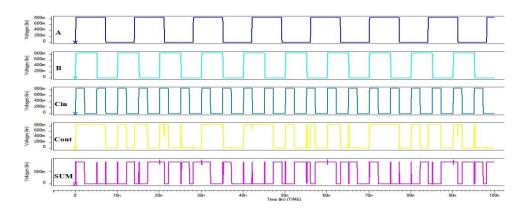


Figure 12. Simulation waveform for Proposed MNMM GNRFET 1-bit FAC.

From Table 1, it is clear that the TGMM GNRFET FAC has the 27% better speed performance than TGMM CNTFET FAC. Dynamic Power Dissipation of TGMM GNRFET FAC is 17% less than Dynamic Power Dissipation of TGMM CNTFET FAC. Static Power Dissipation of TGMM GNRFET FAC is 19% less than TGMM CNTFET FAC Static Power Dissipation.

Table 1. Comparative analysis of different FACs in new technologies

Parameters	TGM		TGMM		MNM		MNMM	
	CNTFET	GNRFET	CNTFET	GNRFET	CNTFET	GNRFET	CNTFET	GNRFET
Propagation Delay(ns)	0.0224	0.0212	0.0210	0.0153	2.1069	0.0179	1.3286	0.01182
Dynamic Power(nw)	32.933	23.430	19.963	16.435	66.928	59.235	27.097	25.021
Static Power(nw)	33.657	25.061	20.967	16.909	61.381	58.138	26.558	23.432

MNMM GNRFET FAC has the 99% better speed performance than the MNMM CNTFET FAC. Dynamic Power Dissipation of MNMM GNRFET FAC is 7% less than the MNMM CNTFET FAC. Static power Dissipation of MNMM GNRFET FAC is 11% less than that of the MNMM CNTFET FAC, From the over all comparison the MNMM GNRFET based FAC is better one.

The proposed designs TGMM FAC and MNMM FAC designs have less Dynamic and Static Power dissipations and Delays when compared with the existing designs TGM FAC and MNM FAC in both the CNTFET and GNRFET technologies.

Finally from the table it is clear that TGMM GNRFET FAC is better than TGM GNRFET FAC and MNMM GNRFET FAC is better than MNM GNRFET FAC. Also it can be concluded that GNRFET technology is better when compared to CNTFET technology.

# 5. CONCLUSION

This paper presents the Design and Comparative Analysis of different FACs using CNTFET and GNRFET Technologies and the design is simulated using the Synopsys HSPICE tool at 16nm technology with supply voltage of 0.85v. The performances of all these designs are compared in terms of Propagation Delay, Static Power Dissipation and Dynamic Power Dissipation. The TGM 1-bit FAC is analysed in CNTFET and GNRFET technologies. The TGM 1-bit FAC is designed by using 25 transistors where as in the TGMM FAC which is newly designed by using only 23 number of transistor. The TGMM FAC is designed by modifying the MUX logic circuitry. The MNM 1-bit FAC is analysed in the CNTFET and GNRFET technology and it is designed by using 26 transistors. The MNMM 1-bit FAC is analysed in the CNTFET and GNRFET technologies and it is designed by using only 18 number of transistors. Thus Proposed designs TGMM and MNMM FACs are best in terms of Power dissipations, delay and the transistor count.

#### REFERENCES

- [1] Mojtaba Maleknejad, et al., "A Low Power High Speed Hybrid Multi-Threshold Full Adder Design in CNFET Technology," *Journal of Computational Electronics*, vol. 17, no. 2, Apr 2018.
- [2] M. Mohammadi Ghanatghestani, B. Ghavami, and H. Salehpour, "A CNFET full adder cell design for high-speed arithmetic units," *Turkish Journal of Electrical Engineering & Computer Sciences*, vol. 25, pp. 2399-2509, 2017.
- [3] Deng, J and Wong, H. S. P, "A circuit-compatible SPICE model for enhancement mode carbon nanotube field effect transistors," *International Conference on Simulation of Semiconductor Processes and Devices*, pp. 166-169, 2006
- [4] Dr. Rajendra Prasad Somineni, Sai, Y Padma Sai Leela, and S Naga, "Low leakage CNTFET full adders," in *IEEE* 2015 Global Conference on Communication Technologies (GCCT), pp. 174-179, 23-24 Apr 2015.
- [5] Dr. Rajendra Prasad Somineni and Shaik Mohammed Jaweed, "Design of Low Power Multiplier Using CNTFET," 2017 IEEE 7th International Advance Computing Conference (IACC-2017), Hyderabad, pp. 556-559, Jan 05-07 2017.
- [6] Mokhtar MOHAMMADI GHANATGHESTANI, Behnam GHAVAMI, Honeya SALEHPOUR, "A CNFET full adder cell design for high-speed arithmetic units," *Turkish Journal of Electrical Engineering & Computer Sciences* vol. 25, pp. 2399-2409, 2017.
- [7] Majid Amini-Valashani, Mehdi Ayat, and Sattar Mirzakuchaki, "Design and analysis of a novel low-power and energy-efficient 18T hybrid full adder," *Microelectronics Journal*, vol. 74, pp. 49-59, 2018.
- [8] Stanford University, CNFET Model. [Online] Available: http://nano.stanford.edu/model.php?id=26. 2019.
- [9] Ying-Yu Chen, Amit Sangai, Morteza Gholipour, and Deming Chen "Graphene Nano-Ribbon Field-Effect Transistors as Future Low-Power Devices," *Symposium on Low Power Electronics and Design*, 2013.
- [10] Mayank Mishra, Ronil Stieven Singh, and Ale Imran, "Performance optimization of GNRFET Inverter at 32nm technology node," *Materials Today: Proceedings*, vol. 4, no. 9, pp. 10607-10611, 2017.

#### **BIOGRAPHIES OF AUTHORS**



Nandhaiahgari Dinesh Kumar received Bachelor of Technology in Electronics & communication Engineering from Nalla Malla Reddy Engineering College, Hyderabad, Telangana, India, in 2017. He is currently pursuing M.Tech in VLSI System Design from VNR Vignana Jyothi Institute of Engineering and Technology (VNR VJIET), Hyderabad, Telangana, India. His research of interest is in low power VLSI. His current research does in the low power VLSI filed in order to design and analyse the digital circuit in terms of static and dynamic power dissipations and delays.



**Dr. Rajendra Prasad Somineni**, Professor, Department of Electronics and Communications, Vallurupalli Nageswara Rao Vignana Jyothi Institute of Engineering &Technology, Hyderabad, India (VNR VJIET), Hyderabad. Published 25 Research Papers in International/National Journals/Conferences. His areas of interest are Low Power VLSI, Nano Technology; New Technology based VLSI circuit's design, Embedded Systems and Microcontrollers.



CHILUKURI.RAJAKUMARI received the B.E degree from Electronics And Communication Engineering, from ANNA University- Chennai, in 2005. Further she has been awarded M. Tech degree from the Electronics and communication Engineering Department, from Dr.M.G.R.Educational & Research institute- Chennai, in 2007. She is currently an assistant professor in Vallurupalli Nageswara Rao Vignana Jyothi Institute of Engineering & Technology, Hyderabad, India. Along with that she is pursuing PhD in the Electronics and Communication Engineering Department, Koneru Lakshmaiah University, Andhra Pradesh, India. Her research interest includes Estimation of different parameters of Low Probability of Intercept Radar in the area of VLSI Signal Processing.