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Surface potential modeling of dual metal gate-graded channel-dual oxide thickness with two dielectric constant different of surrounding gate MOSFET

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ABSTRACT

An Analytical study for the surface potential, threshold voltage and Subthreshold swing (SS) of Dual-metal Gate Graded channel and Dual Oxide Thickness with two dielectric constant different cylindrical gate surrounding-gate (DMG-GC-DOTTDCD) metal–oxide–semiconductor field-effect transistors (MOSFETs) is proposed to investigate short-channel effects (SCEs). The performance of the modified structure was studied by developing physics-based analytical models for the surface potential, threshold voltage shift, and Subthreshold swing. It is shown that the novel MOSFET could significantly reduce threshold voltage shift and Subthreshold swing, can also provides improved electron transport and reduced short channel effects (SCE). Results reveal that the DMG-GC-DOTTDCD devices with different dielectric constant offer superior characteristics as compared to DMG-GC-DOT devices. The derived analytical models agree well with simulation by ATLAS.

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1. INTRODUCTION

The decrease of the dimensions in transistors MOSFETS is not the fruit of the hazard and follows a law of reduction of generalized scale [1]. This law is in fact a version improved by the first law drafted by Dennard In 1974. The principle of these laws is to quantify the major parameters of a technology (dimensions, doping, capacity, current...) using a single factor K in order to easily predict the expected performance for the future nodes technological [2].

This reduction in size leads in the other hand to the proliferation of parasitic effects. Let us quote for example the effects of short channel (decrease of the threshold voltage of the transistor, DIBL ...) [3], the leakage current gate, and the technological fluctuations (inhomogeneities of doping, thickness ...). These effects come to disrupt in a significant way the functioning of the integrated circuit.

So, it becomes important to develop new architectures of component and / or use other materials than those traditionally used in microelectronics (Si, SiO2, silicon polycristrallin ...) while deviating the least possible from the currently maitrized manufacturing processes. Several types of devices are at present for the study in applied research and in research and at the large founders of integrated circuits. Examples

include the devices with silicon on isolant (SOI), the transistors multigrilles (DG for Double Gate, GAA for All Around, SG Surrounding Gate ...). These new architectures must offer the advantage of better control of potential in the channel by the gate voltage what will make it possible to still push back the limits of the miniaturization of the MOSFETS. The structure Gate-All-Around MOSFET also called "surrounding-gate MOSFET"[4], offers a better control of the electrostatic potential by appearing with DG MOSFET structure [5].

In recent years, to reduce the SCEs and improve hot carrier reliability, various studies have been carried out on SG MOSFET. Many works suggested that gate material engineering as the solution to overcome these effects, Dual-material gate (DMG) structure using two metals with different work functions which improves SCEs than single Material (SM) SG MOSFET [6]. Many authors have reported the channel engineering, graded channel (GC) [7], as one of the possible solution for suppressing the SCEs and enhancing the device performance. The use of GC, with two doping region highly doped region near source end and low doped region near drain end , showed significant improvement of hot carrier reliability and immunity against SCEs. Many works have also reported high-k dielectrics as an alternative to replace SiO2 as the gate dielectric In order to reduce gate leakage current and improve gate controllability over the channel [8, 9].

Therefore in this research work, we have developed the model considering all important device engineering, as Dual-metal Gate Graded channel and Dual Oxide Thickness with different dielectric constant surrounding-gate (DMG-GC-DOT), using parabolic approximation method which is valid for the other structures shown in the Figure1(a)[10]. An intensive comparative study of other device structure is also carried out. Also the analytical model results are verified by comparing them with results obtained from the simulation using ATLAS.

2. MODEL DERIVATION

A cross section along the channel direction of the DMG-GC-DOTTDCD MOSFET is shown in Figure 1(b). A dual material gate device can be perceived as two sub-devices connected in series. M_1 and M_2 with length L_1 and $L-L_1$ are the two metal gates having different work function. The work function of M_1 is higher than M_2 ($\varphi_1 \succ \varphi_2$). The doping concentration N_H in the halo region (L_1) is higher than N_L in the rest of the channel ($L_2 = L - L_1$) and the thickness oxide t_{ox2} (SiO_2) in the rest of the channel in region $L_2 = L - L_1$ is large than t_{ox1} (high-k) in region L_1. Owing to the cylindrical symmetry of the device structure, a cylindrical coordinate system is employed, which consists of a radial direction r and a horizontal direction z (angular component is not shown in the figure). The symmetry of the structure ensures that the potential and the electric field have no variation with the angular in plane of the radial direction. Hence, a 2D analysis is sufficient.

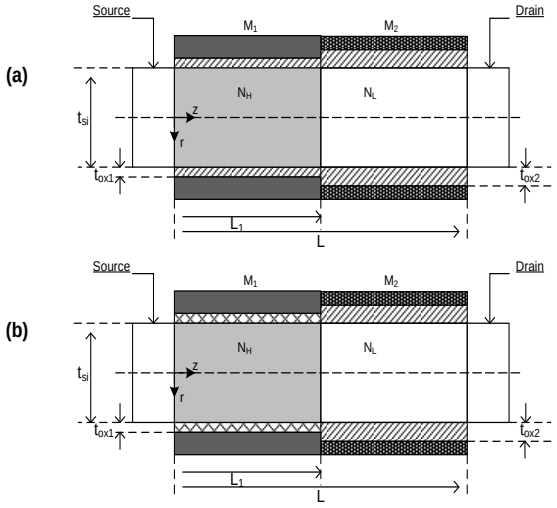

Figure 1. Cross-sectional views of various device design engineering on SG MOSFET;
(a) (DMG–GC–DOT), (b) (DMG–GC–DOTTDCD)

Analytical and numerical models of threshold voltage and subthreshold swing for DMG-GC-DOTTDCD MOSFET are compared to those for DMG-GC-DOT MOSFET.

2.1. Surface potential model

The electrostatic potential and electric field distribution in the silicon channel can be derived by solving Poisson's equation. Neglecting the influence of charge carriers and fixed charges, the Poisson's equation in cylindrical coordinates in two regions (i=1, 2) can be written as:

$$\frac{1}{r}\frac{\partial}{\partial}\left(r\frac{\partial\varphi_i(r,z)}{\partial r}\right)+\frac{\partial^2\varphi_i(r,z)}{\partial z^2}=\frac{qN_i}{\varepsilon_{si}} \quad (1)$$

$$0\le z\le L,\ 0\le r\le\frac{t_{si}}{2}$$

Where t_{si} is the thickness of the silicon channel, ε_{si} is the dielectric constant of silicon pillar, $N_1=N_H$ and $N_2=N_L$.

The potential distribution in the two regions is assumed to be a parabolic profile [11] in the radial direction and can be written as:

$$\varphi_i(r,z)=p_{i0}(z)+p_{i1}(z).r+p_{i2}(z).r^2 \quad (2)$$

Where $p_{i0}(z)$, $p_{i1}(z)$ and $p_{i2}(z)$ are functions of z only.

The electric field in the centre of the silicon pillar is zero by symmetry

$$\left(\frac{\partial\phi_i(r,z)}{\partial r}\right)_{r=0}=0=p_{i1}(z)$$

The electric flux at the oxide-silicon interface is continuous

$$\left(\frac{\partial\phi_i(r,z)}{\partial r}\right)_{r=\frac{t_{si}}{2}}=\frac{c_{ox_i}}{\varepsilon_{si}}\left(V_{GS}+V_{FB_i}+\phi_{si}(z)\right)=p_{i2}(z)t_{si}$$

Where $c_{oxi}=\dfrac{2\varepsilon_{oxi}}{t_{si}\ln\left(1+\dfrac{2t_{oxi}}{t_{si}}\right)}$

c_{oxi} is the oxide capacitance of part oxide (i=1, 2), V_{GS} is the gate to source voltage. $\varphi_i(r,z)$ is the surface potential, ε_{ox1} and ε_{ox2} are the dielectric constant of high-k and SiO_2 gate oxide respectively, and t_{ox1} is the oxide layer of region L_1 and t_{ox2} is oxide layer of region $L-L_1$.

V_{FBi} is the flat band voltages of the two regions will be different and they are given as follows:

$$V_{FB_1}=\varphi_1-\varphi_{siH},\ V_{FB_2}=\varphi_2-\varphi_{siL}$$

Where φ_1 and φ_2 are the work functions of M_1 and M_2, respectively, and φ_{siH} and φ_{siL} are the work functions of the region L_1 and the rest of silicon pillar, respectively.

The Poisson equation in the two regions is solved using the boundary conditions, and is reduced to the following form:

$$\frac{\partial^2 \varphi_{si}(z)}{\partial z^2} - \lambda_i^{\,2} \varphi_{si}(z) = D_i \quad \text{i=1, 2} \tag{3}$$

Where $\lambda_i = \sqrt{4c_{oxi}/\varepsilon_{si}t_{si}}$, is characteristic length and $D_i = \frac{qN_i}{\varepsilon_{si}} - \lambda_i^{\,2}(V_{GS} - V_{FBi})$

The potential at the source end is $\varphi_1(0,0) = V_{bi1}$, where V_{bi1} is the built in potential

The potential at the drain end is $\varphi_2(0,L) = V_{bi2} + V_{DS}$, Where L is the device channel length and V_{DS} is drain to source voltage.

The general solution for the surface potential has the form:

$$\varphi_{si}(z) = A_i \exp(-\lambda_i z) + B_i \exp(\lambda_i z) - \frac{D_i}{\lambda_i^{\,2}} \tag{4}$$

Using boundary conditions, the coefficients A_i and B_i (i = 1, 2) can be determined as:

$$A_1 = V_{bi_1} + \frac{D_1}{\lambda_1^{\,2}} - B_1$$

$$A_2 = \left(\left(V_{bi_2} + V_{ds} + \frac{D_2}{\lambda_2^{\,2}}\right) - B_2 \exp(\lambda_2 L)\right)\exp(\lambda_2 L)$$

$$B_2 = \frac{U_2}{U_0},\ B_1 = \frac{U_1}{U_0},\ U_2 = a_0 C_2 - c_0 C_1$$

$$U_1 = d_0 C_1 - b_0 C_2,\ U_0 = a_0 d_0 - b_0 c_0,$$

$$C_1 = \left(V_{bi_2} + V_{ds} + \frac{D_2}{\lambda_2^{\,2}}\right)\exp(-\lambda_2 L_1) - \left(V_{bi_1} + \frac{D_1}{\lambda_1^{\,2}}\right)\exp(-\lambda_2 L)\exp(-\lambda_1 L_1) + \left(\frac{D_1}{\lambda_1^{\,2}} - \frac{D_2}{\lambda_2^{\,2}}\right)\exp(-\lambda_2 L)$$

$$C_2 = -\lambda_2\left(V_{bi_2} + V_{ds} + \frac{D_2}{\lambda_2^{\,2}}\right)\exp(-\lambda_2 L_1) + \lambda_1\left(V_{bi_1} + \frac{D_1}{\lambda_1^{\,2}}\right)\exp(-\lambda_2 L)\exp(-\lambda_1 L_1)$$

By differentiating the surface potential $\varphi_{si}(r = R, z)$ with respect to z, the electric field E (z) at the channel surface in the z direction is given as:

$$E_i(z) = -A_i\lambda_i \exp(-\lambda_i z) + B_i\lambda_i \exp(\lambda_i z) \tag{5}$$

$0 \le z \le L$, i=1, 2

2.2. Threshold voltage model

In a DMG-GC-DOTTDCD MOSFET structure, the position of the minimum surface potential is always located under the gate material having higher work function (M_1). Therefore, the position of

the minimum surface potential can be found by equating the derivative of the surface potential under M_1 to zero. By equating $\frac{d\varphi_{s1}}{dz} = 0$, we obtain:

$$z_{\min} = \frac{1}{2\lambda}\sqrt{\frac{B_1}{A_1}}$$

The threshold voltage V_{TH} is defined as the value of V_{GS} at which the minimum surface potential is

$$\varphi_{si,\min} = \varphi_{si}\left(z_{\min}\right) = 2\varphi_B ,$$

Where φ_B is the bulk Fermi potential.

We considered the minimum surface potential in the region L_1, where the doping concentration N_H is high (region (1)).

$\varphi_{si,\min}$ can be deduced from (4):

$$\varphi_{si,\min} = 2\sqrt{A_1 B_1} - \frac{D_1}{\lambda_1^{\,2}} \tag{6}$$

The threshold voltage can be expressed as:

$$V_{TH} = \left(-\eta + \sqrt{\eta^2 - 4\sigma\xi}\right)\Big/ 2\sigma$$

Where:

$$a_0 = 2\exp\left(-\lambda_2 L\right)\sinh\left(\lambda_1 L_1\right)$$

$$b_0 = 2\sinh\left(\lambda_2\left(L - L_1\right)\right)\ c_0 = 2\lambda_1\exp\left(-\lambda_2 L\right)\cosh\left(\lambda_1 L_1\right)\ d_0 = -2\lambda_2\cosh\left(\lambda_2\left(L - L_1\right)\right),$$

$$U_0 = a_0 d_0 - b_0 c_0\ \ e_0 = \exp\left(-\lambda_1 L_1\right),\ e_1 = \exp\left(-\lambda_2 L_1\right),\ e_2 = \exp\left(-\lambda_2 L\right),\ a_1 = \frac{\left(qN_{aH}\right)}{\varepsilon_{si}\lambda_1^{\,2}} + V_{FB_1},$$

$$a_2 = \frac{\left(qN_{aL}\right)}{\varepsilon_{si}\lambda_2^{\,2}} + V_{FB_2},\ b_1 = e_2 e_0\left(V_{bi_1} + a_1\right),\ b_2 = e_1\left(V_{ds} + V_{bi_2} + a_2\right),\ c_1 = \lambda_1 b_1, c_2 = \lambda_2 b_2$$

$$E = \left(d\left(e_2 e_0 - e_1\right) + b\left(\lambda_1 e_2 e_0 - \lambda_2 e_1\right)\right)\Big/ U_0$$

$$\sigma = -\left(4E^2 + 4E + 1\right),\ \eta = 4\left(V_{bi_1} + a_1\right) + E4D - 8DE + 2a_1 + 4\phi_B$$

$$\xi = 4\left(V_{bi_1} + a_1\right)D - 4D^2 - a_1^{\,2} - 4a_1\varphi_B - 4\varphi_B^{\,2}$$

2.3. Subthreshold swing

We considered the minimum surface potential in the region L_1, where the doping concentration N_H is high (region (1)).

A subthreshold swing (SS) is an important parameter and defined as:

$$SS = \frac{KT}{q}\ln(10)\left(\frac{\partial\phi_{si,\min}}{\partial V_{GS}}\right)^{-1} \tag{7}$$

From (6), we obtain:

$$\left(\frac{\partial \varphi_{si,\min}}{\partial V_{GS}}\right) = 1 + \left(A_1 B_1\right)^{\left(\frac{-1}{2}\right)} \left(A_1 P_1 + B_1 P_2\right)$$

Where

$$P_1 = \frac{d_0}{U_0}\left(\exp\left(-\left(\lambda_2 L + \lambda_1 L_1\right)\right) - \exp\left(\lambda_2 L_1\right)\right)$$

$$-\frac{b_0}{U_0}\lambda_2\left(\exp\left(-\lambda_2 L_1\right) - \exp\left(-\left(\lambda_2 L + \lambda_1 L_1\right)\right)\right)$$

$$P_2 = -1 - P_1$$

3. RESULTS AND DISCUSSION

In this section, it is explained the results of research and at the same time is given the comprehensive discussion. Results can be presented in figures, graphs, tables and others that make the reader understand easily [2], [5]. The discussion can be made in several sub-chapters.

Now the performance of DMG-GC-DOTTDCD in threshold voltage shift, SS and DIBL will be examined. The performance of DMG-GC-DOTTDCD with different dielectric oxide constant, which Silicon dioxide (SiO_2) is taken as low-k gate oxide material and hafnium dioxide (HfO_2) is taken as high-k gate oxide material with permittivity $3.9\varepsilon_0$ and $10\varepsilon_0$, respectively, here ε_0 is the permittivity of the free space, is also compared with the DMG-GC-DOT with two different dual layer oxide of SiO_2. The analytical models are verified by comparing analytical results with the simulation obtained by using ATLAS. Unless otherwise stated, the channel doping concentrations in two regions are $N_H = 3.10^{17}(cm)^{-3}$, $N_L = 4.10^{16}(cm)^{-3}$, $t_{ox1} = 2nm$, $t_{ox2} = 4nm$, $L = 100nm$, $L_1 = 25nm$, $t_{si} = 20nm$, $V_{GS} = 0.1V$, $V_{DS} = 0.5V$. The work functions of M_1 and M_2 are 4.8V and 4.4V, respectively.

Figure 2 shows the evolution of the surface potential for DMG-GC-DOT and DMG-GC-DOTTDCD along the channel. It can seen That the incorporation of two oxide thickness with different dielectric constant in (DMG–GC-DOTTDCD) SG MOSFET introduces an increase in the potential barrier, it also evident according to the figure that the minimal surface potential occurs in the first region near the source of DMG-GC-DOTTDCD.

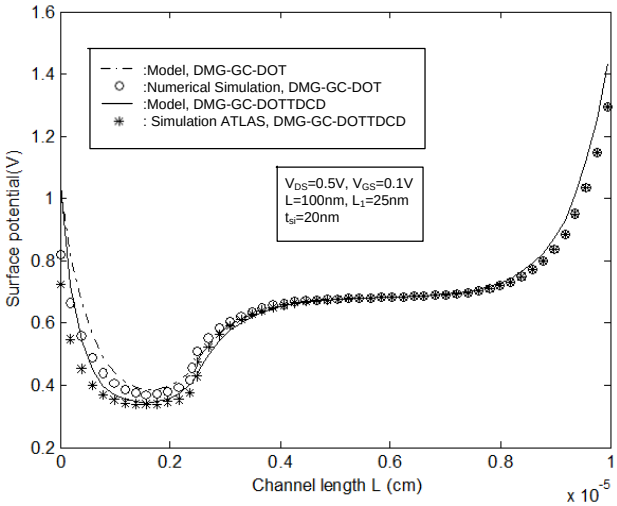

Figure 2. Surface potential along the channel for DMG-GC-DOT, and DMG-GC-DOTTDCD

Figure 3 reveals a change of step in the potential. The profile involves a change of step in the electric Field located at the junction of two metals. The increase in the lateral Electric Field in the channel located under the interface of two gate materials causes an increase in the carrier transport efficiency.

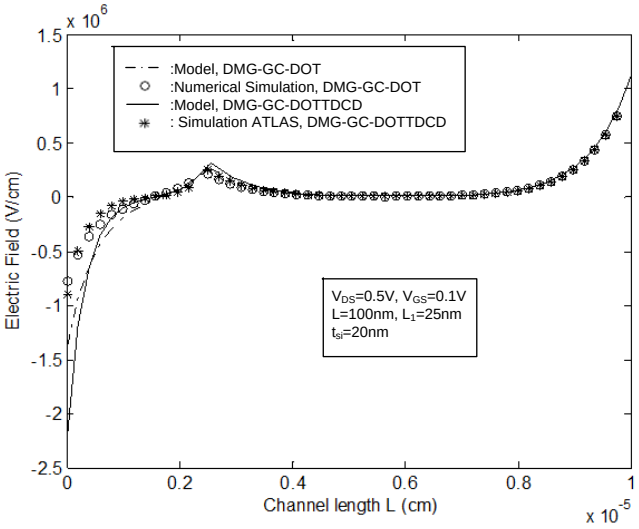

Figure 3. Variation of the electric field versus channel length for DMG-GC-DOT and DMG-GC-DOTTDCD with V_{GS}=0.1V and V_{DS}=0.5V

In Figure 4, we plot the threshold voltage shift (ΔV_{TH}) variation versus channel length for DMG-GC-DOT and DMG-GC-DOTTDCD MOSFETs. In Figure 4, it is evident that DMG-GC-DOTTDCD MOSFET provides higher efficacy to (ΔV_{TH}) as compared to DMG-GC-DOT MOSFETs.

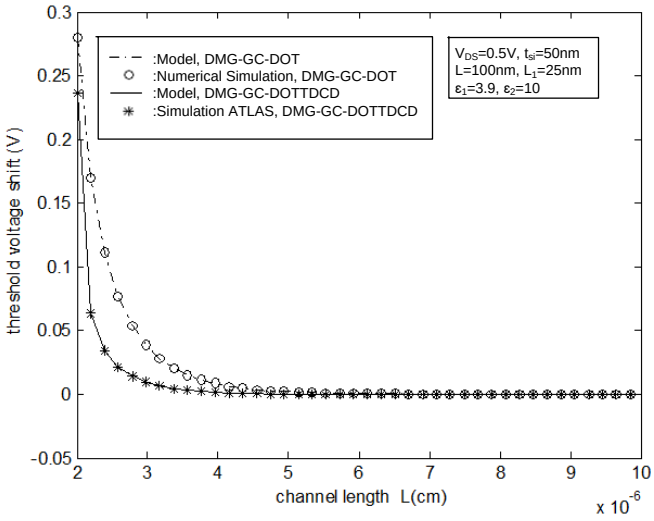

Figure 4. Threshold voltage shift versus channel length for DMG-GC-DOT and DMG-GC-DOTTDCD MOSFET

Figure 5 shows the variation of the subthreshold swing along the channel for DMG-GC-DOT and DMG-GC-DOTTDCD. It is clear that the subthreshold reduced for device DMG-GC-DOTTDCD than DMG-GC-DOT.

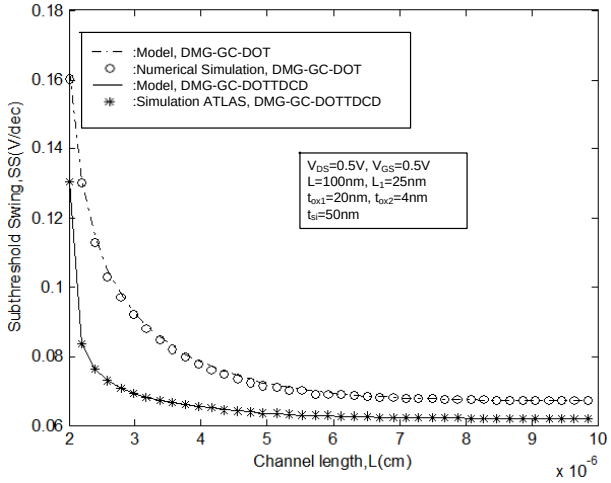

Figure 5. Subthreshold swing (SS) versus channel length (L) for DMG-GC-DOT and DMG-GC-DOTTDCD

Figure 6 shows the DIBL variations of DMG-GC-DOT MOSFET and DMG-GC-DOTTDCD MOSFET versus the channel length. DIBL can be expressed by $\Delta V_{th}/\Delta V_{ds}$. Where $\Delta V_{th} = V_{th}\big|_{(V_{ds}=0)} - V_{th}\big|_{(V_{ds}=2)}$ and $\Delta V_{DS} = 2V$. It is evident from the figure that because of the joint effects of the dual oxide thickness with different dielectric constant, DMG-GC-DOTTDCD exhibits better suppression of DIBL than DMG-GC-DOT.

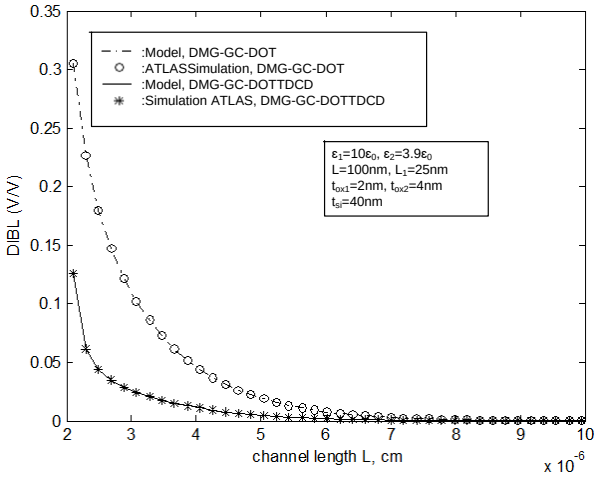

Figure 6. DIBL variations versus the channel length for DMG-GC-DOT MOSFET and DMG-GC-DOTTDCD MOSFET

4. CONCLUSION

By solving 2D Poisson's equation in the two channel regions, an analytical model comprising surface potential, threshold voltage shift and DIBL for a DMG-GC-DOTTDCD MOSFET has been developed in order to improve short channel effects and hot carrier effects. Using this analytical model, the characteristics of DMG-GC-DOTTDCD are investigated in terms of surface potential, threshold voltage shift, and DIBL. It has been demonstrated that DMG-GC-DOTTDCD MOSFET provides a better immunity to SCEs as compared to DMG-GC-DOT MOSFET. It is evident from the results that the properoptimization of dual oxide thickness with different dielectric constant in DMG–GC–DOTTDCD MOSFET significantly reduces DIBL effect and subthreshold swing. The results obtained from the models agree well with the results obtained using simulation ATLAS.

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