❏   34

A compact model of transconductance and drain conductance for DMG-GC-DOT cylindrical gate MOSFET

Hind Jaafar[1], Abdellah Aouaj[2], Ahmed Bouziane[3], and Benjamin Iñiguez[4]
[1,2,3]Faculty of Science and Technology, University Sultan Moulay Slimane, Morocco
[4]Department of Electronic, Electrical and Automatic Control Engineering, Universitat Rovira i Virgili, Spain
Email: h.jaafar@usms.ma[1]

Article Info	ABSTRACT
	A compact model for dual-material gate graded-channel and dual-oxide thickness with two dielectric constant different cylindrical gate (DMG-GC-DOTTDCD) MOSFET was investigated in terms of transconductance, drain conductance and capacitance. Short channel effects are modeled with simple expressions, and incorporated into the core of the model (at the drain current). The design effectiveness of DMG-GC-DOTTDCD was monitored in comparing with the DMG-GC-DOT transistor, the effect of variations of technology parameters, was presented in terms of gate polarization and drain polarization. The results indicate that the DMG-GC-DOTTDCD devices have characteristics higher than the DMG-GC-DOT MOSFET. To validate the proposed model, we used the results obtained from the simulation of the device with the SILVACO-ATLAS-TCAD software.

Corresponding Author:

Hind Jaafar,
Faculty of Science and Technology,
University Sultan Moulay Slimane,
Beni Mellal, Morocco.
Email: h.jaafar@usms.ma

1. INTRODUCTION

Since the invention of the first transistor in 1947, then that of the integrated circuit in 1958, by Jack Kilby, the progress of microelectronics has been considerable, both at the improvement of the performance and the increase of the complexity of the circuits lower production costs. MOS (Metal Oxide Semiconductor) transistors on silicon used in CMOS architecture (Complementary MOS) are the main artisans of this continual progression and overwhelmingly dominate the semiconductor market.

However, after almost twenty years of unrestrained racing of the dimensions of the electronic components, the problems are no longer limited only to the difficulties of implementation. We now see phenomena of a theoretical nature calling into question the advantages offered by CMOS technology. These include the lowering of the drain potential barrier (DIBL), short channel effects (SCE), phenomena of a quantum nature, gate tunnel current, and so on [1]. These phenomena have unfortunately become inevitable when the dimensions of the devices are drastically reduced and make miniaturization difficult or even impossible. To overcome these difficulties, one of the solutions is to modify the architecture of current components, in particular the increase in the number of grids in order to have better control of the current flow, appears to be a solution of choice for the future of the microelectronics [2]. It seems clear that transistors integrating a second grid such as the double-gate transistor and the FinFET are becoming essential solutions for the design of micro and nanoelectronic circuits [3].

At this scale, one of the current locks for industrialists and especially integrated circuits (IC) designers is to improve existing compact models and establish new compact, reliable and simple models for modern components such as multi-gate MOS transistors, also known as Multi-Gates (MG) FETs. Thanks to their structures, these devices offer not only a higher current but also a better control of the channel when their dimensions are greatly reduced compared to the bulk MOSFET [4]. The Cylindrical Surrounding Gate MOSFET (SRG MOSFET) is an excellent candidate to continue the miniaturization of the MOS devices as well as to increase the density of integration in the CMOS circuits. Indeed, this architecture exhibits high performance for small dimensions and small radi of silicon (less than or equal to 5 nm), such as excellent electrostatic control, a slope below the ideal threshold, a low DIBL, etc [5-8].

The incorporation of dual material gate in DMG-GC-DOT MOSFET overcomes the device degradation due to a high electric field at the drain end. High metal work function on the source side (4.8 eV) and low work function on the drain side (4.4 eV) enhance the performance of the device and improves the carrier transport efficiency. Although DMG-GC-DOT MOSFET with dual gate material shows superior immunity against the SCEs, but still SCEs are not negligible for such device. Due to decreasing gate oxide thickness, the gate leakage problem increases. To reduce gate leakage current, high-k gate dielectric is mostly used as an alternative to replace SiO_2 as the gate dielectric. In the double gate oxide architecture, material with high dielectric constant is presented in the oxide thin layer on the source side to increase the effective thickness and decrease the physical thickness of the oxide layer thereby reducing gate leakage current. In Graded channel, high doping profile at the source side and low doping profile at the drain side, enhance the concentration of electron on the source side and increases the mobility of carrier on the drain side. From the Poisson equation and the gradual channel approximation (GCA), the surface potential, threshold voltage and subthreshold voltage are calculated in a simple manner.

In this work, the analysis of drain current is extended to obtain the expressions for transconductance g_m and drain conductance g_{ds} [9]. The effectiveness of DMG-GC-DOTTDCD MOSFET has been compared with the characteristics of DMG-GC-DOT MOSFET. The accuracy of the model has been verified by comparing the analytical results with simulated data obtained using ATLAS simulator.

2. MODEL DERIVATION

In this work, we have developed the model considering all important device engineering, as Dual-metal Gate (DMG) [10, 11] Graded channel (GC) and Dual Oxide Thickness [12] with two different dielectric constant (DOTTDCD) surrounding-gate (DMG-GC-DOTTDCD), using parabolic approximation method which is valid for the other structures shown in the Figure 1-(b) [13], which gate has two metal (M_1 and M_2) with length L_1 and $L - L_1$ are the two metal gates having different work function. The work function of M_1 is higher than M_2 $(\varphi_1 \succ \varphi_2)$. The doping concentration N_H in the halo region (L_1) is higher than N_L in the rest of the channel $(L_2 = L - L_1)$ and the thickness oxide t_{ox2} (SiO_2) in the rest of the channel in the region $L_2 = L - L_1$ is large than t_{ox1} (high-k) in the region L_1.
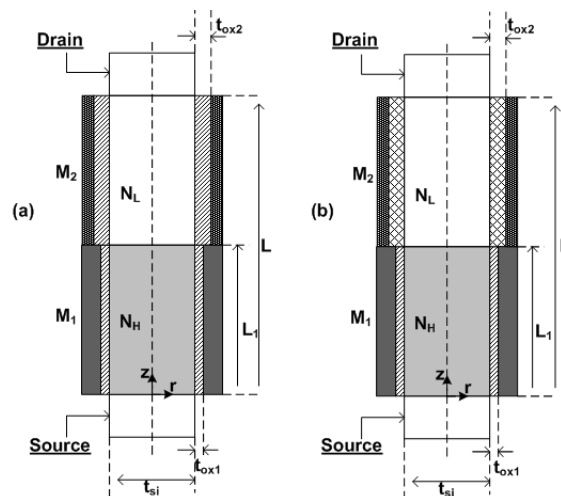

Figure 1. Cross-sectional views of device design engineering; (a) DMG–GC–DOT,
(b) DMG-GC-DOTTDCD with different permittivity of oxide

2.1. Current model

The drain current is predominantly given by the drift mechanism and can be expressed as:

$$I_{ds}(z) = \pi t_{si} Q_{ni}(z) \frac{\mu_{ni}(dV(z)/dz)}{1+(1/E_{sat})(dV(z)/dz)} \tag{1}$$

Where V(z) is the channel potential along the z direction, t_{si} is the radius of the device, $dV(z)/dz$ is the electric field along the z direction, $E_{sat} = 2\upsilon_{sat}/\mu_{ni}$ is the critical field, υ_{sat} is the saturation velocity, μ_{ni} is the mobility in the higher and lower metal work function region according to i equal to 1 and 2, respectively, and is given as

$$\mu_{ni} = \frac{\mu_1}{1+\theta_i(V_{gs}-V_{thi})} \tag{2}$$

Where θ_i is a fitting parameter and the μ_1 expresses an impurity density dependence of mobility and is empirically given by

$$\mu_1 = \frac{\mu_{n0}}{\sqrt{\left(1+\left[N_i/(N_{ref}+(N_i/S))\right]\right)}} \tag{3}$$

Where μ_{n0} is the electron mobility. The parameters S and N_{ref} involve trade-offs between phonon and impurity scattering, respectively, and given as S=450, $N_{ref} = 3\times10^{22} m^{-3}$. $Q_{ni}(z)$ is the surface charge density at a point z in the strong inversion region and is given by

$$Q_{ni}(z) = c_{ox_i}(V_{gs}-V_{thi}-V(z)) \tag{4}$$

Where V_{gs} is the gate to source bias, V_{thi} is the threshold voltage [14] for the two regions according to i equal to 1 and 2, respectively, and c_{ox_i} is the gate oxide capacitance for two regions of the DMG-GC-DOT MOSFET.

Substituting (2) – (4) in (1) and upon subsequent integration, results in the following expression for the drain current in the linear region:

$$I_{ds} = \frac{\pi t_{si}\mu_{eff}c_{ox_1}\left[V_{gs}-V_{th}-\left(V_{ds}/2\right)\right]V_{ds}}{L\left(1+\left(V_{ds}/LE_{eff}\right)\right)} \tag{5}$$

Where

$$\mu_{eff} = \frac{L}{\left[(L_1/\mu_{n1})+(L_2/\mu_{n2})\right]}$$

$$E_{eff} = \frac{2\upsilon_{sat}}{\mu_{eff}}$$

2.2. Transconductance formulation

The transconductance is a crucial parameter in circuit design analog, must be as high as possible. The transconductance increases very rapidly when the channel length becomes less than 100 nm, is calculated by deriving the drain current with respect to V_{gs} $(V_{ds} = constant)$ and therefore makes it possible to verify the differential of the model, and is expressed as:

$$g_m = \left(\frac{dI_{ds}}{dV_{gs}} \right)\Bigg|_{V_{ds}=const} \tag{6}$$

Using the equations of drain current (5) and (6) the expression for g_m in the linear region, is derived as given below.

$$g_m = \pi t_{si} c_{oxi} V_{ds} \left[\frac{Ab - aB}{\left(L \left(1 + \left(\frac{V_{ds}}{LE_{eff}} \right) \right) \right)^2} \right] \tag{7}$$

Where

$$a = \mu_{eff} \left(V_{gs} - V_{th} - \frac{V_{ds}}{2} \right)$$

$$b = L \left(1 + \left(\frac{V_{ds}}{LE_{eff}} \right) \right)$$

$$E = \frac{-L\theta_i \mu_1^{\,3} \left(L_1 + L_2 \right)}{\left[\left(L_1 + L_2 \right) \left(\mu_1 + \theta_i \mu_1 V_{gs} \right) - \theta_i \mu_1 \left(L_1 V_{th1} + L_2 V_{th2} \right) \right]^2}$$

$$A = E \left(V_{gs} - V_{th} - \frac{V_{ds}}{2} \right) + \mu_{eff} \ ,$$

$$B = \frac{V_{ds}}{2\upsilon_{sat}} E$$

2.3. Drain conductance formulation

The conductance is a significant parameter of the apparatus for analogical simulation of the circuit and is defined like:

$$g_{ds} = \left(\frac{dI_{ds}}{dV_{ds}} \right)\Bigg|_{V_{gs}=const} \tag{8}$$

Using the equation of drain current (5), the expression for g_{ds} is derived to be,

$$g_{ds} = \frac{Cd - Dc}{\left(L \left(1 + \frac{V_{ds}}{LE_{eff}} \right) \right)^2} \tag{9}$$

Where

$$C = \pi t_{si} \mu_{eff} c_{oxi} \left(V_{gs} - V_{th} - V_{ds} \right)$$

$$D = \frac{1}{E_{eff}}$$

$$c = \pi t_{si} \mu_{eff} c_{oxi} V_{ds} \left(V_{gs} - V_{th} - \frac{V_{ds}}{2} \right)$$

$$d = L \left(1 + \frac{V_{ds}}{LE_{eff}} \right)$$

3.   RESULTS AND DISCUSSION

Using the developed analytical models, the transconductance and drain conductance of DMG-GC-DOTTDCD MOSFET is examined in terms of variation of gate source and drain source. The gate to source capacitance, C_{gs} and gate to drain capacitance, C_{gd} are calculated with respect to gate to source voltage by Atlas-3D simulator.

The simulated results of DMG-GC-DOT MOSFET are compared to other devices such as DMG-MOSFET, and DMG-DOT MOSFET. So high-k gate dielectric is used, in the DMG-GC-DOTTDCD, in the thin oxide layer on side the source to replace SiO_2 to increase the effective thickness thereby reducing gate leakage current, this structure is compared with the DMG-GC-DOT. To verify these analytical models, the 2-D device simulator TCAD is used to simulate the device characteristics.

Figure 2 shows the comparison between transconductance as a function of gate-source voltage characteristics as computed using the model DMG-GC-DOT and DMG-GC-DOTTDCD with ε_1 and ε_2. The results are compared with the simulated results. The two are observed to be in close agreement.

The variation of drain conductance has been plotted against drain-source voltage for DMG-GC-DOT and ε_1 and ε_2 in DMG-GC-DOTTDCD structures in Figure 3. It can be analyzed that the drain conductance in DMG-GC-DOTTDCD higher than DMG-GC-DOT structure.

Figure 4 shows a reasonable variation of the transconductance g_m as a function of the gate-source voltage V_{gs} for a low and a high value of the drain voltage $V_{ds} = 0.05\,V$ and 1V. It compared with the numerical simulation, good agreement is found for low and for high drain voltage.

Figure 5 also illustrates the drain conductance g_{ds} in function of the drain voltage V_{ds} for different values of $V_{gs} = 0.5\,V$, 1V and 1.5V. A good agreement between analytical and simulated results validates the model.

Figure 6 shows the capacitance C_{sg} and C_{dg} as functions of the gate voltage, for different values of the drain-source voltage. The modeled capacitance characteristics show a smooth transition between the different operating regimes.
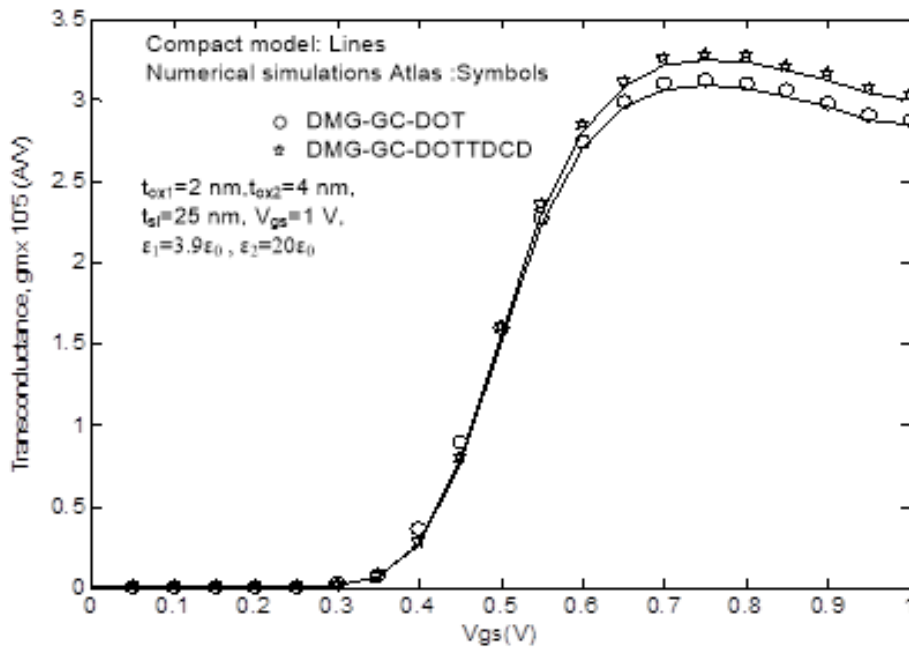

Figure 2. Comparison between DMG-GC-DOT and ε_1 and ε_2
in DMG-GC-DOTTDCD structure for transconductance
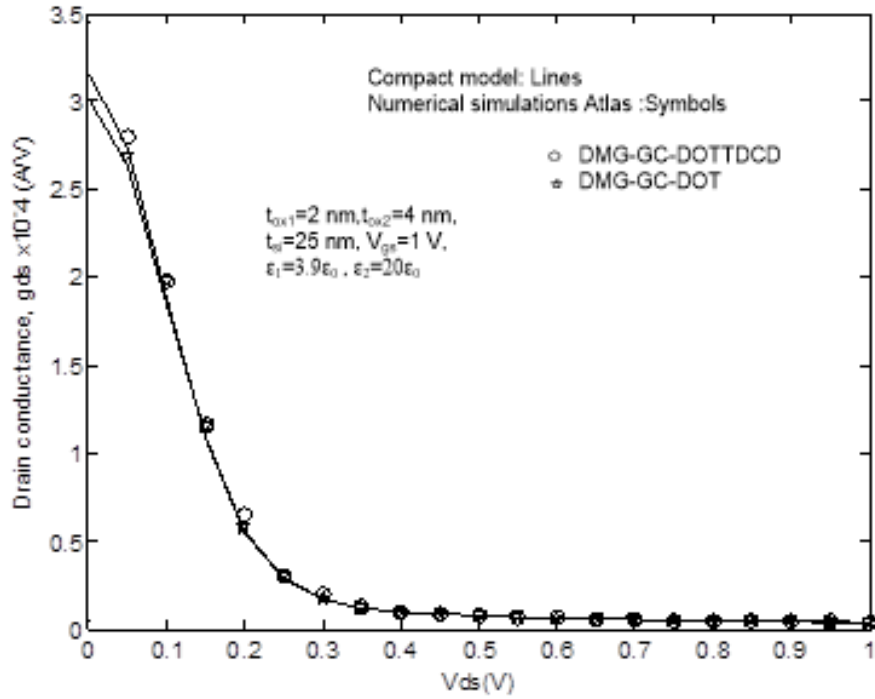
Figure 3. Comparison between DMG-GC-DOT and ε_1 and ε_2
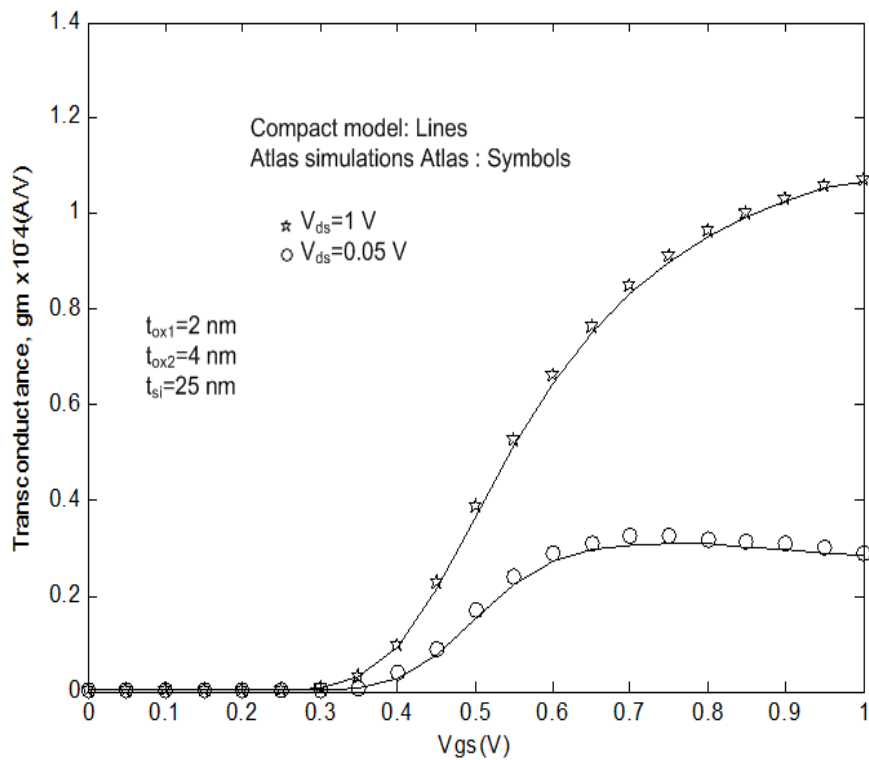in DMG-GC-DOTTDCD structure for drain conductance

Figure 4. Transconductance vs gate-source voltage for different value of V_{ds}
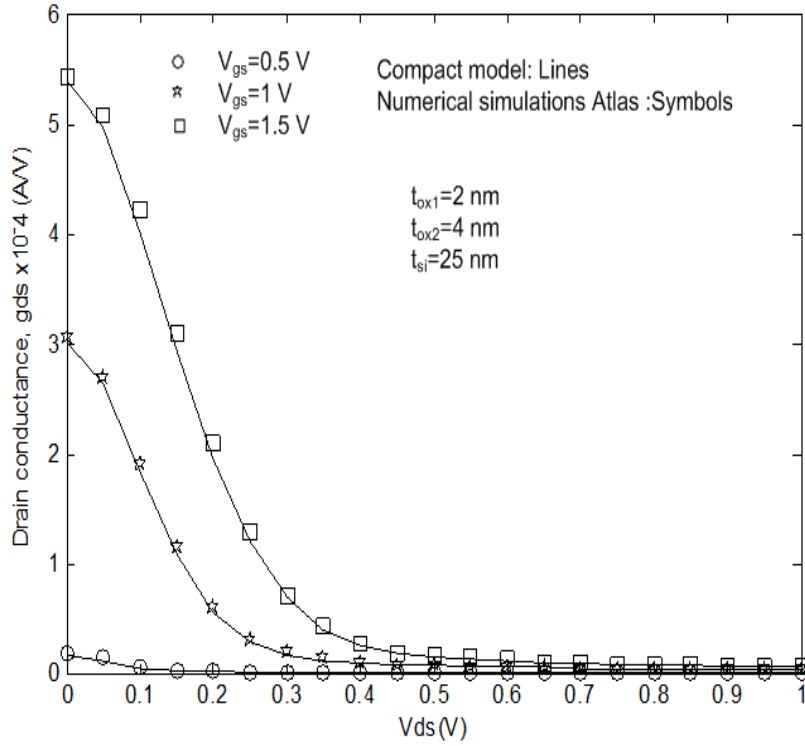in DMG-GC-DOTTDCD MOSFET structure

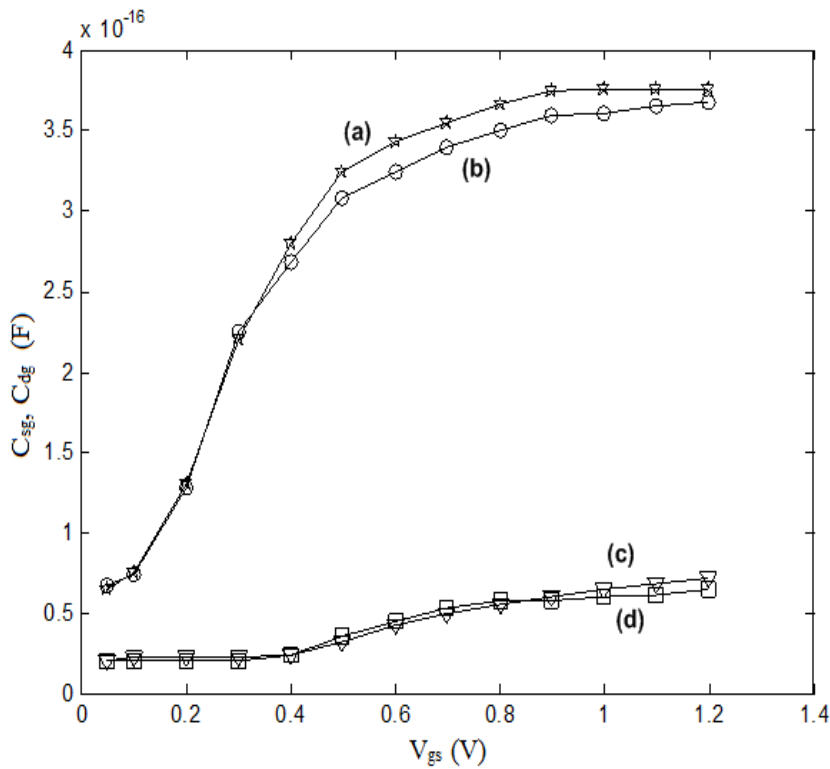Figure 5. Drain conductance vs drain-source voltage for different V_{gs} in DMG-GC-DOTTDCD structure

Figure 6. Drain to gate capacitance (c,d) and source to gate capacitance (a,b) with respect to the gate voltage, for $V_{ds} = 0.1V$ (a,c) and $V_{ds} = 1V$ (b,d)

4.   CONCLUSION

In this paper, the characteristics of DMG-GC-DOTTDCD are presented in terms of transconductance, drain conductance and capacitance. It has been demonstrated that DMG-GC-DOTTDCD MOSFET provides a better immunity to SCEs as compared to DMG-GC-DOT MOSFET. It is analysed from the figures that the decreases of V_{ds} causes the increase of conductance, also the results show that the DMG-GC-DOTTDCD MOSFET structure provides greater transconductance than the DMG-GC-DOT MOSFET structure when increasing V_{gs}. It can be concluded that a very slight difference is observed between the two structures DMG-GC-DOTTDCD MOSFET and DMG-GC-DOT MOSFET for small voltages of V_{ds}. Furthermore in DMG-GC-DOTTDCD structure the use of dielectric constant of SiO2 $\left(\varepsilon_1\right)$ in t_{ox1} and dielectric constant of high K $\left(\varepsilon_2\right)$ in t_{ox2} leads to improved device performance. The results obtained from the models agree well with obtained using device simulator.

REFERENCES

[1]   N. Arora, *MOSFET models for VLSI circuit simulation: theory and practice*, Springer-VerlagTelos, 1993.
[2]   J. Colinge, *Silicon-on-insulator technology: Materials to VLSI*, Kluwer Academic Publishers, 3rd edition, 1997.
[3]   Semiconductor Industry Association (SIA), "ITRS (International Technology Roadmap for Semiconductors)," 2003 ed, Austin, TX. Int. SEMATECH, 2003. [Online]. Available: http://public.itrs.net.
[4]   B. Smaani, "Establishment of compact models of multi-nanoscale MOS transistors for application in circuit design (in French)," Doctoral thesis, University FreresMentouri, Constantine, 2015.
[5]   N. Singh, A. Agarwal, L. K. Bera *et al*, "High-Performance Fully Depleted Silicon Nanowire (Diameter ≤ 5 nm) Gate-All-Around CMOS Devices," *IEEE Electron Device Letters*, vol. 27, pp. 83-86, 2006.
[6]   H. A El Hamid., B. Iñíguez and J. R.Guitart, "Analytical Model of the Threshold Voltage and Subthreshold Swing of Undoped Cylindrical Gate-All Around Based MOSFETs," *IEEE Transact. onElectr. Devic.*, vol. 54, pp. 72-79, 2007.
[7]   B. Ray, and S. Mahapatra, "Modeling and Analysis of Body Potential of Cylindrical Gate-All-Around Nanowire Transistor," *IEEE Transact. On Electr. Devic.*, vol. 55, pp. 09-16, 2008.
[8]   H. Børli, S. Kolberg, T-A. Fjeldly *et al*, "Precise Modeling Framework for Short- Channel Double-Gate and Gate-All-Around MOSFETs," *IEEE Transact. On Electr. Devic.,* vol. 55, pp. 78-86, 2008.
[9]   H. Jaafar, A. Aouaj, A. Bouziane , Benjamin Iñiguez, "Analytical study of drain current and transconductance for a new cylindrical gate MOSFET structure 2018," *4th International Conference on Optimization and Applications (ICOA)*, Jun. 2018.
[10]   Cong, Li., Yi-Qi, Z., Li, Z., and Gang, J., "Quasi-two-dimensional threshold voltage model for junctionless cylindrical surrounding gate metal-oxide-semiconductor field-effect transistor with dual-material gate," *Chinese Physic B*, vol. 23, 2014.
[11]   Wu, M., Jin, X., I., H., Kwon, Chuai, R., Liu, X., and Lee, J.H., "The optimal design of junctionless transistors with double-gate structure for reducing the effect of band-to-band tunneling," *Journal of semiconductors technology and science*, vol. 13, pp. 245-251, 2013.
[12]   H. Jaafar, A. Aouaj, A. Bouziane, "Analytical and Numerical Modeling of Vth and S for new CG MOSFET Structure," *International Journal of Information Science and Techniques*, vol. 6, pp. 1-11, 2016.
[13]   P. S. Dhanaselvam, and N. B. Balamurugan, "Analytical approach of a nanoscale triple-material surrounding gate (TMSG) MOSFETs for reduced short-channel effects," *Microelect. J.*, vol. 44, pp. 400-404, 2013.
[14]   H. Jaafar, A. Aouaj, A. Bouziane, "Analytical Model of The Threshold Voltage Vth, Subthreshold Swing and Drain Induced Barrier Lowering (DIBL) For a new Device Structure of Cylindrical Gate MOSFET," *Journal of Theoretical and Applied Information Technology,* vol. 95, pp. 1355-1362, 2017.