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Performance evaluation of an efficient five input majority gate design in QCA nanotechnology

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Article Info	ABSTRACT
	Quantum-dot-cellular-automata (QCA) is the imminent transistor less technology, considered at nano level with high speed of operation and lower power dissipation features. The present paper proposes a novel and an efficient 5-input coplanar majority gate (PMG) with improved structural and energy efficiency. The proposed gate consumes an occupational area of $0.01\mu m^2$ with 17 QCA cells which is 50% less in comparison to the best designs reported in literature. The proposed structure is also more energy efficient because it dissipates 21.1% less energy than the best reported designs. The correctness of a proposed majority gate is verified by designing a single bit full adder. The new 1-bit full adder design is structural efficient and robust in terms of gate count and clock delay. It consumes occupational area of $0.05\mu m^2$ with 58 QCA cells showing 16.6% improvement in structural efficiency as compared to the best design reported in. It is having a gate count of 4 with the delay of 1 clock cycle. Here, the QCADesigner and QCAPro tools are utilized for the simulation and energy dissipation analysis of proposed majority gate and full adder design.

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1. INTRODUCTION

Designing and fabricating complementary metal oxide semiconductor (CMOS) based logic devices at nano scale [1] has an issues like oxide thickness, thermal reliability and power dissipation [2]. Hence the industries are in search of new techniques which could aid the scaling of CMOS. Researchers are well aware that the CMOS technology could be continued only for a decade. Some of the alternate technologies like QCA, single electron tunneling (SET}, carbon nanotubes (CNT) came into existence. QCA is one of the competitive alternate technology [3] that has none of the above said problems. The benefit of QCA devices over regular CMOS circuits are the absence of electron flow for charge transfer and absence of metallic interconnects which are the main source of IR losses with low power consumption [4]. Hence QCA [5] is more prudent than CMOS technology.

Many QCA logic designs have been implemented during recent years. Various 5–input majority gates [6-15], 1-bit full adder designs [6-8, 10, 12, 14, 16, 17-29], multiplier designs [30-33], RAM cell structures [34-35], flip flops [36-39] and logic circuits [40, 41]. In the above work, most of the circuits were not potent and hence susceptible to various defects at fabrication level because of the wire-crossing structures of QCA cells. Here, an effective use of cross overs can reduce the number of QCA cells, complexity and total cost. Multiple cross over wire designs results in various fabrication defects [42] and area overhead. One can replace these multilayer structures with 45 degree rotated cells which results in coplanar cross over designs. Such coplanar cross over designs are utilizing two types

of QCA cells which results in a problem of increased fabrication cost and reduced robustness [43]. Hence there is a need to design robust single layer QCA structures which uses only single type QCA cells (that is 90 degree cells). The basic idea is to propose a design of a robust and energy efficient 5-input majority gate and investigate the energy dissipation of existing majority gate with PMG. The PMG proposed in this paper is utilizing lesser area with reduced power dissipation as compared to the best designs reported in the literature. The correctness of PMG is validated by designing a one bit full adder based on proposed gate.

In this work, a coplanar 5-input novel and efficient majority gate is proposed. To measure its effectiveness, 1-bit novel full adder structure is designed using PMG. The remaining paper is arranged as follows. Section 2 showcase the basic concept of QCA structure and the clocking concepts. Section 3 describes the existing QCA based five input majority gates. Section 4 describes a proposed 5-input novel majority gate design, simulation results, its physical proof and energy dissipation analysis. The energy dissipation analysis is done using QCAPro tool. Section 5 represents a new robust full adder circuit design using the PMG, its simulation, energy dissipation analysis and comparison of proposed robust full adder circuit with the existing designs in terms of area and delay. Section 6 compares the result of PMG with the existing designs in terms of occupational area and interference. The Conclusion is presented in section 7.

2. REVIEW OF A QCA CELL

QCA cell is the fundamental nano structure which can construct all elements of a circuit (wiring and computing). A basic QCA cell is having four quantum dots placed at the extreme edges of a quantum cell. Out of which, two quantum dots contain free electrons in a diagonal direction. These two electrons can exchange their positions by lowering the barrier potential between them to achieve P=+1 (logic 0) or P=-1 (logic 1) polarization state [16] as depicted in Figure 1. These two free electrons confines with in a QCA cell and can never tunnel between the adjacent QCA cells. Hence when array of QCA cells placed adjacent to one another to form a wire, only a polarization state (columbic charge) will travel along the wire. Such an array of QCA cells can be used to construct wire or any logic structure. Hence there is less power dissipation because of the change in the polarisation and propagation of columbic charge (absence of flow of electrons). Therefore a QCA technology can be an alternative to that of a CMOS technology. The digital structure in QCA is designed by joining these cells in cascade.
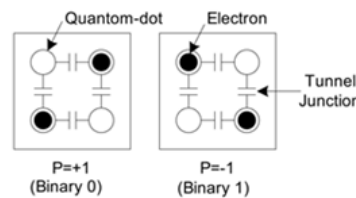

Figure 1. QCA cells with two polarization states

2.1. Basic structures

By connecting basic QCA cells in cascade, a wire can be formed shown in Figure 2(a). Other QCA structures like inverter and majority gate of three inputs can also be constructed using these quantum cells. An inverter circuit of Figure 2(b) invert its state because the output cell is in the diagonal orientation (interaction) with respect to the adjacent QCA cell. A majority gate works on the principle that the value of the output cell is true if majority of the input QCA cells are true. The QCA structure of a 3-input majority gate is illustrated in Figure 2(c). This gate can be further configured to form AND and OR gate structures. The function of 3-input majority gate is exhibited by the following equation:

$$M(A, B, C) = AB + BC + AC \qquad (1)$$

The majority gate with 5-inputs based designs are much faster and are having less area as compared to the same designs made using the majority gate with 3-inputs. Figure 2(d) represents a basic structure of 5-input majority gate. Its Boolean function is described (2)

$$MG(A, B, C, D, E) = ABC + ABD + ABE + ACD + ACE + ADE + BCD + BCE + BDE + CDE \qquad (2)$$
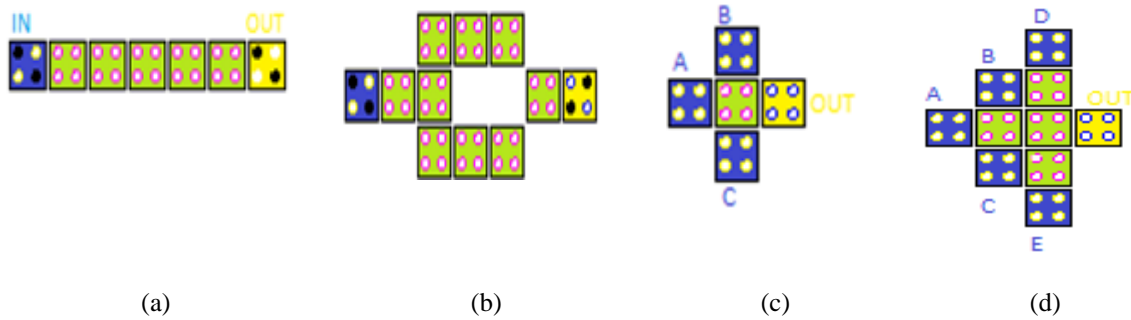
(a)	(b)	(c)	(d)

Figure 2. (a) QCA Wire, (b) Inverter gate, (c) 3-Input Majority gate, (d) 5-input Majority gate

2.2. Clocking

In switch phase, the barrier potential of a QCA cell starts increasing, hence moving from unpolarized state to polarized state. In this state, the polarization state of the QCA cell will depend upon its neighboring cells. In Hold phase, the barrier potential will remain constant and the QCA cell is completely polarized. Now it becomes independent of its neighboring cells. In release phase, the barrier potential of QCA cell starts reducing, hence moving from polarized state to unpolarized state. In relax phase, the barrier potential of the QCA cell becomes zero and hence the cell will be unpolarized.
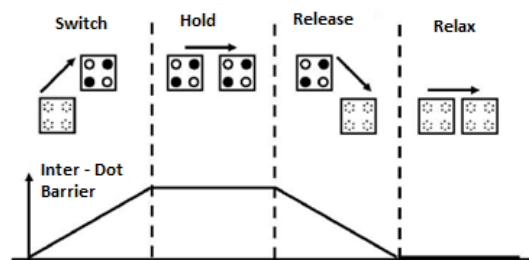
Figure 3. QCA clocking with four phases

3. EXISTING 5-INPUT MAJORITY GATES BASED ON QCA

In addition to 3-input majority gate design many researchers tried to implement the digital circuits using 5-Input majority gate. The purpose of designing digital circuits using 5-input Majority gate is reduced area, latency, faster speed of operation than the traditional designs. Various five input majority gates existing in the literature are described in this section. Many digital circuits implementing 5-Input Majority gate using (2) have been designed in [6, 8, 19, 22, 24].

The design [6] shown in Figure 4(a), is utilizing only 10 QCA cells with an area of $0.01\mu m^2$. This 5-input majority gate is having a drawback that its output QCA cell is trapped by the input QCA cells, hence limited the access of output cell in a single layer only. The majority gate design [8] Figure 4(b) also utilizing 10 QCA cells with an area of $0.01\mu m^2$ but it causes an interference between the input QCA cells as they are too close to each other. However the design presented in [22] depicted in Figure 4(c), tries to overcome the previous disadvantages but at the cost of increased area from $0.01\mu m^2$ to $0.02\mu m^2$. The designs in [19] and [24] Figure 4(d) and Figure 4(e) also shows the improvement in terms of no interference and accessibility to single as well as multi-layer designs. These designs are not so encouraging because of their increased up to $0.03\mu m^2$. The design in [19] is utilizing 42 QCA cells whereas the design in are using 51 QCA cells [24].
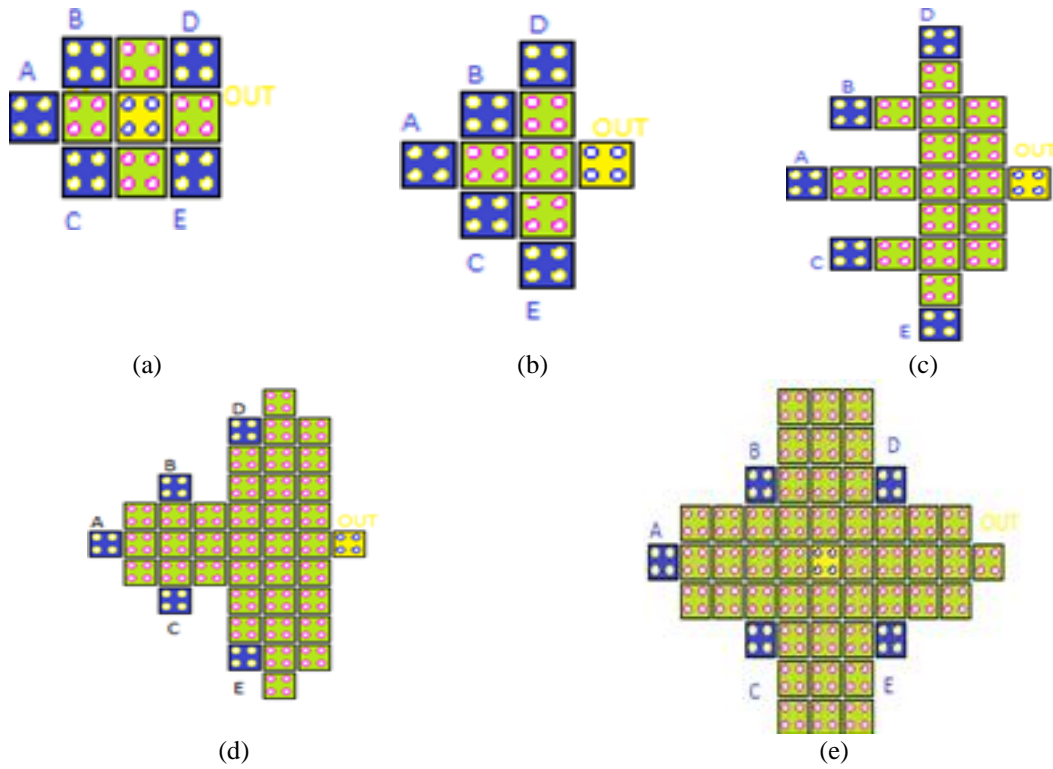
Figure 4. Various 5-input majority gates (a-e) design

4. PROPOSED FIVE-INPUT MAJORITY GATE (PMG)
4.1. Structural analysis

The five input novel majority gate proposed in this paper is utilizing 17 QCA cells having an area of 0.01 μm^2 as shown in Figure 5(a). It has no interference between the input cells and can be used for both single layer as well as multi-layer design. Figure 5(b) shows the simulation waveform for the PMG. From the simulation results, it is clear that when majority number of inputs are at high logic then the output is also at logic high.

(a)
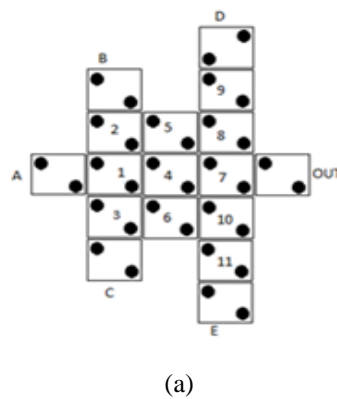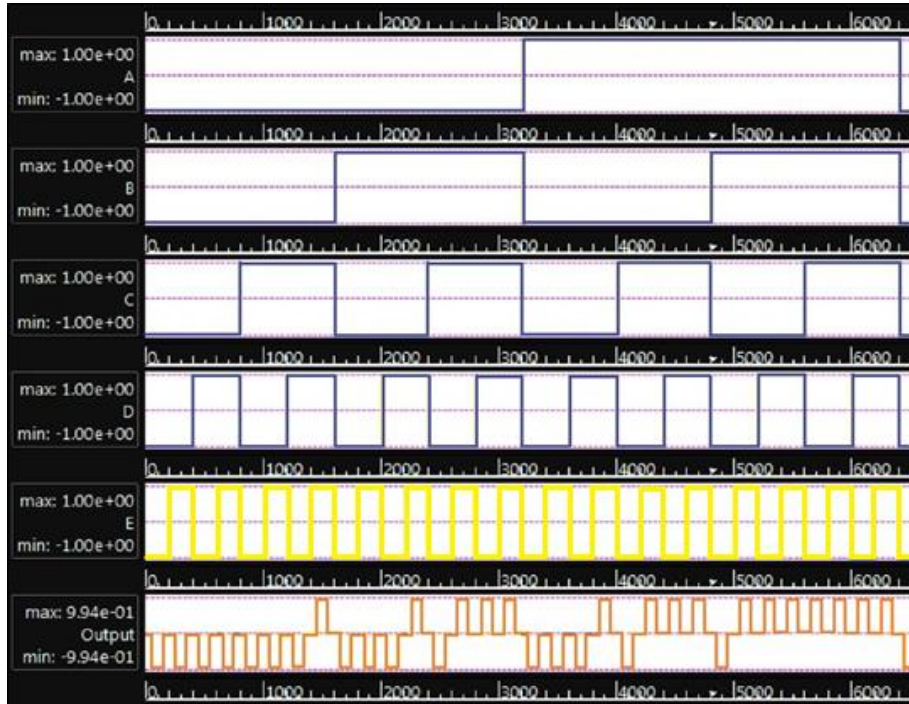
(b)

Figure 5. The Proposed five input majority gate, (a) Structure, (b) Simulation results

4.2. Physical proof

The proposed 5-input coplanar majority gate (PMG) has 2^5=32 input combinations. Accuracy of these 32 input combinations need to be verified but due to insufficient space, only one state is proven for consideration. Rest of the other states can be similarly verified. All the QCA cells of PMG are of equal size (18nm*18nm) and are separated from each other by 2nm space. The electrons in each cell are positioned in a manner that they must acquire minimum potential energy to become stable. The lesser the potential energy of a qca cell, the more stable it is.The potential energy between two electron charges in a QCA cell can be calculated as:

$$U = \frac{kq_1q_2}{r} = \frac{A}{r} \tag{3}$$

$Where\ A = kq_1q_2 = 9 * 10^9 * (1.6)^2 * 10^{-38} = 23.04 * 10^{-29}$ (4)

Where, U=Potential Energy, K=Coulomb' s law Constant, r=distance between two electrons and q_1 and q_2 are charges of electrons.

$$U_T = \sum_{i=1}^{n} U_i \tag{5}$$

Where U_T=Summation of potential energies [34, 44].

In this section, the stability analysis of proposed PMG is done on one state that isA=B=C=E=1 and D=0, by finding the potential energy between Input cells (i.e. A, B, C, D and E) and their corresponding middle cells (I.e. cell no. 1, 2, 3, 9 and 11). Figures 6(a, b) shows Cell 1 with electrons x and y in two different states. Next step is to find which state is more stable by calculating their potential energies separately.
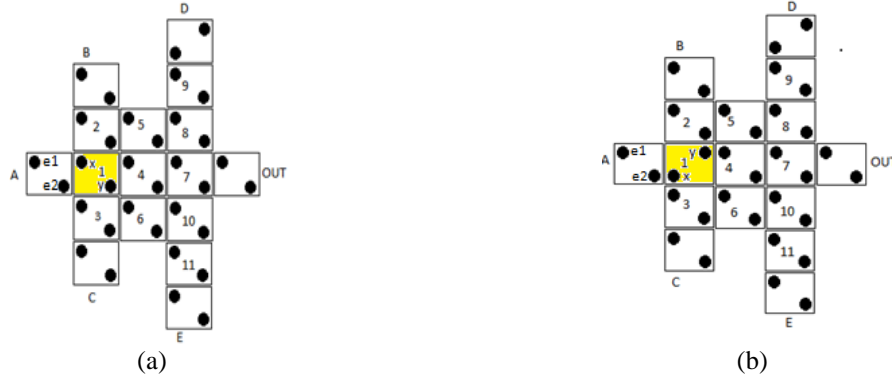
Figure 6. Two states of cell 1,(a) Cell 1=Logic "1", (b) Cell 1=logic "0"

Firstly the potential energy of cell 1(highlighted with yellow colour) in Figure 6(a) will be calculated, when the value of cell 1 is logic '1'. The polarization of cell 1 is affected by input cell A only because it is the only adjacent input cell for cell 1.The potential energy of electron x (U_x) is calculated with reference to electron e1 and e2 called as U_{x1} and U_{x2}. In the simillar way potential energy of electron y (U_y) is calculated withreference to electron e1 and e2 called as U_{y1} and U_{y2}. The calculation of potential energies U_{x1}, U_{x2}, U_{y1} and U_{y2} are given below:

$$U_{x1} = \frac{A}{r1} = \frac{23.04 * 10^{-29}}{20} \approx 1.152 * 10^{-20} \text{ (J)} \qquad U_{y1} = \frac{A}{r1} = \frac{23.04 * 10^{-29}}{42.04} \approx 0.5479 * 10^{-20} \text{ (J)}$$

$$U_{x2} = \frac{A}{r1} = \frac{23.04 * 10^{-29}}{18.11} \approx 0.07024 * 10^{-20} \text{ (J)} \qquad Uy_2 = \frac{A}{r1} = \frac{23.04 * 10^{-29}}{20} \approx 1.152 * 10^{-20} \text{ (J)}$$

$$U_x = \sum_{i=1}^{2} U_{xi} = 1.222 * 10^{-20} \text{ (J)} \qquad U_y = \sum_{i=1}^{2} U_{yi} = 1.6999 * 10^{-20} \text{ (J)}$$

$$U_{T11} = U_x + U_y = 2.92219 * 10^{-20} \text{ (J)}$$

Where, UT_{11} is the total potential energy of cell1 when it is at the '1' state.
Similarly the results of U_{x1}, U_{x2}, U_{y1} and U_{y2} are calculated when the value of cell 1 is at logic '0' as shown in Figure 6(b).

$$U_x = \sum_{i=1}^{2} U_i = 12.376 * 10^{-20} \text{ (J)} \qquad U_y = \sum_{i=1}^{2} U_i = 1.46258 * 10^{-20} \text{ (J)}$$

Where, UT_{10} is the total potential energy of cell1 when it is at the '0' state. The results shows that the potential energy of UT_{11} is lower than the UT_{10}. So the Cell1 will acquire the polarization state of '1' because it achieves lower potential energy with more stability.
In the same way the potential energies of other middle cells which are adjacent to input cells will be calculated by assuming them to be at the state "1" and "0" respectively. The final results of potential energies for adjacent middle cells (2, 3, 9, and 11) are given below.

Cell 2:   At Logic "1"$U_{T21} = 4.1239 * 10^{-20}(j)$
               At Logic "0"$U_{T20} = 13.8387 * 10^{-20}(j)$
Cell 3:   At Logic "1"$U_{T31} = 4.1241 * 10^{-20}(j)$
               At Logic "0"$U_{T30} = 13.8387 * 10^{-20}(j)$
Cell 9:   At Logic "1"$U_{T91} = 13.8387 * 10^{-20}(j)$
               At Logic "0"$U_{T90} = 4.1240 * 10^{-20}(j)$
Cell 11:   At Logic "1"$U_{T111} = 4.1241 * 10^{-20}(j)$
               At Logic "0"$U_{T110} = 13.8387 * 10^{-20}(j)$

From the above results, it is clear that when the inputs are A=B=C=E=1 and D=0, then cell 2, Cell 3 and Cell 11 will remain at the logic 1 because potential energies UT_{21}, UT_{31}, UT_{111} are less than UT_{20}, UT_{30} and UT_{110} respectively. Whereas Cell 9 will be at the logic 0 because UT_{90} is lesser than UT_{91}. This is practically true also because its adjacent input Cell D is at logic 0. By considering the achieved results, the proposed QCA structure for implementing 5-input novel majority gate is fully correct and results in a precise output.

4.2. Energy dissipation analysis

Low power dissipation, even below traditional *KT*, is one of the main feature of QCA nanotechnology. QCAPro is one of the accurate power estimation tool which uses non-adiabatic power dissipation model to estimate the switching power loss in QCA [44]. The basics of this model was taken from quasi adiabatic model in [23]. According to this model, the expectation energy value of cell for every clock cycle is described as:

$$E = \frac{\hbar}{2}.\vec{\Gamma}.\vec{\lambda} \tag{6}$$

Where, $\vec{\lambda}$ = coherence vector $\vec{\Gamma}$ = 3D energy vector
Now, the total power of single QCA cell at any instant is:

$$P_{total} = \frac{dE}{dt} = \frac{d}{dt}\left[\frac{\hbar}{2}.\vec{\Gamma}.\vec{\lambda}\right] = \frac{\hbar}{2}\left[\frac{d\vec{\Gamma}}{dt}.\vec{\lambda}\right] + \frac{\hbar}{2}\left[\vec{\Gamma}.\frac{d\vec{\lambda}}{dt}\right] = P_1 + P_2 \tag{7}$$

The first term i.e. $P_1 = \frac{\hbar}{2}\left[\frac{d\vec{\Gamma}}{dt}.\vec{\lambda}\right]$ indicates two components, first is transfer of power from clock signal to the QCA cell and the second is power gain due to the difference in input and output signal power.

The second term $P_2 = \frac{\hbar}{2}\left[\vec{\Gamma}.\frac{d\vec{\lambda}}{dt}\right]$ indicates instantaneous power dissipation. In one clock cycle, the energy dissipation in a QCA cell is calculated by integrating P_2 over time. Therefore,

$$E_{diss} = \int_{-T}^{T} P_2 \, dt = \frac{\hbar}{2}\int_{-T}^{T}\vec{\Gamma}.\frac{d\vec{\lambda}}{dt} \, dt \tag{8}$$

$$E_{diss} = \frac{\hbar}{2}\left(\left[\vec{\Gamma}.\vec{\lambda}\right]_{-T}^{T} - \int_{-T}^{T}\vec{\lambda}.\frac{d\vec{\Gamma}}{dt} \, dt\right) \tag{9}$$

The value of energy dissipation is maximum for maximum changing rate of $\vec{\Gamma}$. So the upper bound power dissipation is given by:

$$P_{diss} = \frac{E_{diss}}{T_{cc}}\langle\frac{\hbar}{2T_{cc}}\vec{\Gamma}_+ \times \left[-\frac{\vec{\Gamma}_+}{|\vec{\Gamma}_+|}\tan h\left(\frac{\hbar|\vec{\Gamma}_+|}{k_BT}\right) + \frac{\vec{\Gamma}_-}{|\vec{\Gamma}_-|}\tan h\left(\frac{\hbar|\vec{\Gamma}_-|}{k_BT}\right)\right]\rangle \tag{10}$$

Here, k_B represents Boltzmann Constant, T represents temperature. The author of [33] has presented a power dissipation model in which total power is classified as leakage power and switching power. Here leakage power is a power loss at clock transitions at leading edge or trailing edge of the pulse and switching power loss is due to the switching state of the cell. Based upon this, a tool called QCAPro is developed which estimates average power dissipation of the circuit.

In this paper, the energy dissipation of proposed 5-input coplanar majority gate is analyzed. For this switching energy, leakage energy and total energy dissipation is calculated for three different tunneling energies Table 1 at temperature T=2K. Also the results of proposed 5-input coplanar majority gate is compared with the existing structures proposed in [6, 8, 19, 22, 24]. Table 1 presents energy dissipation analysis of PMG and the previous existing designs. The comparative results of leakage, switching and total energy dissipation are also illustrated in Figures 7(a, b, c) respectively. The results calculated in Table 1 concludes that the proposed 5-input coplanar majority gate design has 20.1% less switching energy, 10.5% less leakage energy and 21.1% less total energy dissipation than the best conferred design in [25] for single layer as well as multi-layer design at 1.0Ek tunneling energy level. The existing designs in [6, 8] cannot be used for single layer design. So in the graph Figure 7 our results are compared only with the designs that can be used for single layer as well as multilayer structures. Figure 8 shows the thermal layout of proposed five input majority gate at temperature 2.0k with tunneling energy of 0.5ek. In this, the darker QCA cells indicate more average energy dissipation where as white cells represents the inputs.

Table 1. Energy dissipation analysis of proposed 5-input coplanar majority gate (PMG) and previous designs at temperature, T=2K

| 5 input Majority Gate design	Average leakage Energy Dissipation (meV)			Average Switching Energy Dissipation (meV)			Average Energy Dissipation of the circuit (meV)		
	$0.5E_k$	$1.0E_k$	$1.5E_k$	$0.5E_k$	$1.0E_k$	$1.5E_k$	$0.5E_k$	$1.0E_k$	$1.5E_k$
	1.28	4.14	7.69	11.53	10.37	9.16	12.81	14.51	16.85
	1.35	4.25	7.8	10.94	9.84	8.7	12.29	14.09	16.5
	4.4	11.33	24.2	35.78	32.8	29.64	40.18	46.09	53.84
	8.2	26.14	49.15	117.57	110.66	102.67	125.77	136.8	151.82
	6.33	17.34	38.22	92.44	86.45	76.44	98.77	103.79	114.66
PMG	3.32	10.14	18.4	28.74	26.19	23.57	32.06	36.33	41.98

(a)

(b)

(c)
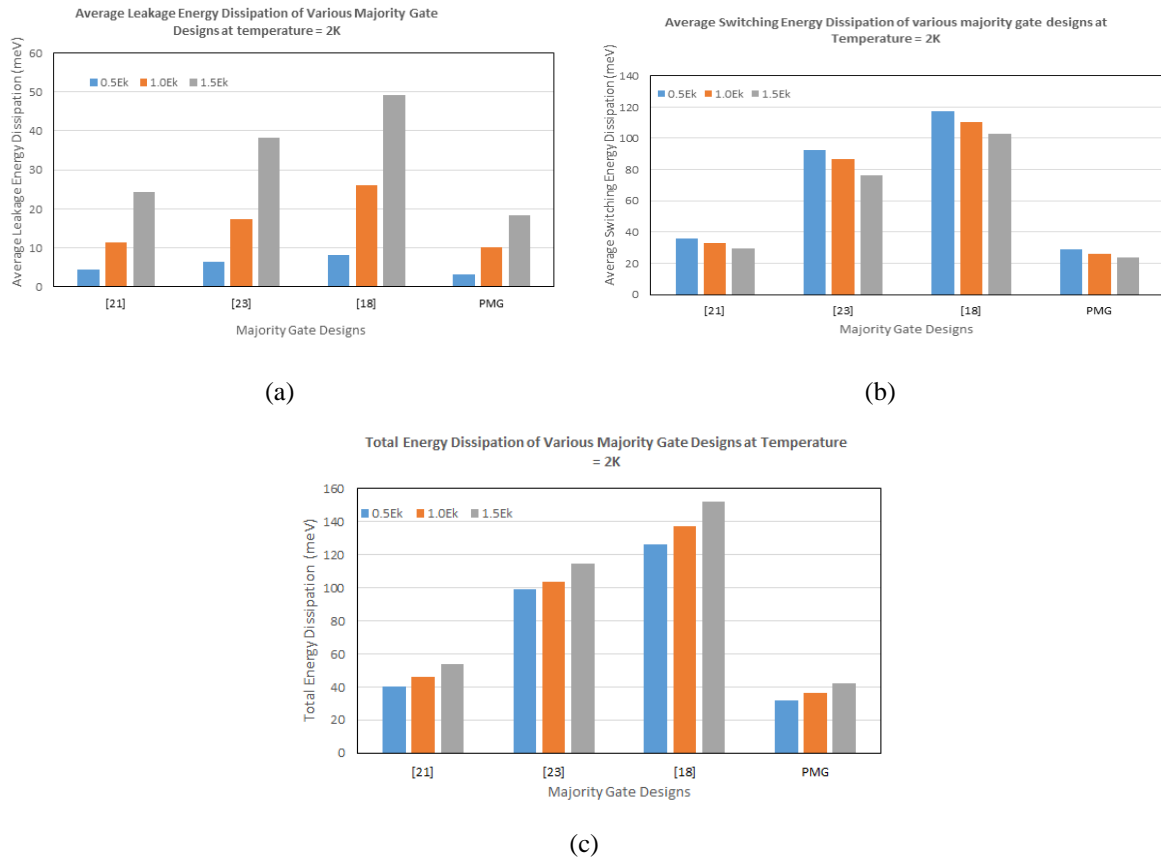
Figure 7. (a) Leakage energy dissipation, (b) Switching energy dissipation and, (c) Total energy dissipation of the PMG at three different tunneling energies (at T=2.0k)
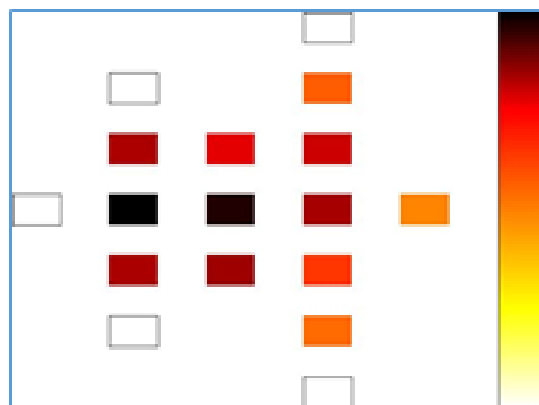

Figur 8. Thermal layout of PMG at temperature 2K (Tunneling energy=0.5ek)

5. SINGLE BIT QCA FULL ADDER

5.1. Proposed 1-bit full adder

The correctness of proposed coplanar majority gate (PMG) is validated by designing a full Adder structure using proposed gate. The structure of proposed full adder (PFA) using PMG is shown in Figure 9(a). Its QCA equivalent and simulations are represented in Figurs 9(b, c). The PFA circuit adds the two input bits A and B and carry C. The output is taken from SUM and CARRY bits. The PFA structure outperforms the previous designs with 58 QCA cells, occupational area of $0.05\mu m^2$, gate count of 4 and input to output delay of 1 clock cycle. Its energy dissipation analysis is also done using QCAPro tool and its results are shown in Table 2. The PFA dissipates 129.97 meV energy at $0.5E_k$ tunneling energy, 154.73 meV energy at 1.0 E_k tunneling energy and 186.61 meV energy at $1.5E_k$ tunneling energy at the temperature of 2K.

(a)

(b)

(c)
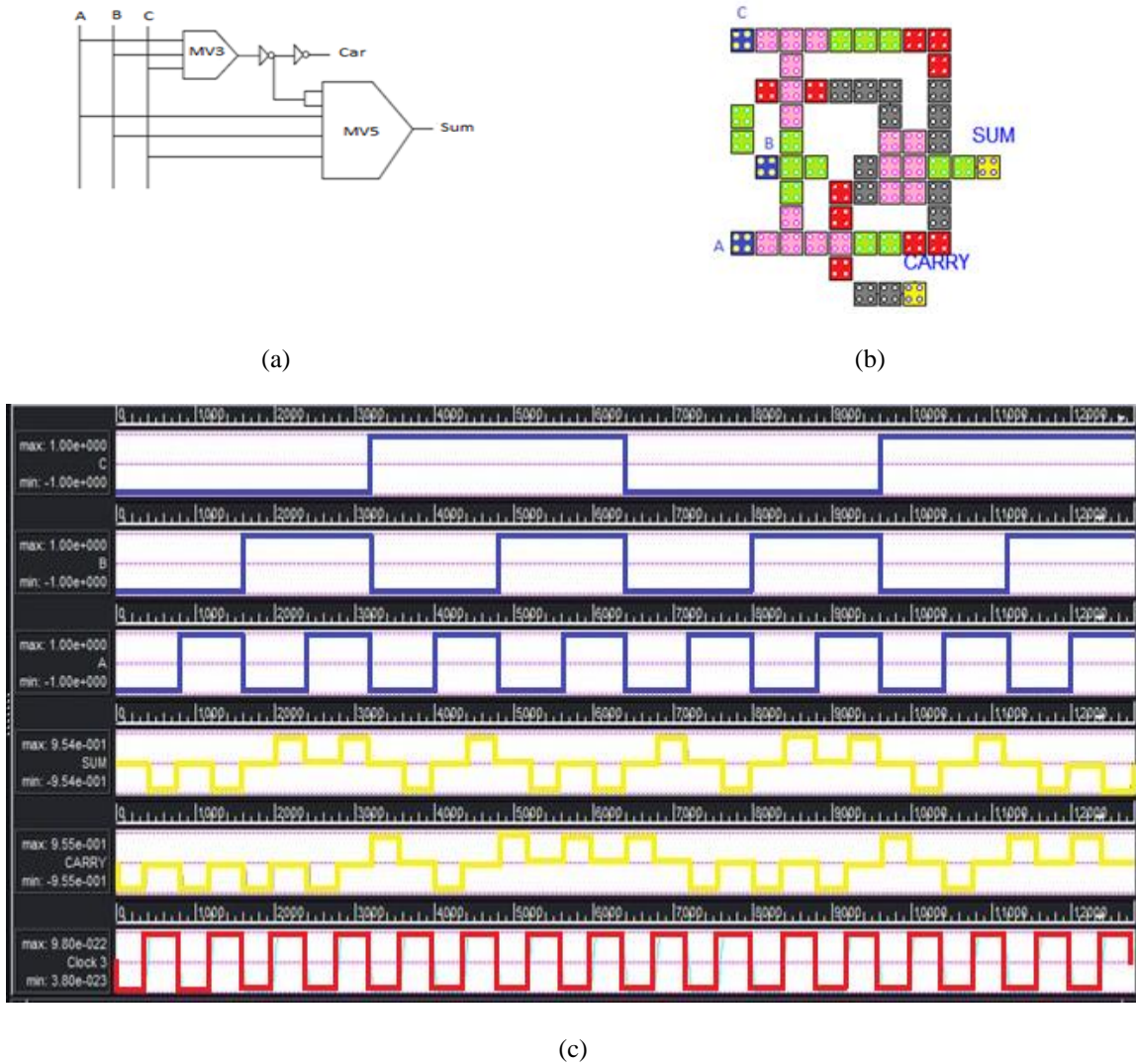
Figure 9. Proposed full adder, (a) Circuit diagram, (b) QCA implementation, (c) Simulation results of proposed 1-bit full adder

Table 2. Energy dissipation analysis of PFA design for tunneling energies $0.5E_k$, $1.0E_k$ and $1.5*E_k$ at T=2K

Tunneling Energy	Average leakage Energy Dissipation (meV)	Average Switching Energy Dissipation (meV)	Average Energy Dissipation of the circuit (meV)
$0.5E_k$	19.62	110.35	129.97
$1.0E_k$	57.97	96.76	154.73
$1.5E_k$	102.92	83.69	186.61

Here existing QCA based full adder designs are compared with a new full adder design based upon PMG. The proposed full adder design (PFA) outperforms the existing presented designs in terms of latency and occupational area. The comparison of PFA with the existing designs is presented in Table 3. The PFA design shows 16.6% enhancement in occupational area and 33.3% enhancement in latency in comparison to the best design conferred in for single layer as well as multi-layer design [11].

Table 3. Comparison of proposed full adder with the existing layout

Full adder designs	Number of cells	Area (μm^2)	Latency (clock cycles)	Coplanar
[20]	135	0.14	1.25	No
[29]	105	0.14	0.75	No
[31]	95	0.08	2	No
[24]	93	0.08	1	No
[28]	82	0.09	0.75	No
[13]	79	0.05	1.25	No
[30]	79	0.06	1	No
[27]	73	0.08	0.75	No
[8]	73	0.04	0.75	No
[6]	61	0.03	0.75	No
[9]	52	0.04	0.75	No
[13]	51	0.03	0.75	No
[15]	292	0.62	3.5	Yes
[16]	220	0.36	3	Yes
[19]	145	0.16	1	Yes
[25]	105	0.17	1	Yes
[26]	102	0.097	2	Yes
[11]	71	0.06	1.5	Yes
Proposed	58	0.05	1	Yes

6. COMPARISON OF PMG WITH EXISTING DESIGNS

The proposed 5-Input coplanar majority gate is verified by a QCADesigner tool. The simulation is done for bistable and coherence vector simulation engine setup for which the total number of samples taken is 32000 with temperature of 2K. The simulations of PMG are done at the default value of relative permittivity of 12.9 for GaAs and AlGaAs heterostructure implementation. Table 4 depicts the comparison of PMG with the existing designs. It is illustrated that the PMG design occupies an area of 0.01 (μm^2) which is 50% less as compared to the best design presented in [22] for single layer as well as multi-layer design.

Table 4. Comparison of PMG with the existing layouts

QCA Layout Design in	No. of QCA cells	Area (μm^2)	Interference	Single Layer Structure	Multi-Layer Structure
[21]	22	0.02	No	Yes	Yes
[18]	42	0.034	No	Yes	Yes
[23]	51	0.038	No	No	Yes
Proposed Layout	17	0.01	No	Yes	Yes

7. CONCLUSION

In this paper, a novel 5-input coplanar majority gate design with its physical proof is presented. The detailed analysis and energy dissipation of proposed gate were performed. To authenticate the correctness of the proposed gate, a full adder circuit is designed and their power analysis is also done. The results proved that the proposed designs have outgrown all previous mentioned structures and shows remarkable improvement in terms of latency, occupational area, complexity and average energy dissipation. The designs have been verified at three different tunneling energies that is 0.5 Ek, 1.0Ek and 1.5Ek at the temperature of 2K. The total energy dissipation of the circuit is computed as the sum of average leakage energy and switching energy dissipation. The PMG design has 21.1% less total energy dissipation than the best reported circuits in at a tunneling energy level of 1.0Ek [22].

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