International Journal of Reconfigurable and Embedded Systems (IJRES)
Vol. 9, No. 1, March 2020, pp. 19~27
ISSN: 2089-4864, DOI: 10.11591/ijres.v9.i1.pp19-27

Two state-of-the-arts current-mode ternary full adders based on CNTFET technology

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Article Info

Article history:

Received Apr 16, 2019
Revised Oct 7, 2019
Accepted Nov 12, 2019

Keywords:

CNTFET
Current mode logic
MVL circuitry
Ternary full adder

ABSTRACT

Adder core respecting to its various applications in VLSI circuits and systems is considered as the most critical building block in microprocessors, digital signal processors and arithmetic operations. Novel designs of a low power and complexity Current Mode 1-bit Full Adder cell based on CNTFET technology has been presented in this paper. Three major parts construct their structures; 1) the first part that converts current to voltage; 2) threshold detectors (TD); and 3) parallel paths to convey the output currents flow. Adjusting threshold voltages which are significant factor for setting threshold detectors switching point has been achieved by means of CNTFET technology. It would bring significant improvements in adjusting threshold voltages, regarding to its unique characterizations. Simple design, less transistor counts and static power dissipation and better performance comparing previous designs could be considered as some advantages of the novel designs.

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1. INTRODUCTION

In Current Mode Logic (CML), logical levels are represented by currents. This approach has its own pros and cons compared to the conventional Voltage Mode Logic (VML). The merits include: 1) the reduction of the number of active devices in a circuit by means of a simple wiring procedure [1]; 2) the ease of circuit development and producing several multiple-input circuits by using different Threshold Detectors (TDs) [2]; 3) the elimination of sign bit by applying the direction of current to describe the sign [1]; 4) less noise sensitivity [3, 4]; 5) the usage of current mirrors for current scaling and duplication [4, 5]; and 6) high-speed operation [4, 5]. The main disadvantage of CML is its high static power consumption [5, 6]. Regarding the requirement of higher speed, it is expected that current mode approaches become even more important in near future [6, 7].

Traditionally, bipolar and MOS devices have been utilized to implement current mode circuits. The latter is often selected for mixed analog-digital signal environments. Meanwhile, MOSFETs benefit from higher supply noise immunity [3-6], and less power consumption.

Multiple-Valued Logic (MVL) approach uses more than two logic levels. It relies on the increment of logic levels, whereas Binary logic computations are based on only two values (‘0’ and ‘1’). MVL benefits from fewer interconnections and pinouts, less area dissipation, and higher parallel and serial communication rates [1]. These advantages with regards to the serious challenges of interconnections and the amount of wire congestion in nanoscale chips, make MVL as an alternative design technique for Binary circuits [5, 6].

In short, MVL is a mixture of binary logic and analogue signal processing. It takes advantage of both noise tolerance of a digital signal and more information processing in analogue mode [8]. Among different MVL systems, Ternary logic brings about less product cost and complexity comparing to Binary logic [8-11].

Voltage-mode MVL circuits suffer from the reduction of voltage swing during encoding more than two logic levels [12]. The current-mode technique seems to be a possible solution to overcome the challenge. This approach utilizes current as a signal carrier, either alone or in mixture with voltage [12]. Regarding the design simplicity and less noise sensitivity, the current mode approach can be considered as a worthy technique for designing MVL circuits [12-14].

For many years, MOSFET technology has been considered as the premier technology, providing the vital potentials to implement energy-efficient and dense VLSI circuits. However, the trend of scaling down the feature size of CMOS technology in nano-ranges in today`s nanometer VLSI industry leads to numerous challenges. Carbon NanoTube Field Effect Transistor (CNTFET) [15], owing to its unique specifications and the ability of adjusting the desired threshold voltage, has achieved considerable attention as a successor to the MOS technology in near future, especially for MVL designs.

This paper presents new Ternary Full Adder cells. They are based on CNTFET technology and CML design approach. Full Adder is considered as the most important component [16-18] because of its consequential role in digital signal processors, microprocessors, and arithmetic operations and computations. Therefore, its efficiency impacts the performance of a system as a whole [16, 17]. The new proposed circuits are built on mixed current and voltage signals. A constant current source is applied respecting to the logical relationship between the sum of input currents and constant current value. Hence, power dissipation is reduced in comparison with the previously presented structures.

The rest of the paper is organized as follows: Section 2 reviews the previously presented current-mode Ternary Full Adders in the literature and their transistor-level implementation will be presented. The proposed designs are presented in Section 3. Simulation results and comparisons are accessible in Section 4. Finally, section 5 draws the conclusion.

2. LITERATURE REVIEW

Full Adder can be used in MVL systems either in CML or VML mode, based on both MOSFET and CNTFET technologies [10, 12, 13]. Nevertheless, CNTFET-based adders provide higher performance [19-21]. Some current-mode Full Adders have been presented previously in [22-24] based on linear addition and subtraction of input currents. Their design simplicity can be considered as their major advantage. The presented CML Full Adder in [22] is specifically designed for fuzzy logic. In discrete systems and circuits the ability of generating full-swing outputs, even with non-full-swing input signals, is one of the essential characteristics. Fuzzy circuits do not provide this vital necessity. Their employment in digital systems most probably causes some problems such as malfunction and high noise sensitivity [5, 6].

Figure 1a display the first prior Ternary Full Adder circuit, presented in [24]. A threshold detector is implemented by using a constant independent current source whose function depends on which network it is situated:

- If the constant independent current source is placed in a pull-up network: In this case, whenever the sum of input currents (Σin) is less than a constant value (the threshold), the relevant p-type transistor turns off, since the rest of the current charges the gate capacitor of the p-type transistor.
- If the constant independent current source is placed in a pull-down network: The related p-type transistor switches on if the sum of input currents (Σin) is more than a constant value (the threshold).

The transistor-level implementations of a constant independent current source are exhibited in Figures 1b and 1c [23, 25]. Both implementations are used in this paper. The three positive logic values $\{0, 1, 2\}_3$ explain the unsigned Ternary digits. They are characterized in current-mode logic by different current levels. Each current unit is considered as 8μA. Therefore, logical values '0', '1', and '2' are equivalent to 0A, 8μA, and 16μA, respectively.

Figure 2 depicted the transistor-level implementations of the former Ternary Full Adder by two different constant independent current sources. Each transistor is marked by three values (numbers), which indicate the diameter of CNTs (D_{CNT}), the number of nanotubes under the gate terminal (Tube), and the pitch parameter. For example, a transistor with the values 0.783, 6, and 18 has two CNTs with the diameter of 0.783nm under its gate terminal. Therefore, its threshold voltage is 0.549V (1) [19-21]. Meanwhile, the distance between the centers of two adjacent CNTs is 18nm (Pitch=18nm). In addition, these designs need constant currents of 4μA, 8μA, 12μA, 20μA, 28μA, and 36μA as threshold detectors. Furthermore, current mirror circuits are used to duplicate the sum of input value currents (Σin).

$$V_{Th} \approx \frac{0.43}{D_{CNT}(nm)} \quad (1)$$

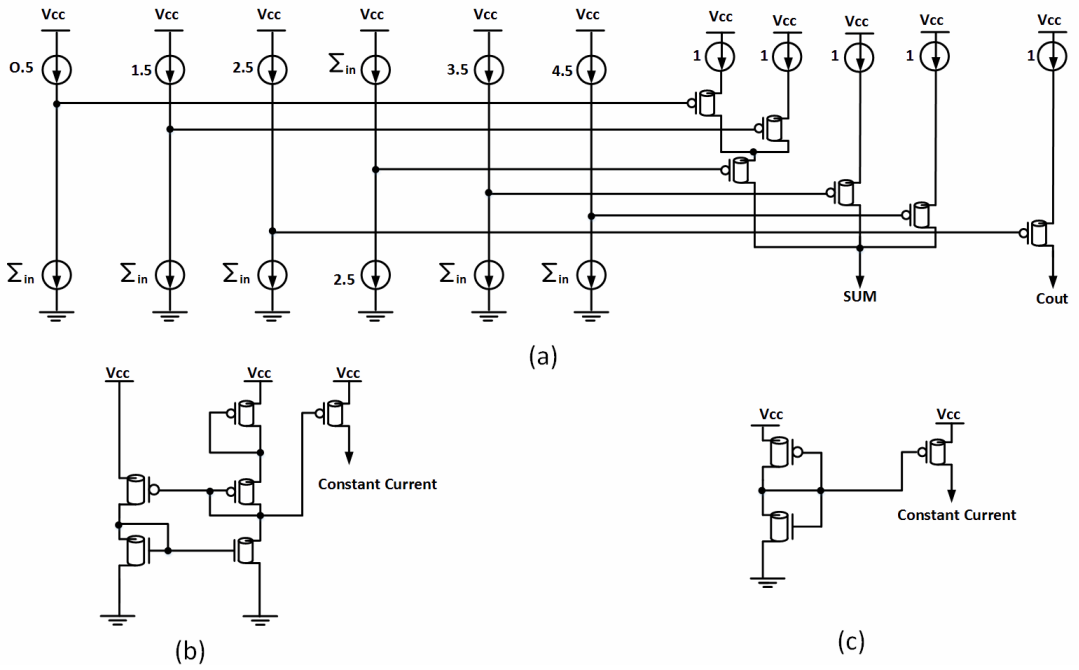

Figure 1. The previously presented circuits; (a) Ternary full adder [24], (b) independent current source [25], (c) Constant independent current source [23]

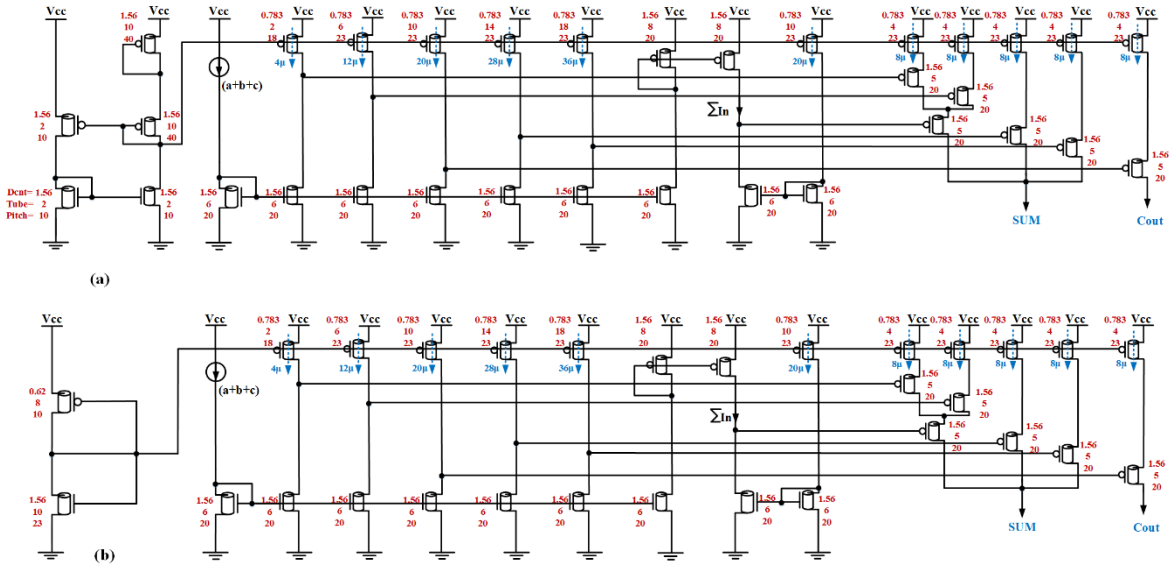

Figure 2. The previous current-mode circuits [24]; (a) with independent current source [25], (b) independent current source [23]

3. THE PROPOSED CURRENT-MODE TERNARY FULL ADDER (CMTFA)

In this section, it is explained the results of research and at the same time is given the comprehensive discussion. Results can be presented in figures, graphs, tables and others that make the reader understand easily [2, 5]. The discussion can be made in several sub-chapters.

Full Adder cells are principally considered among the most fundamental logic blocks. Respecting to their numerous applications in other mathematical operations, they could be used in many large and complex circuits and functional units such as multiplier and ALU [26, 27]. Table 1 shows the functionality of a current mode Ternary logic Full Adder based on its inputs summation. New Ternary Full Adder circuits based on CML and CNTFET technology are proposed separately in this section. They both exploit Multiple-Valued Current Mode Logic (MVCML) specifications [1, 6, 9] and the unique characteristics of CNTFET technology [19-21] like its flexibility in MVCML. Their designing method relies on converting the sum of the input currents to voltage. The switching activity of the final transistors is controlled by threshold detectors, which are located through the output paths. A unit of current flows if an output transistor switches on. Accordingly, the currents of two different paths are summed up to increase the amount of current to 16μA.

Table 1. The truth table of ternary full adder

$\Sigma in(a, b, C_{in})$	C_{out}	SUM
0	0	0
1	0	1
2	0	2
3	1	0
4	1	1
5	1	2
6	2	0

Figures 3 and 4 demonstrate the 1st and 2nd proposed CML Ternary Full Adder cells. A Full Adder cell includes three inputs (a, b and C_{in}) and two outputs (SUM and C_{out}). The presented technique is founded upon the sum of input currents. In CML, the simple connection of input wires provides the linear addition of inputs. In order to convert the sum of the input currents (Σin) to voltage, a diode-connected transistor (T_1) is used as a resistor. To achieve higher resistivity, the channel (L_g) and doped CNT source- (L_{ss}) and drain-side (L_{dd}) extension regions have been stretched to 100nm. Although the channel length increment makes more resistance, it does not decrease the operation speed, since the converting transistors do not impact the critical path of the whole cell [5, 7].

After the conversion, the threshold detectors (TDs) are responsible for controlling the switching activity of the rest of the transistors [5]. As mentioned earlier, the threshold value adjustment is accomplished by changing the diameter of CNTs (1) [19- 21].

Both proposed structures include a constant current source, which is responsible for generating a constant current value. T_5 and T_6 are used for this purpose. In (2) explains the way the output Sum is generated.

$$Sum = \Sigma in - 3I_1 - 3I_2 \quad (2)$$

The proposed Ternary Full Adder design uses two TDs, whose turning points are set as follows: For example, the output of the TD with switching point of $\frac{5.5}{6}$ would be equivalent to '0', if the summation of inputs (a, b, C_{in}) equals to (Σin=6) as shown in Figures 3 and 4. The presented Adder Cells do not need binary inverter, which leads to better performance.

The last part is the most important part of this structure. It defines the output values (SUM and C_{out}). It contains of different paths, through which the output currents flow. It is necessary to set the dimensions of the transistor(s) on a specific path properly. This leads to the precise unit of output current (0, 8μA, and 16μA).

Over and above, two parallel paths constructed by two transistors in each path T_3, T_7 and T_4, T_8 are used to generate SUM based on (2). However, T_2 directs the current of input summation (Σin). For Sum output, the current through the paths, including T_7, T_3 and T_8, T_4 would flow, based on TDs switching point and their related transistors. Transistors T_9 and T_{10} generate Cout values based on their switching status as shown in Figure 3.

The switching points of TDs are set properly so that T_3 and T_9 are switched on if Σin>3 and T_4, T_{10} are switched on if Σin>6(Figure 3).

The main functionality of the presented cells is as follows (Figure 3):

If the sum of the inputs equal to '0', transistors T_3, T_4, T_9, and T_{10} are switched off; accordingly both outputs would equal 0.

In case of (Σin=1), T_3, T_4, T_9, and T_{10} are switched off, while T_2 would be switched on. It copies the summation of input currents, so the 8μA current to the SUM output would be indicated, although C_{out} equals 0.

While (Σin=2), the threshold detector switches T_3, T_4, T_9, and T_{10} are switched off, while T_2 is switched on. Hence, the SUM current reaches 16μA, while C_{out} remains 0.

Regarding (Σin=3), the threshold detector switches T_3 and T_9 on, respecting to (2) the SUM output would be 0A, while C_{out} would be 8μA.

If (Σin=4), the threshold detector switches T_3 and T_9 on. Thus, SUM output equals to 8μA and C_{out} remains 8μA.

While (Σin=5), the transistors T_3 and T_9 switches on, in a same manner SUM output remains to 16μA and C_{out} continues 8μA.

Finally if (Σin=6), the threshold detector switches T_3 ,T_4,T_9,T_{10} on, hence SUM equals to 0A due to (2), while C_{out} would be 16μA because of the unification of two current flow paths.

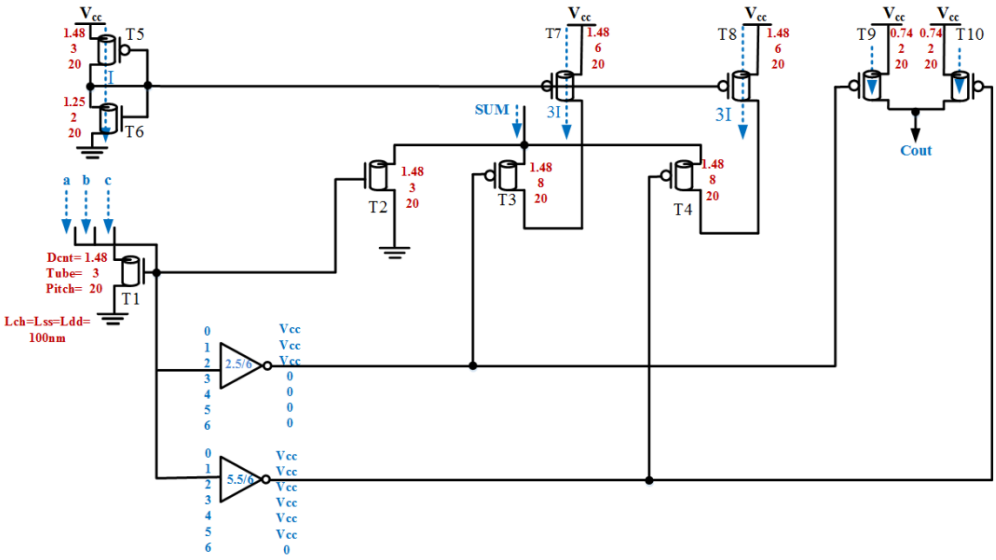

Figure 3. The 1st proposed current-mode ternary full adder (CMTFA1) with the current mirror in SUM generator module last part

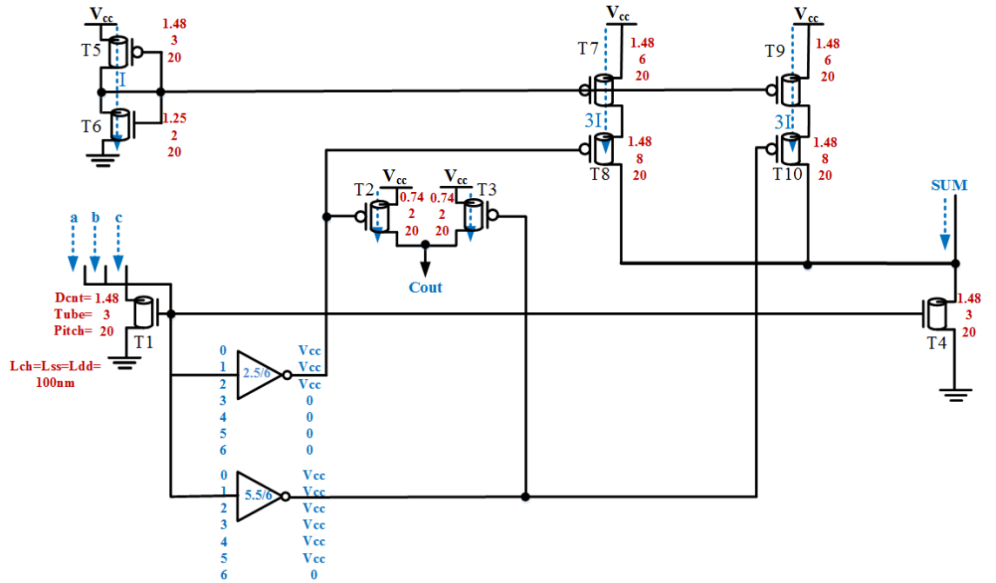

Figure 4. The 2nd proposed current-mode ternary full adder (CMTFA2) without the usage of current mirror in SUM generator module last part

4. RESULTS AND ANALYSIS

All of the proposed and previous designs (Figures 2, 3, 4) are simulated with Synopsys HSPICE and 32nm CNTFET technology [19, 20]. Simulations are done in 1V power supply with 1GHz operating frequency at room temperature.

A random input pattern (Figure 5) is fed to the Full Adder cells to measure the delay parameter. However, the complete Ternary Full Adder cells can generate the expected outputs if that the sum of inputs reaches to 6 ($0 \leq \Sigma in \leq 6$) (Figure 5).

The average power consumption is calculated during all of the transitions. The energy consumption (known as PDP), which makes a balance between delay and power, is calculated by the multiplication of delay time and power consumption [26, 27]. The average static power is also measured while the inputs are kept unchanged. All of the 27 possible different input patterns are fed to the circuits to measure the stand-by power dissipation. The average amount is reported as the static power. The simulation results are demonstrated in Table 2.

The proposed designs operate more efficiently than the previous ones. The simulation results show that the proposed Current-Mode Ternary Full Adders (CMTFA1 and CMTFA2) advantage from significant delay and power reductions, which is mainly due to the less transistor counts compared to the previous circuits. They also show greater reduction in terms of PDP, which originates from the elimination of a few transistors and shortening the critical path. Sensitivity to the variation of temperature is examined for the previous and proposed designs. The amount of energy consumption (PDP) versus a wide range of ambient temperatures, from 0°C to 70°C, is depicted in Figure 6. The proposed designs show insignificant sensitivity to temperature variations.

In addition, the capability of working in high frequencies such as 2GHz and 4GHz is examined for the previous and proposed designs. The results of energy consumption (PDP) versus frequency are depicted in Table 3.

Table 2. The simulation results

Designs	Delay (psec)	Average Power(μW)	PDP (fJ)	Static Power (μW)	No. of Transistors
Previous FA[24,25]	22.258	200.1	4.4537	186.87	33
Previous Modified FA[24,23]	22.498	161.69	3.6377	148.41	30
CMTFA1	14.498	49.186	0.71312	28.882	14
CMTFA2	17.631	49.307	0.86935	28.894	14

Table 3. The PDP variations versus frequency

Block		1GHZ	
	Delay (psec)	Power (μW)	PDP (fJ)
CMTFA1	14.498	49.186	0.71312
CMTFA2	17.631	49.307	0.86935
Previous FA[24,25]	22.258	200.1	4.4537
Previous Modified FA[24,23]	22.498	161.69	3.6377
Block		2GHZ	
	Delay (psec)	Power (μW)	PDP (fJ)
CMTFA1	14.793	49.204	0.72786
CMTFA2	17.972	49.349	8.8688
Previous FA[24,25]	22.246	200.35	4.4569
Previous Modified FA[24,23]	23.353	161.93	3.7816
Block		4GHZ	
	Delay (psec)	Power (μW)	PDP (fJ)
CMTFA1	14.87	49.248	0.73231
CMTFA2	17.875	49.44	0.88388
Previous FA[24,25]	21.017	200.81	4.2204
Previous Modified FA[24,23]	22.504	162.45	3.6558

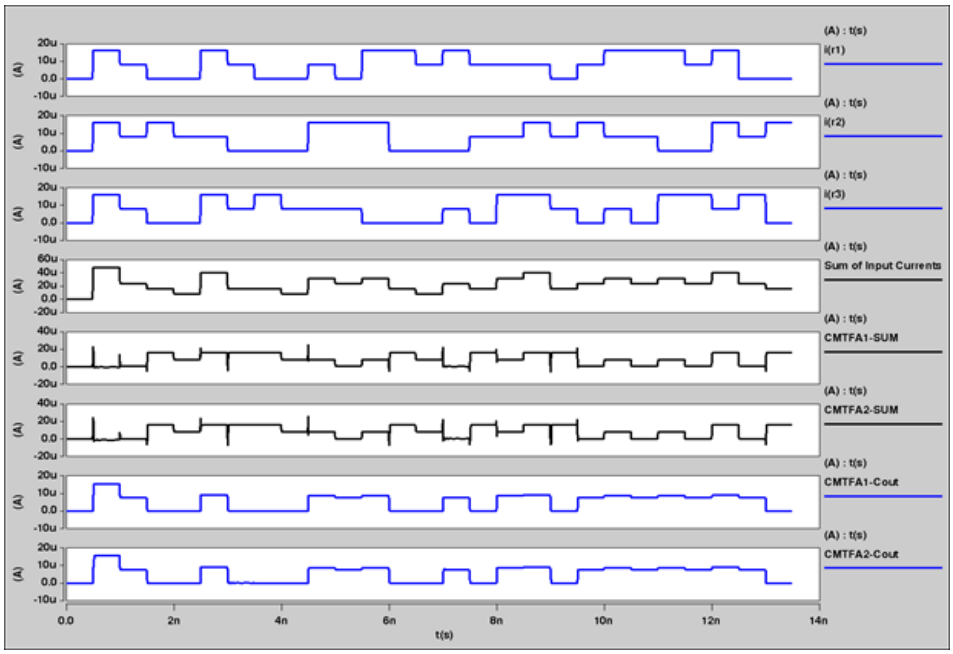

Figure 5. Input and output waveforms of proposed (CMTFA1,2)

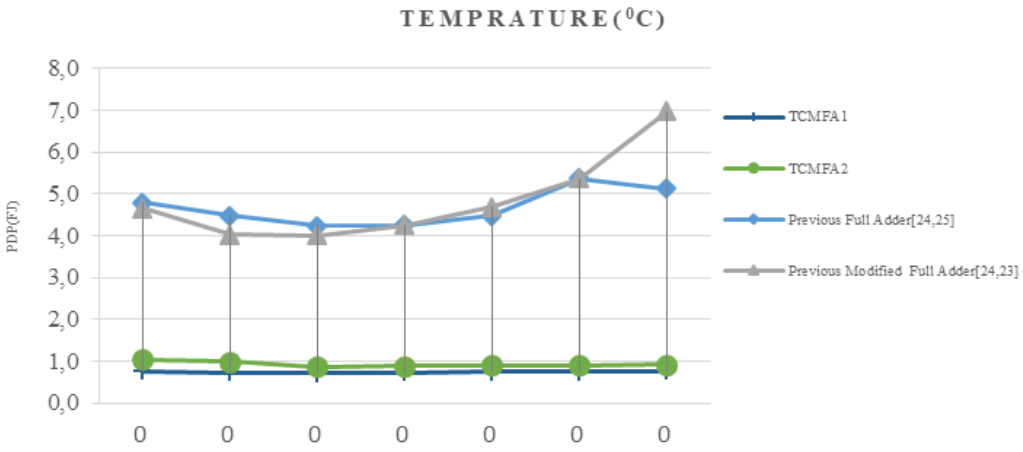

Figure 6. PDP versus temperature

One of the advantages of CML over VML is the elimination of speed degradation and performance loss when applying fan-out circuits. This mainly originates from the way that fan-out circuits are connected to a CML circuit [5]. To do this, the output currents are mirrored to the new branches, instead of a direct connection [5]. For this manner, simulations are redone twice more to investigate the mentioned capability: Firstly, with only one extra output load transistor. Secondly, four copies of the output current are also included in the analysis. Table 4 exhibits that the presence of the output load transistor and the connection of the fan-out circuits do not impact the cell delay time. These overheads do not increase extra load to the output nodes, whereas, voltage-mode circuits perform slower when the output load increases [5].

Table 4. Delay parameter of the proposed designs versus the output load(s)

Designs	Without any Load	With The Output Load Transistor	With The Output Load Transistor and 4 Copies of the Output Current
	Delay(ps)	Delay(ps)	Delay(ps)
CMTFA1	14.498	29.678	28.6790
CMTFA2	17.631	29.287	27.6020

5. CONCLUSION

New designs of Current Mode Ternary Full Adder cells based on CNTFET technology have been presented. The novel designs are based on mixed current and voltage logics. Adder cells respecting to their various applications could be designed in both CML and VML approaches, hence its performance can impact the performance of the system as a whole. The presented Ternary CML Full Adder cells based on CNTFET technology and MVCML specifications together, perform better than the previous cells. It can be utilized in mentioned applications in large CML circuits and units in future nano-electronics designs.

The novel designs of Full Adders lead to fewer transistors, TDs, and simple design. These specifications are due to higher performance of the proposed cells comparing the peer ones, which employ constant current sources as threshold detectors. It is worth to mention that conventional Ternary Full Adders must be able to perform with the complete sum of inputs (Σin=6), whereas the previous designs are not capable of adding Σin=6. Additionally, the load tolerance and capability of both proposed designs in large circuits have been studied. The simulation results indicate a great improvement in terms of power consumption, PDP, number of transistors, and driving capability. Regarding to simulation results, the best proposed CMTFA has approximately 80% higher efficiency than the best previous design in terms of PDP.

ACKNOWLEDGEMENTS

This paper has been supported by Young Researcher and Elite Club, Roudehen Branch, Islamic Azad University, Roudehen, Iran.

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