Design and implementation of CNTFET based ternary 1x1 memories

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Article Info	ABSTRACT
	In this paper presented Design and implementation of CNTFET based Ternary 1x1 RAM memories high-performance digital circuits. CNTFET Ternary 1x1 SRAM memories is implement using 32nm technology process. The CNTFET decresase the diameter and performance matrics like delay,power and power delay, The CNTFET Ternary 6T SRAM cell consists of two cross coupled Ternary inverters one is READ and another WRITE operations of the Ternary 6T SRAM cell are performed with the Tritline using HSPICE and Tanner tools in this tool is performed high accuracy. The novel based work can be used for Low Power Application and Access time is less of compared to the conventional CMOS Technology. The CNTFET Ternary 6T SRAM array module (1X1) in 32nm technology consumes only 0.412mW power and data access time is about 5.23ns.

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1. INTRODUCTION

The progress in traditional silicon technology continues to outpace the historic pace of Moore's Law, but however the end of device scaling now seem to be few years away. Therefore, it is of intense interest to find new, molecular-scale devices that might complement replace existing silicon technology and allow more advanced device scaling. As device sizes are approaching the nanoscale, new opportunities are also arising therefore; new materials and devices have been investigated to replace CMOS technology to carbon nanoscale technology from the year 2015 and beyond [1]. As one of the promising new devices, carbon nanotube FETs (CNTFETs) new nanoelectronic systems based on new devices with completely new system architectures, for examples:-nanotubes, nanowires, molecular devices, and novel device concepts for nanoelectronics [2]. Of the various material Systems and structures studied so far, carbon nanotubes have shown particular promise owing to their nanoscale size and unique electronic properties [3]. They have been also fabricated successfully and it is reported that they have shown performance is better than present silicon transistors size. Silicon-on-insulator (SOI) MOSFET. Several leakage current mechanisms in MOSFET such as reverse-bias p-n junction current, weak inversion current and drain induced barrier lowering (DIBL) current [4-7] are being introduced by short-channel effect. Tunneling effect in nanoscale MOSFET is also impacting the performance of the transistor However, in case of carbon nano-scale transistor as the transistor size and the distance between two transistors is also been scaled down, it cause the carriers of one transistor to cross the barrier and has effect to another transistor lying close to it. The tunneling effect is found to be increasing exponentially as the barrier distance is decreased [6] appropriate circuit design methods and process development strategies have to be devised in order to tackle the abovementioned issues on power dissipation and variability. This work concentrates on the CNT as one of the most promising of emerging nanodevices. Though holding a great promise for future electronics, CNTs are extremely prone to various

sources of variations. As the electrical characteristics of CNTs are directly related to their physical structure, atomic structural changes can translate into significant variation in their electronic behavior. This work aims to facilitate CNT-based design in the presence of CNT diameter and doping variations. To achieve this, an exhaustive study is carried out to examine the effects of CNT physical characteristics.

Variations on circuit performance variables. The effect of CNT diameter variations on performance parameters (delay, power consumption, etc.) of various logic and memory structures is studied in depth. Through various simulation strategies, an optimum CNT mean diameter for use in CNT based logic design is put forward for the first time. Further, novel mathematical models for the prediction of delay behavior of CNT-based circuits in the presence of diameter variations are developed [3]. Threshold voltage and gate oxide thickness are major issues/factor to introduce the reverse saturation current in nano-scale MOSFET transistor. Scaling down the conventional MOSFET not only bring to transistor performance issues but also to fabrication problem. The limitation of the MOSFET technology due to the fact that Zener breakdown will occur at source/substrate junction, lithography limitation and also the yield control for the product are the limitation to continue scaled the conventional MOSFET into smaller sizes. The low carrier mobility in silicon (compared to carbon nanotube) may be also degrade the MOSFET transistor performance. For these reasons, the new device CNFET with new channel material is being extensively explored. This project work uses same 32nm technology transistor channel length to prove that CNFET can provide better transistor performance compared to another technology CNTFET technology. The data collected from the simulation will be compared to 62nm CNTFET technology and conclude with some analysis.

This paper is organized in the following manner. In Section 1, we mainly are giving some brief introduction on utilization of carbon nanotube devices in recent technology. In section 2 A brief discussion on the structure of carbon nano tubes including chiral vector and metallic and semiconducting nanotube and also Synthesis of Nano tubes will be covered. In section 3 discussion on Simple Ternary inverter, positive ternary inverter and negative ternary inverter In Section4, we have implemented a Ternary 1x1 Sram Array Module circuit using Carbon Nanotube Field Effect Transistor (CNFET). The key performances of Ternary such as tritline conditioning circuit read sensing circuit and write driver circuit. This section focuses on low power and high speed inverter circuit design issues for CNFET technology In section 5 describes the design of ternary 1x1 sram section 5.1 describes the diameter, CNT pitch charality vector and number of tubes etc in section 6 simulation results using Hspice tools simulated the ternary 1x1 Sram simulation for logic 0,1/2,1are shown In section 7,in this section shows the performance of the ternary 1x1 Sram compare with STI,PTI,NTI and different technology 62nm,32nm ,In Section 8 conclusion we discuss the how best the ternary 1x1 Sram performance like power consumption and access time compare to CMOS technology [8].

2.   DESIGN OF 2-BIT HARDWARE OPTIMIZED TERNARY

An ALU is one of the main components inside central processing unit (CPU) of a digital computer, and even it is found inside the simplest microprocessors also, where it is responsible for performing arithmetic and logic operations. The increasing demand for highly optimized modern information processing system clearly points to the need of efficient implementation of ALU in terms of power, speed and hardware. Design of Ternary Logic Gates Ternary logic is a type of multi-valued logic, which adds a third value to the conventional binary logic. Table 1 shows the definition of ternary logic states denoted by 0, 1 and 2 and their equivalent voltage levels. An n-variable ternary function f (a1, a2…an) is a logic function which is mapped on {0, 1, 2} n to {0, 1, 2}. The basic ternary operations (AND, OR and NOT) are defined as follows. Architecture of 2-bit HO-TALU a shown in Figure 1.

$$a_1, a_2, a_3 \dots \dots \dots a_n = \min (a_1, a_2, a_3 \dots \dots \dots a_n)$$

$$a_1 + a_2 + a_3 \dots \dots \dots a_n = \min (a_1, a_2, a_3 \dots \dots \dots a_n)$$

Table 1. Definition of logic states in ternary logic

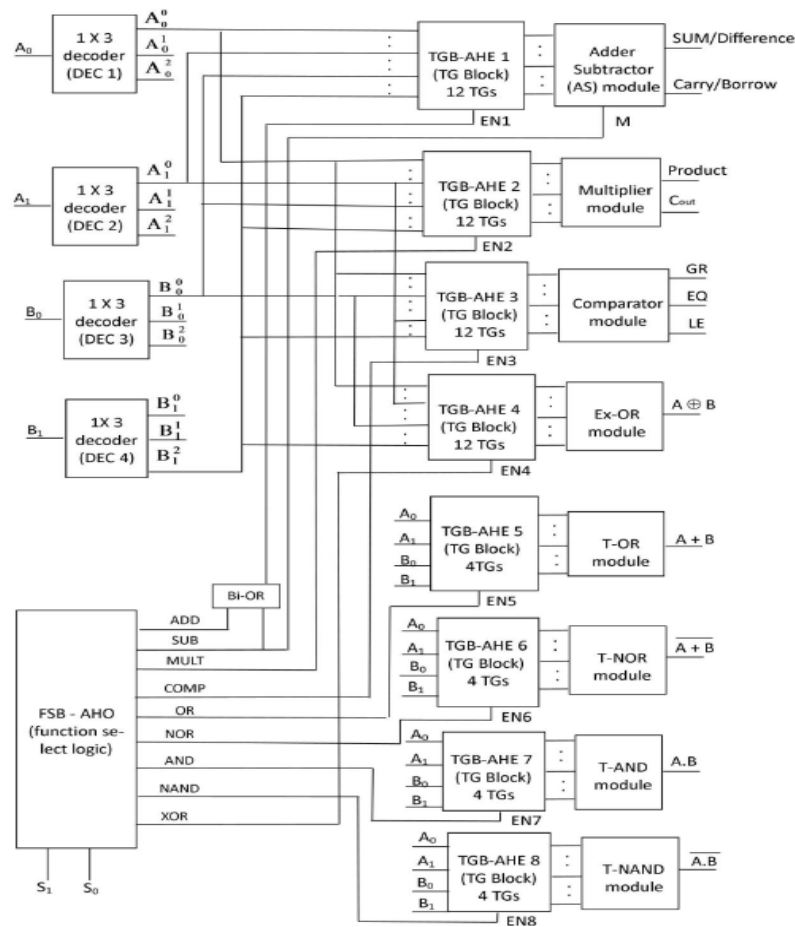| Logic state	Voltage level
0	0
1	0.45 (Vdd/2)
2	0.9 (Vdd)

Figure 1. Architecture of 2-bit HO-TALU

1-to-3-line Ternary Decoder
Figure 1 shows logic diagram of 1-to-3-line ternary decoder and its truth table. It is a one-input, three-output combinational circuit that generates three unary functions for an input 'a' as a0, a1 and a2. This design uses NTI to produce a0, PTI followed by a binary inverter to generate a2, and a binary NOR gate having inputs a0 and a2 to produce a1.

Ternary Logic and Building Blocks
Ternary logic functions are those functions that have significance if a third value is introduced to the binary logic. In this paper, 0, 1/2, and 1 denote the ternary values to represent false, undefined, and true, respectively. The three types of inverters that are.
a.   Simple Ternary Inverter (STI)
        The first type of ternary inverter is the simple ternary inverter (STI). For the inputs {0, 1/2, 1} it yields the output {1, 1/2, 0}. Because of its ability to produce {1/2} at the output, STI is used as the primary building block for the ternary 1x1 SRAM, A high resistance transmission gate is connected between the output of a low-resistance threshold modified binary inverter and 1/2Vs to produce the middle level voltage. The Simple Ternary Inverter is made by combining a binary CMOS inverter with a transmission gate [9]. The threshold voltages of the transistors in CMOS inverter. The inverter works as a simple inverter when the input is 0V or 1V. But when the input is 1V, the transistorsQ1 and Q2 goes in cut off region and the transmission gate aids in pulling up the control signal(whose value is equal to the half of supply voltage), to the output when the inverter is in cut off region. A circuit representation of simple ternary inverter a shown in Figure 2.
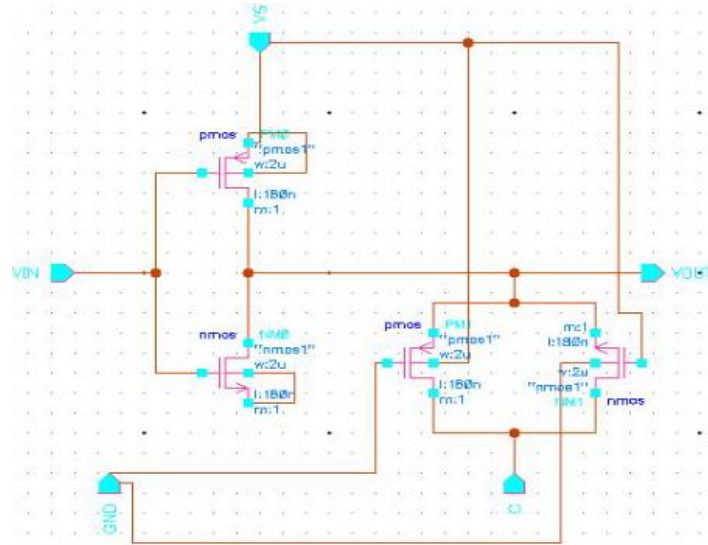
Figure 2. A circuit representation of simple ternary inverter

b.   Negative Ternary Inverter (NTI)
        The Negative Ternary Inverter (NTI) For the input of {0, 1/2, 1}, NTI provides the output {0, 0, 1}. An always on transistor (NMOS for NTI) is used for the passing the middle voltage instead of a transmission gate as its gate is tied to the positive power supply to keep it constantly ON. It behaves as a normal inverter when the input voltage i.e. Vin is equal to 0V and 1V, but when the value of Vin is equal to 1/2V, the transistors Q1 and Q2 goes in cut off region and the transmission gate aids in pulling up the control signal C (whose value is equal to 0Volts), to the output when the inverter is in cut off region. Therefore when the value of Vin is 1/2Volt the output of NTI is 0Volt. A circuit representation of negative ternary inverter a shown in Figure 3.
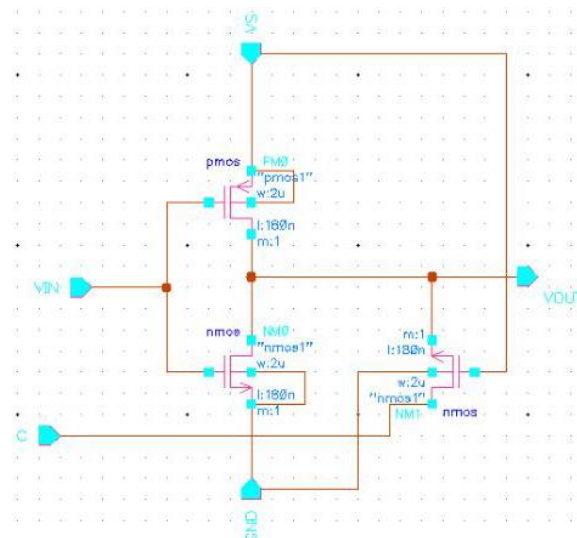

Figure 3. A circuit representation of negative ternary inverter

c.   Positive Ternary Inverter (PTI)
        The Positive Ternary Inverter for the input {0, 1/2, 1} provides {1, 1, 0} for output of PTI. In PTI, an additional always on transistor (PMOS for PTI) is used to pass middle voltage. PMOS transistor is connected to the output of CMOS inverter and its gate is tied to the ground, to keep it constantly turned ON. It behaves as a normal inverter when the input voltage i.e. Vin is equal to 0V and 1V, but when the value

of Vin is equal to 1/2V, the transistors Q1 and Q2 goes in cut off region and the transmission gate aids in pulling up the control signal C, to the output when the inverter is in Cut off region. Therefore when the value of Vin is 1/2Volt the output of PTI is 1 Volts. A circuit representation of positive ternary inverter a shown in Figure 4.

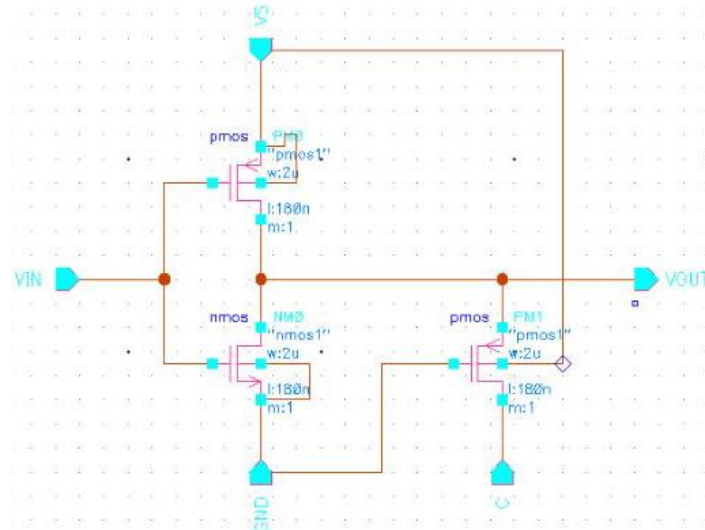Figure 4. A circuit representation of positive ternary inverter

2.1. Ternary sram array module

Array, which consists of Ternary SRAM cell, Tritline conditioning (TC) circuit, Row Decoder (RD), Column Decoder (CD) and Read/write Buffers, Sense amplifier circuit Ternary SRAM cell is precharged by TC with clock input. The word lines and Tritlines of Ternary SRAM cell are selected by Read Decoder and Column Decoder respectively with Address lines (A0-Ak-1) as inputs. Write/Read Buffers are used Write data into the cell and Read data from cell respectively. Block Diagram of Ternary SRAM Array a shown in Figure 5.
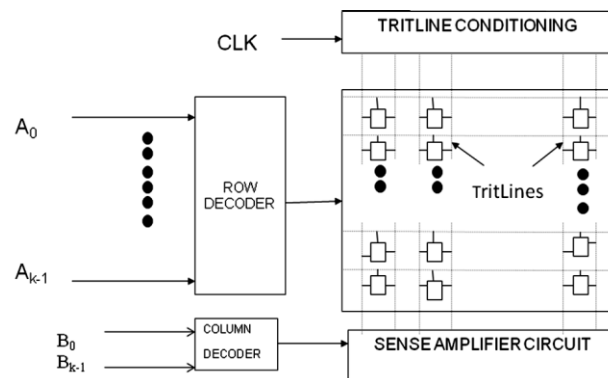

Figure 5. Block diagram of ternary SRAM array

2.2. TRITLINE CONDITIONING CIRCUIT

The Tritline conditioning circuitry is used top recharge the tritlines high before READ/WRITE operation. A tritline conditioner consists of pair of PMOS transistors. Schematic view of tritline conditioning a shown in Figure 6.
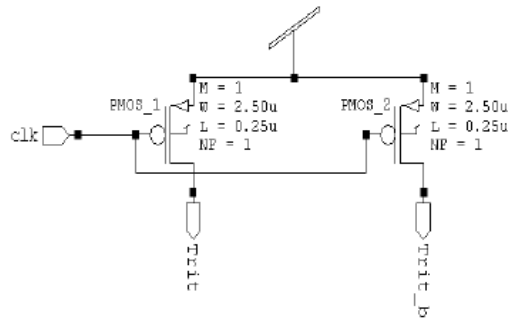
Figure 6. Schematic view of tritline conditioning

2.3. Read sensing circuit

Read sensing circuits are also called as sense amplifiers, which provide faster sensing by applying a small voltage swing. Ternary Read sensing circuit is activated consumes power in the circuit. When Read-enable line input is high, the transistor is active and when Read-enable line input is low, it effectively turns ON the cross-coupled inverter transistor pair, which pulls the output to the data and other complement through inverter. Schematic view of Ternary Read Sense amplifier as shown in Figure 7.
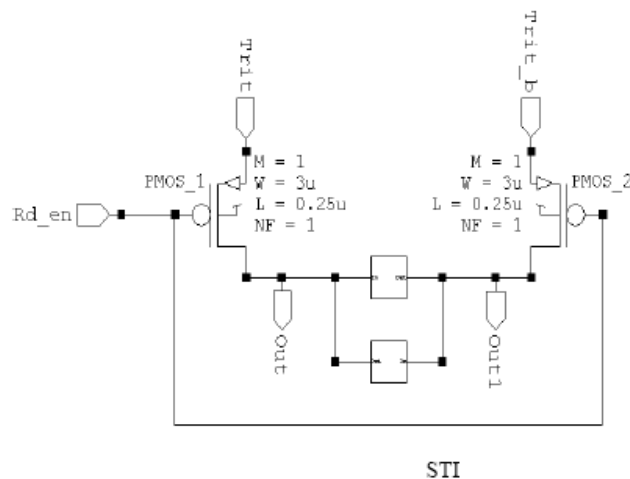

Figure 7. Schematic view of ternary read sense amplifier

2.4. Write driver circuit

To write to the cell, TRIT Lines must be driven to the desired value while WORD line is asserted to force the stored data to the value of TRIT. The value which is to be stored in SRAM must be given to the TRIT Lines and WORD Line must be asserted in order to keep access transistors ON. In this case the value of TRIT Line passes through the access transistors to the first STI Inverter. If TRIT is 1, then the NMOS of first STI turns ON, which in turn makes the output of first STI low. As the output of first STI is connected to the input of second STI, it turns ON the PMOS of second STI which makes the output of second STI high. As the output of second STI is connected to the input of first STI, it again makes the output of first STI low and this is how the process goes on and both the STI support each other. If the value that is to be written in the SRAM is 0 or 1 then voltage applied to the TRIT Lines must be 0, ½, and 1 respectively. Schematic view of ternary write driver a shown in Figure 8.
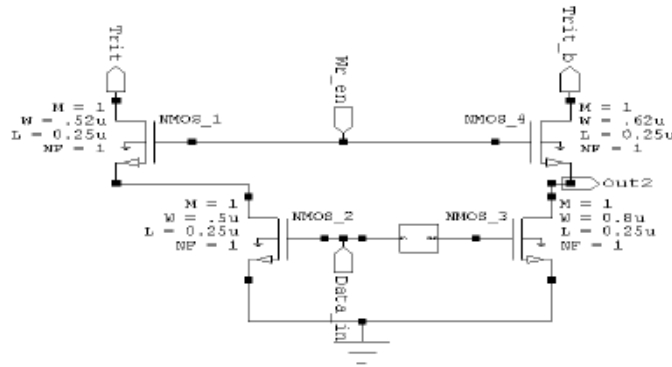
Figure 8. Schematic view of ternary write driver

2.5. Ternary 1x1 SRAM array:

The Ternary 1x1 SRAM memory array Proper design of peripheral and supporting I/O circuits (Precharge, Sense Amplifier, and Row/Column Decoder etc.) are important for proper functionality of the full system. To access a particular memory cell, all the supporting circuits' active participation is necessary. Figure 9 provides a block diagram of the ternary 1x1 Sram array. Here WC denotes write circuit, WE denotes write enable signal, SE is the sense enable signal for enabling the sense amplifier circuits with O1, as the outputs of the sense amplifier block. WL1, are the word lines. Address decoder selects a particular word line for accessing required cell array; the address decoding delay accounts for the maximum percentage of the memory access time in addition with the delay of the bit-line capacitances. Read/Write circuitry provides the interface between internal cells with external hardware facilitating accurate data transfer. Before every read operation precharge circuit is enabled by PE signal to precharge the complementary bit lines. For reading the stored data, SE signal is activated to detect the small voltage differences between BL and BL with the help of sense amplifier block. For write operation, that is to modify the data content of the cells, WE signal is activated and the data is given as an input to DATA. Schematic view of ternary 1x1 SRAM array a shown in Figure 10.
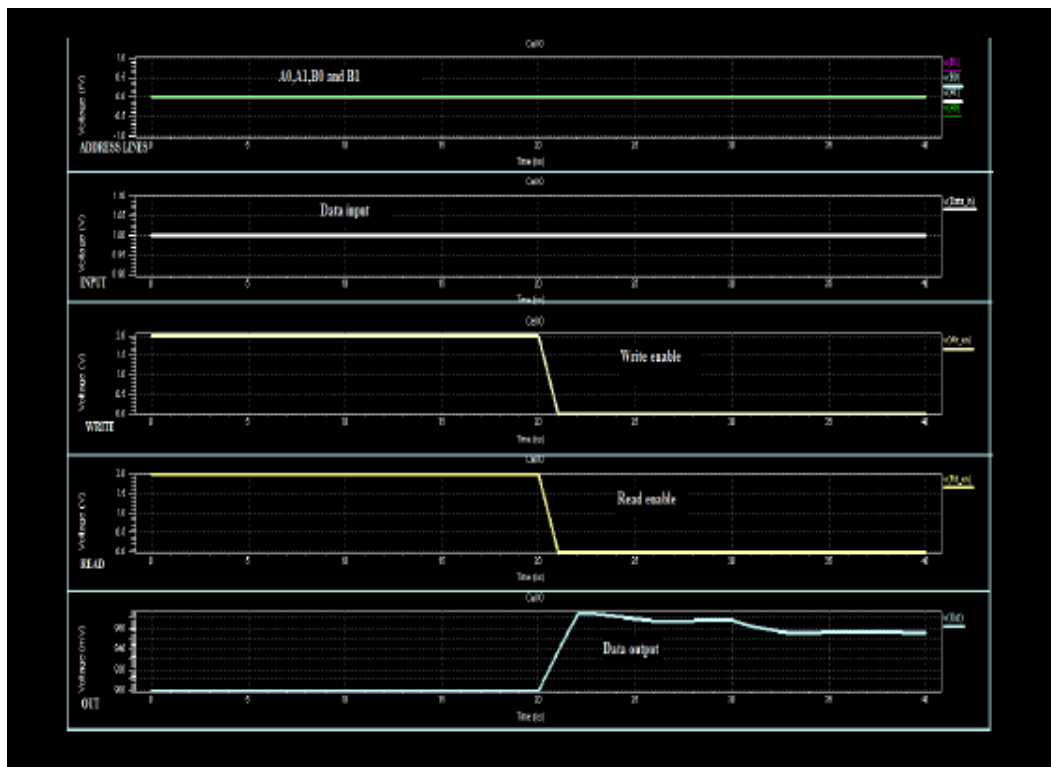

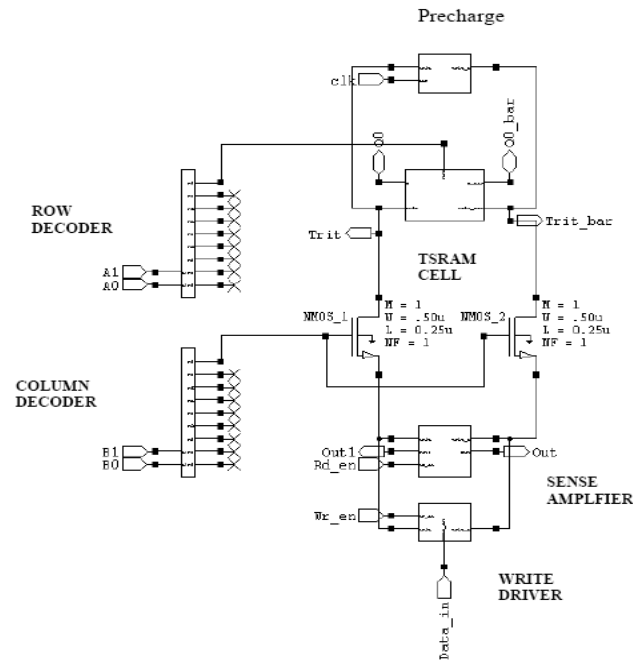Figure 9. Simulation result for logic (1/2)

Figure 10. Schematic view of ternary 1x1 SRAM array

CNFET Specifications
Physical channel length (L_channel)=32.0nm
The length of doped CNT source/drain extension region (L_sd)=32.0nm
Fermi level of the doped S/D tube (Efo)=0.6 eV
The thickness of high-k top gate dielectric material (Tox)=2.0nm
Chirality of tube (m, n)=(19, 0)
CNT Pitch=20nm
Flatband voltage for n-CNTFET and p-CNTFET (Vfbn and Vfbp)=0.0eV and 0.0eVThe mean free path in intrinsic CNT (Lceff)=200.0nm
The mean free path in p+/n+doped CNT=8.0nm
The work function of Source/Drain metal contact=4.6eV
CNT work function=4.5eVThe sizing of a CNFET is equivalent to adjusting the number of tubes. 6T-SRAM
-      M1, M3 --- 4 tubes
-      M2, M4 --- 2 tubes
-      M5, M6 --- 3 tubes

3.   SIMULATION RESULTS

The power dissipated by the memory cell is usually a significant part of the total chip power. Cell accessing consumes a significant fraction (30-60%) of total power dissipation in modern microprocessor. A large portion of cell energy is dissipated in driving the bit-lines, which are heavily loaded with multiple storage cells. Clearly, the memory cells are the most attractive targets for power reduction. In Ternary 1x1 SRAM array because one of three bit-lines must be discharged to low regardless of written value, the power consumption in writing 0, 1/2, 1 are the generally same. There are always transitions on bit lines in writing '0' and reading '1' and while accessing cell since an overwhelming majority of the write and read bits are 1 these cause high power consumption during read/write operation in ternary 1x1 SRAM cell [10]. For reading and writing 1, 1/2, 0, in Q, transistors which are ON are noted and the power dissipated by these transistors is calculated by multiplying voltage and current flowing through that corresponding transistors. Thus the power Dissipated by the transistors is measured. Simulation result for logic (0) a shown in Figure 11.
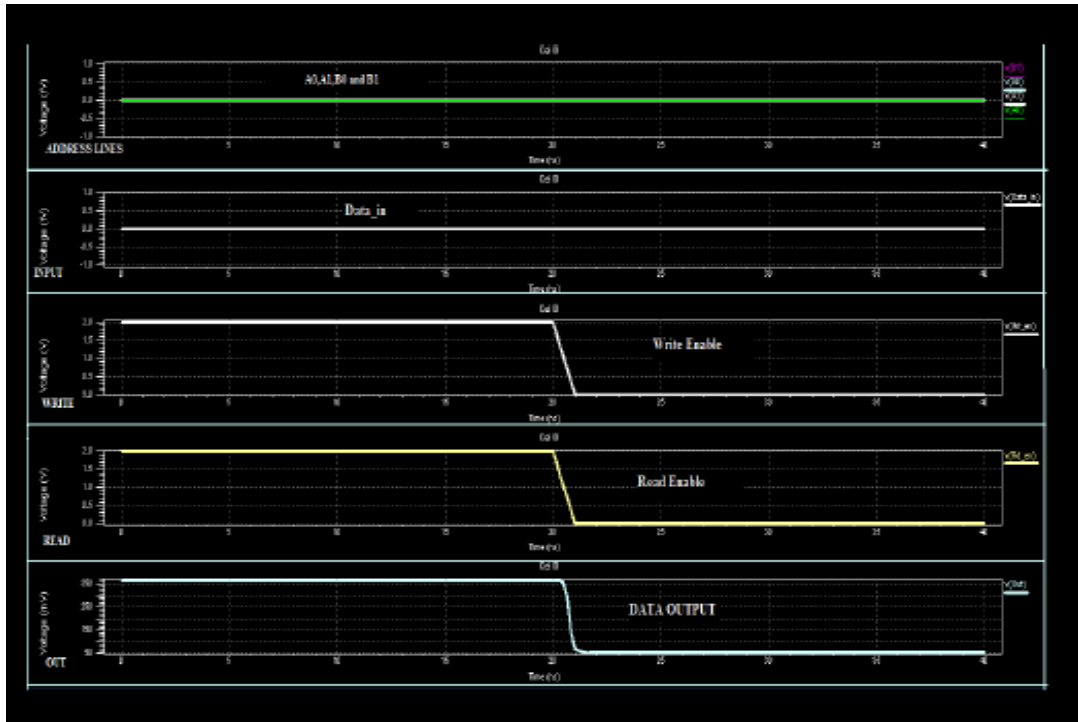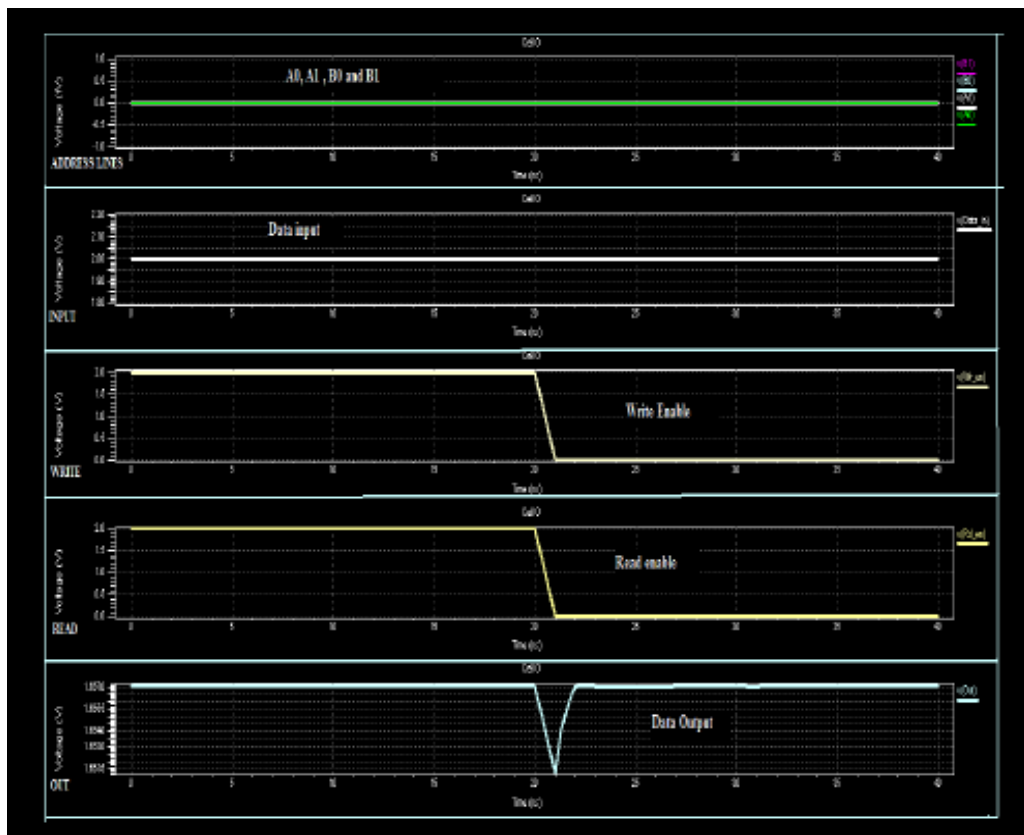
Figure 11. Simulation result for logic (0)

Figure 12. Simulation result for logic (1)

4. PERFORMANCE RESULTS

Table 2 shows the power results of compare 65nm with 32nm different ternary Inverters, It is evident from the Table 2, reduction in technology, results in low power consumption. In this paper, these ternary inverters are used for designing Ternary SRAM for low power applications. performance results of the 1X1Ternary SRAM Array. Power and Data access time is depicted in Table 3. Analysis result of ternary 1x1 memory A as shows in Figure 13.

Table 2. Power results of ternary inverters

S.NO	65nm	32nm
STI	0.02890mw	0.0139mw
PTI	0.0320mw	0.0210mw
ssNTI	0.0107mw	0.0099mw

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            ***** job concluded
******
**ternary  1x1 memory cell
 ****** transient analysis                tnom=  25.000 temp= 25.000

******
 propagation_delay= 5.23-09       targ= 3.0093E-08  trig= 2.0150E-08
 avgpower= 1.412-09     from= 1.0000E-09 to= 8.000E-08
 peakpower= 3.8326E-09      at= 5.0173E-08
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Figure 13. Analysis result of ternary 1x1 memory A

Table 3. Performance results of 1X1 ternary SRAM array

S.NO	65nm	32nm
Power dissipation	0.508mw	1.412mw
Access time	7.88ns	5.23ns

5. CONCLUSION

A Ternary 1x1 SRAM cell was designed using HSPICE and Tanner 32nm Technology. The Read and Write Operations are performed using Hspice. The proposed SRAM is designed using Ternary 1x1 Sram memory array. Based on the evaluation and comparison of the performance parameters of traditional 6T SRAM cells and peripheral circuits between predictable 32nm CNFET, clear superiority of the CNFETs can be observed. These results clearly justify that CNTFET is more suitable for circuit design rather than MOSFETs, The fast operation power consumption, access time less compared with the conventional 65nm technology. As a result of comparison it is found that ternary 1x1 sram uses less number of transistors, reduce in terms of the area, Power and increases the speed. Further enhancement of this work can be designing 8-bit ternary SRAM using CNTFET technology.

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