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A body bias technique for low power full adder using XOR gate and pseudo NMOS transistor

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ABSTRACT

Power dissipation is a major issue in digital circuit design. As technology into developed into range, power and delay becomes vital nanometer parameters to ameliorate the performance of the circuit. To minimize the power consumption many low power techniques such as MTCMOS, stacking, body biasing techniques have been reported. In this paper, a new pseudo NMOS adder circuits have presented. It has designed using transmission gate and body bias technique. Simulation has been accomplished by using SPICE tool. The simulation result show the validity of the proposed techniques is reduces power dissipation from 0.367 mW to 0.267 mW and PDP reduced from 19.311pJ to 13.311pJ. Overall improvement of 29% in power consumption and 30% in PDP has obtained.

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1. INTRODUCTION

In the present span, there is a constant advancement in VLSI technology which has caused fast decrease in size and geometries of the transistors and rise in densities of the transistor [1]. Due to this, the circuit consumes huge amount of power and many times it results to silicon failure in chips. High speed operation with low power utilization is becoming a momentous factor in the modern design of various electronics components [2]. The adder is the most critical component that's extensively used in portable devices i.e. cellular phones, remote sensors, wearable electronics and devices where very low power consumption is needed. Adder has used in the many computational power efficient circuits [3]. The body biasing is a power reduction technique used in many VLSI circuits. The equation which shows how body bias effects the threshold voltage is:

$$V_{th}=V_{th0}+\gamma[(2\phi_B-V_{SB})^{1/2}-(2\phi_B)^{1/2}] \quad (1)$$

Where Φ_B Fermi Potential
γ body effect coefficient
V_{th0} Threshold voltage with zero V_{SB} substrate bias
V_{SB} source to body bias voltage

The leakage current is the sources of power consumption in the sub threshold circuits; this increase the threshold voltage significantly decreases the sub threshold leakage current. In order to maintain the low threshold voltage (V_{th}) in the static CMOS parameters, the body terminals of PMOS has connected to V_{DD} and the NMOS body terminal connected to ground. A PMOS transistor are used as a load device and NMOS used as pseudo-NMOS logic. The merit of pseudo-NMOS logic are its high speed (large fan-in NOR gates)

and low transistor count [4]. The disadvantage is the static power consumption of the pull-up transistor as well as the reduced output voltage and voltage gain, which makes the gate more liable to noise.
In this paper we have proposed a schematic approach to design full adder and this adder are useful in large circuits such as multipliers. In recent year's different circuit technique have been described to improve the performance of XOR/XNOR gates, static CMOS transistor mainly contains pull-up PMOS and pull-down NMOS networks [5].

In this paper, a XOR circuit has designed using pseudo NMOS, this technique reduce power consumption and number of transistors. Adder has designed with XOR circuit and multiplexer. This proposed circuit has reduced supply voltage, less the power and small time delay reduction using sub threshold and different body biasing techniques [6]. Transmission gate have been also used in designing of carry block of proposed adder circuit. Four different circuits have been proposed in this to implement the full adder. Rest of paper organized as: Section II describes the proposed adder circuit, section III discusses simulation result about of the proposed adder, finally section VI conclude the above.

2. PROPOSED ADDER CIRCUIT

In circuit I, a full adder has been designed using XOR gates with the multiplexer block. XOR gate has designed using pseudo NMOS whereas multiplexer has designed using transmission gates. In circuit II, full adder has been designed using same circuit as circuit I with body biasing of PMOS substrate with V_{DD} and NMOS substrate with V_{SS}=GND. Supply voltage V_{DD} had taken between 0.8 to 1.6V. Multiplexer has designed using one transmission gate; it reduced number of the transistors [7-9]. When the body of NMOS has biased with negative supply the channel region increase therefore rises in the threshold voltage. Full adder using XOR and MUX circuit a shown in Figure 1. Body connections in MOS devices a shown in Figure 2.

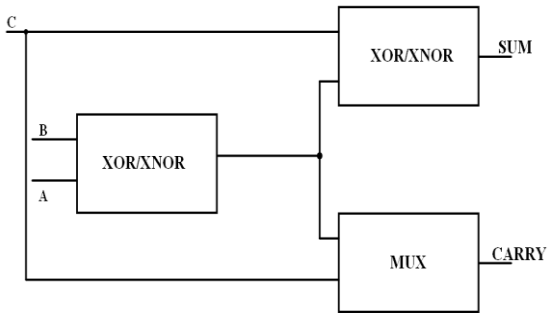

Figure 1. Full adder using XOR and MUX circuit

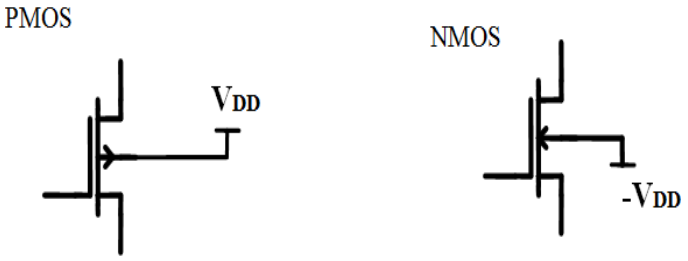

Figure 2. Body connections in MOS devices

In circuit III, full adder has designed using circuits I and II with voltage V_{SS}=-V_{DD} or V_{SS}<0 had taken. In it, width of transistor sized for proper output voltage swing. In Dual threshold CMOS technique, PMOS transistors are biased individually by their inputs so that each transistor have a high or low sub threshold voltage hence, low or high sub threshold leakage current, not dependent on gate's status [10]. In PMOS body biasing technique, all PMOS transistors are connected to the gate output. When PMOS network had OFF then gate output had less rise to sub threshold leakage current. When PMOS transistor is switches ON then its body had already biased low and instantaneous high leakage current has flow caused

the gate to switch faster and the output raise faster which has suppressed the sub threshold leakage current afterwards but only after that current has not required. In proposed technique, PMOS body biasing has done to gate output and NMOS body biasing to a voltage supply V_{SS} (V_{SS}<0.40V). Figure 3 a shown in (a) DTPMOS technique (b) PMOS body biasing technique (c) The proposed technique. Shown in Adder using XOR and multiplexer (Circuit-I) a shown in. Adder using body biasing technique with NMOS substrate connected to ground (Circuit-II) a shown in Figure 5. Adder using body biasing and DTPMOS techniques (Circuit-IV) shown in Figure 7. Adder using body biasing with NMOS substrate connected to Vss (Circuit-III) a shown in Figure 6.

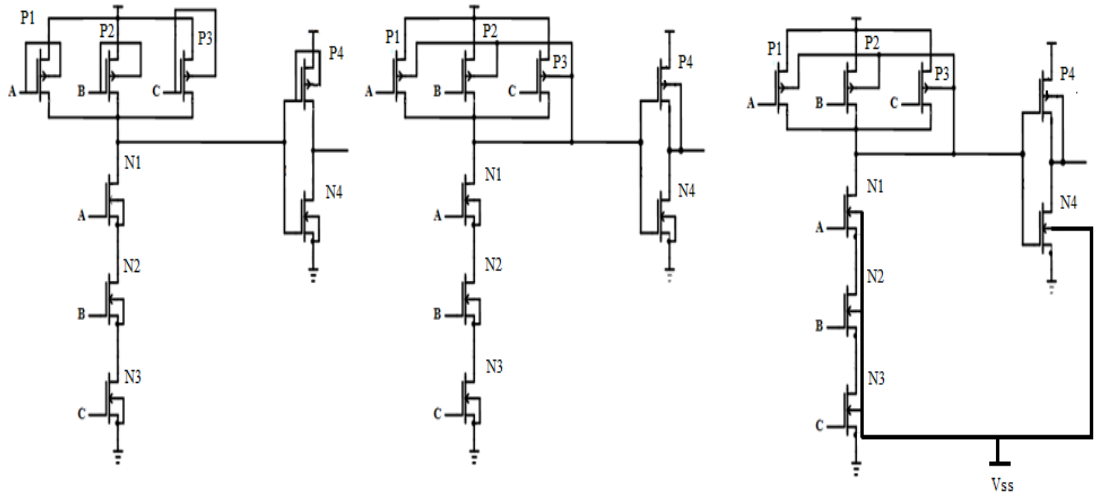

Figure 3. (a) DTPMOS technique (b) PMOS body biasing technique (c) The proposed technique

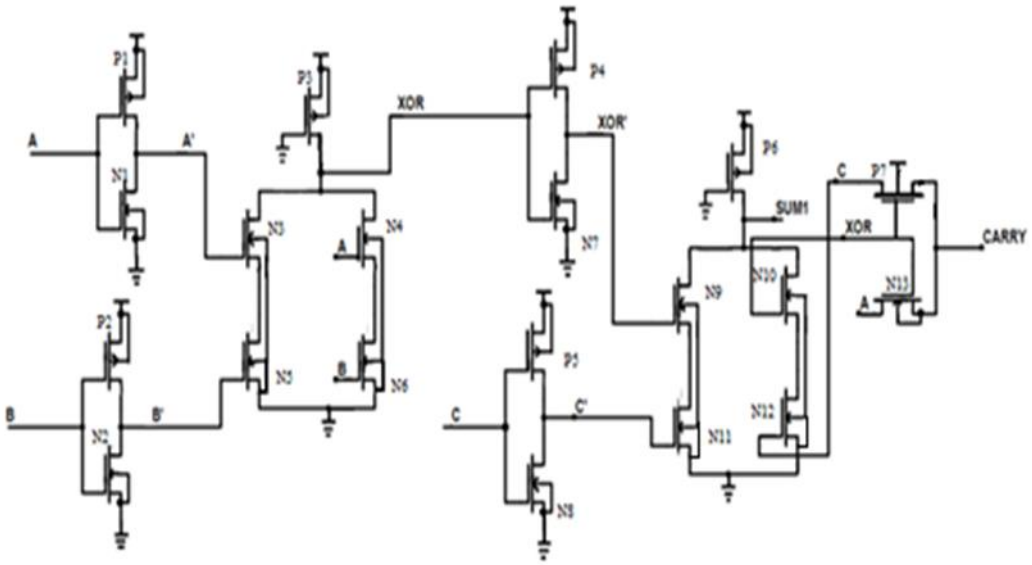

Figure 4. Adder using XOR and multiplexer (Circuit-I)

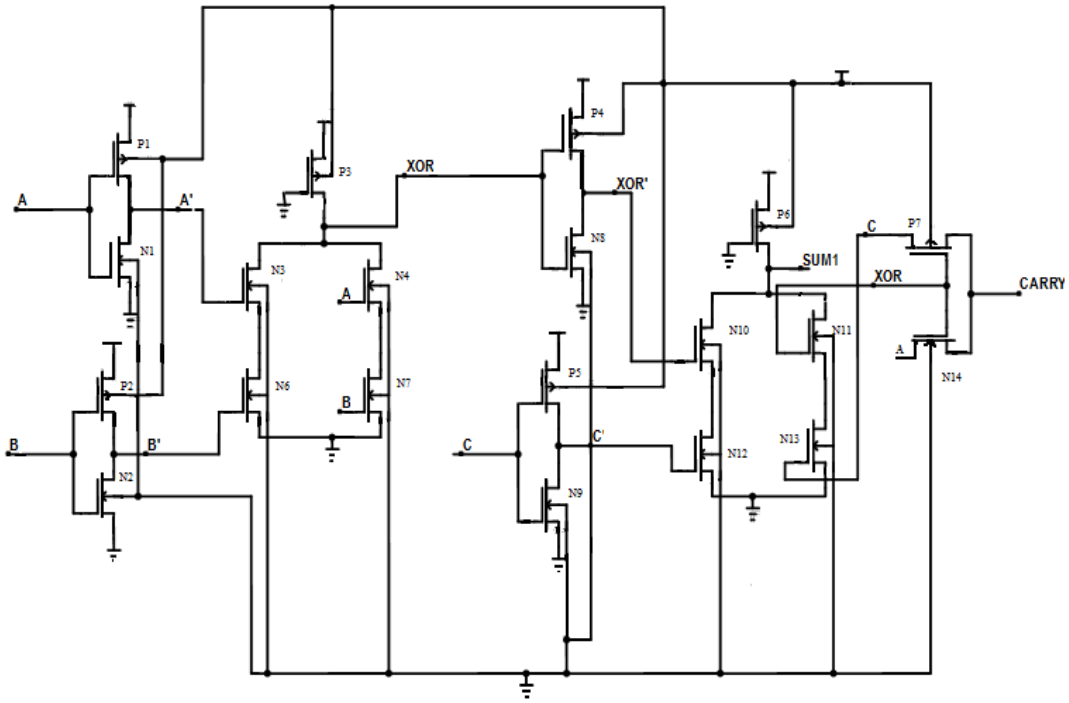

Figure 5. Adder using body biasing technique with NMOS substrate connected to ground (Circuit-II)

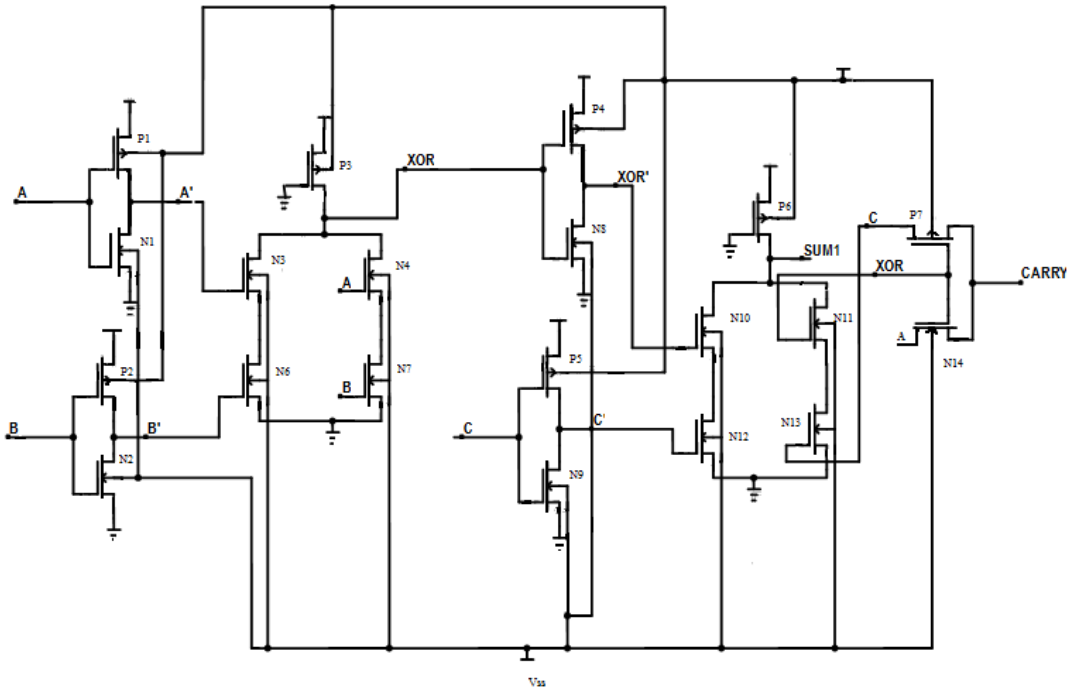

Figure 6. Adder using body biasing with NMOS substrate connected to Vss (Circuit-III)

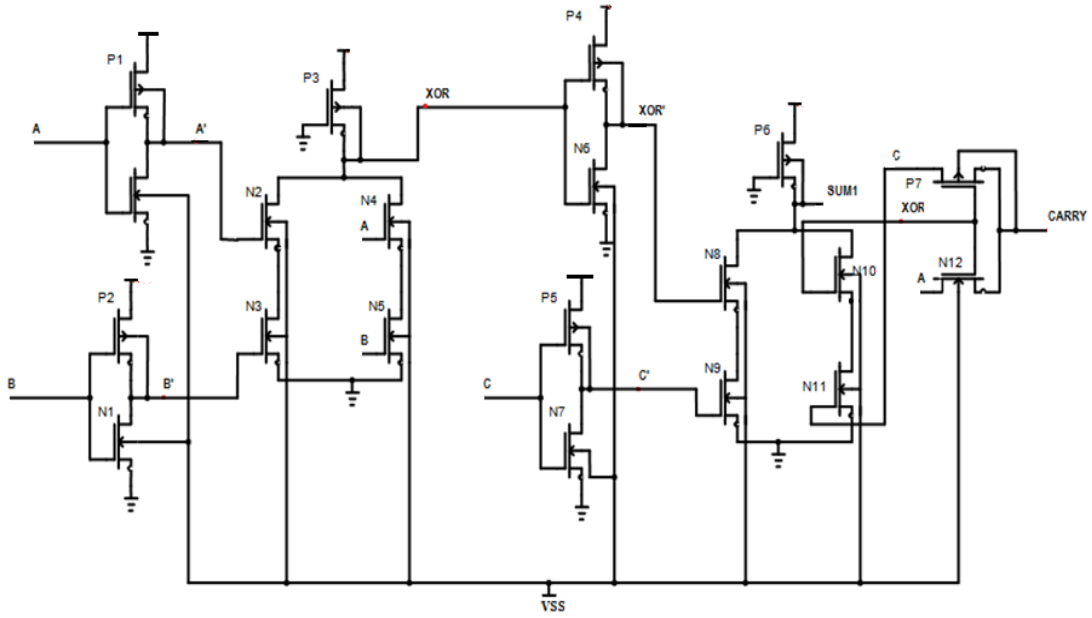

Figure 7. Adder using body biasing and DTPMOS techniques (Circuit-IV)

3. RESULTS AND DISCUSSION

The simulations are performed in SPICE 180nm technology with supply voltage variation from [0.8-1.6]V. Substrate biasing has been used to control the leakage current and power consumption. With help of pseudo NMOS and transmission gates number of transistors and dynamic power dissipation had reduced. It has been observed that by using proposed body bias and DTPMOS techniques more than 29% saving in power and more than 1.5% savings in delay are achieved. To evaluate the performance of the proposed body bias scheme, the implemented full adder is simulated at different supply voltages (V_{DD}) from 0.8V to 1.6V and the performance parameters power, delay, PDP are compared. From the comparisons made it is observed that: Also the magnitude of percentage decrease in power is more with the increase in V_{DD}. Particularly delay of operation (V_{DD}=0.8V) the proposed scheme incurred a penalty of 0.8% increase in delay because of less output driving capability due to the increase in threshold voltage of the device. The proposed full adder circuit has achieved more than 30% power delay product saving than the standard CMOS configuration at the different supply voltage V_{DD} from 0.8V to 1.6V. Power dissipation and time delay with variation in VDD as shown in Table 1.

Table 1. Power dissipation and time delay with variation in VDD

VDD (V)	Adder with NMOS substrate to GND			Adder with NMOS substrate to V_{SS}			Adder with NMOS substrate to Vss and PMOS Substrate to output		
	Power (mW)	Time Delay (ns)	PDP (pJ)	Power (mW)	Time delay(ns)	PDP(pJ)	Power (mW)	Time Delay(ns)	PDP (pJ)
0.8	0.045	50.670	2.280	0.034	50.957	1.732	0.027	51.090	1.379
0.9	0.088	50.703	4.461	0.044	50.632	2.227	0.038	50.938	1.935
1	0.146	50.715	7.404	0.088	50.645	4.456	0.073	50.691	3.700
1.1	0.222	50.634	11.240	0.204	50.650	10.331	0.120	50.654	6.078
1.2	0.316	50.612	15.993	0.305	50.643	15.446	0.181	50.642	9.166
1.3	0.430	50.789	21.839	0.419	50.634	21.215	0.265	50.629	13.416
1.4	0.564	50.648	28.565	0.553	50.621	27.993	0.382	50.612	19.333
1.5	0.720	50.637	36.458	0.708	50.596	35.821	0.532	50.603	26.920
1.6	0.898	50.737	45.561	0.884	50.598	44.728	0.790	50.040	39.531

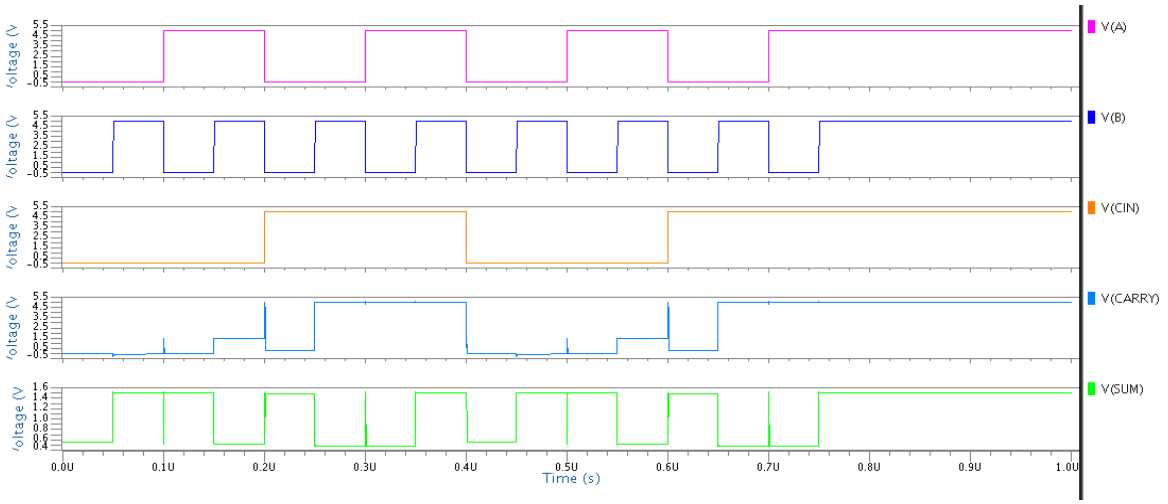

Figure 8. Output waveform for carry and adder in proposed full adder circuit

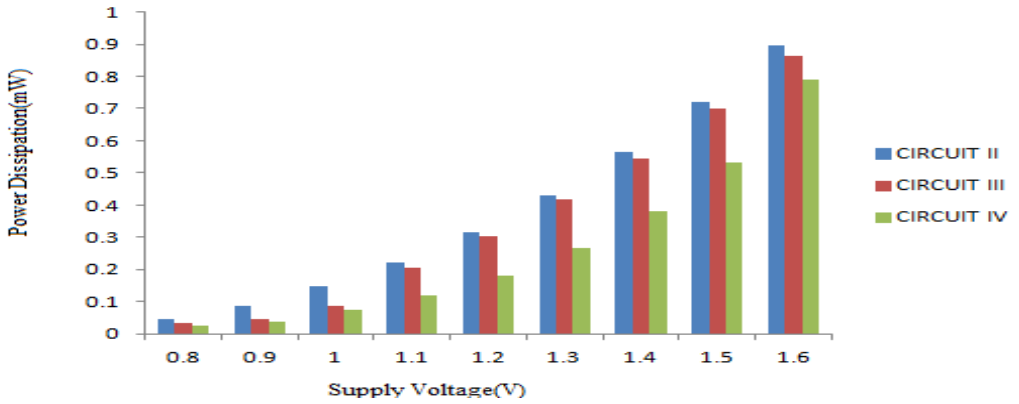

Figure 9. Graphical representation of power versus supply voltage V_{DD}

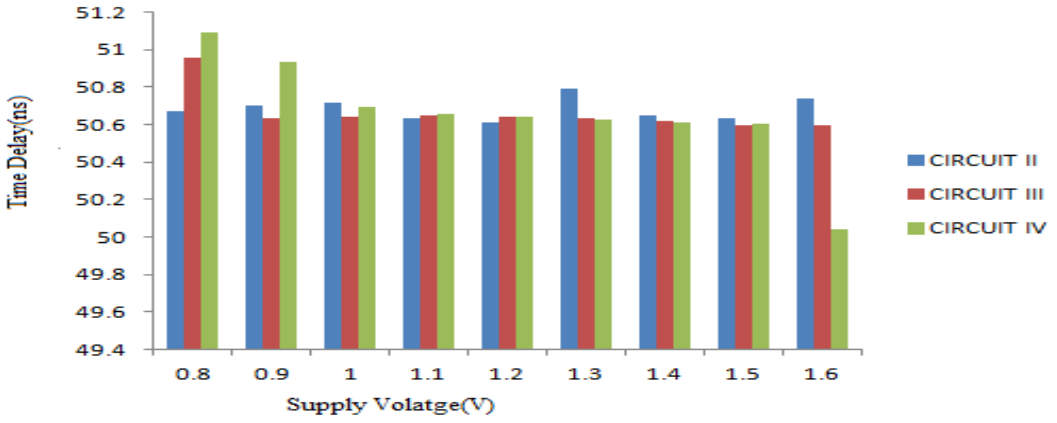

Figure 10. Graphical representation of time delay versus supply voltage V_{DD}

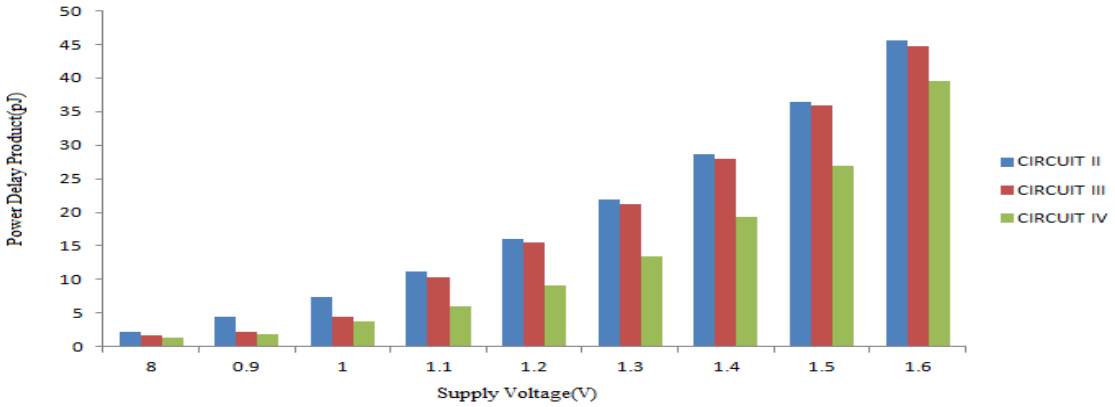

Figure 11. Graphical representation of power delay product versus supply voltage V_{DD}

4. CONCLUSION

The full adder circuits using XOR and multiplexer block using body bias and DTPMOS technique have been proposed. Power and PDP is reduced to greater extent than existing method. The simulations are performed in SPICE 180nm technology. The simulation results show that the proposed adder circuit offers improved average power and average delay such as 0.267 mW and 50.601 ns. The circuit operates with more speed after applying biasing and DTPMOS technique. The proposed full adder circuit show less power consumption and PDP with reduced number of transistors. The adder designed shows minimum power dissipation of 0.267mW with PDP of 13.495 pJ at different supply voltage from V_{DD} =0.8V to 1.6V.

REFERENCES

[1] M.Manoranjani and T.Ravi, "Multi-threshold CMOS Sleep Stack And Logic Stack Technique For Digital Circuit Design", *ARPN Journal of Engineering and Applied Sciences*, vol.10, 10 June 2015

[2] Shashank Gautam, "Designing of Full Adder Using Low Power Technique" ,*International Journal of Computer, Electrical, Automation, Control and Information Engineering* , vol.9(4), 2015

[3] Ms. Namrata V. Bhadade, Prof. Amol K. Boke, "Design And Analyze High Speed, Power Efficient Full Adder Using Digital Logic Technique", *International Journal Of Advanced Information And Communication Technology* , vol.1(7), November 2014

[4] Manoj Kumar, Sandeep K. Arya, Sujata Pandey , "Low Power CMOS Full Adder Design With Body Biasing Approach", *Journal Integrated Circuits & Systems* , vol.6(1), pp. 75-80 ,2011

[5] Suman Nehra and P. K. Ghosh, "Design of a Low Power XNOR gate Using MTCMOS Technique", Advance in Electronic and Electric Engineering, ISSN 2231-1297, vol.3(6) , pp. 701-710 , 2013

[6] Kishore Sanapala and R. Sakthivel, "Low Power Realization Of Sub Threshold Digital Logic Circuits Using Body Bias Technique" , *Indian Journal of Science and Technology* , vol.9(5), February 2016

[7] Basil George and Nikhil Soni, "Design And Analysis Of Low Power 10 Transistor Full Adders Using Novel XNOR Gates", *International Journal Of Advanced Information And Communication Technolog* , vol.2(7), November 2012

[8] Manoj Kumar, Sandeep K. Arya and Sujata Pandey, "Single Bit Full Adder Design Using 8 Transistors With Novel 3 Transistors XNOR Gate",*International Journal of VLSI design & communication system* ,vol.2(4) , December 2011

[9] D.Khalandar Bashaa *et al*,"Gated Body-Biased Full Adder", *ARPN Journal of Engineering and Applied Sciences*, vol.3(7),2016

[10] Walid Elgharbawy *et al*," A new level Body Biasing Technique For PMOS Transistor In Sub-threshold CMOS Circuits", *Institute of Electrical and Electronics Engineers*, vol.05 (0-7803-8834-8), 2005