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Designing ALU using GDI method

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ABSTRACT

As CMOS technology is continuously becoming smaller and smaller in nanoscale regimes, and circuit resistance to changes in the process for the design of the circuit is a major obstacle. Storage elements such as memory and flip-flops are particularly vulnerable to the change process. Power consumption is also another challenge in today's Digital IC Design. In modern processors, there are a large number of transistors, more than a billion transistors, which increases the temperature and the breakdown of its performance. Therefore, circuit design with low power consumption is a critical need for integrated circuits today. In this study, we deal with GDI techniques for designing logic and arithmetic circuits. We show that this logic in addition to low power consumption has little complexity so that arithmetic and logic circuits can be implemented with fewer transistors. Various circuits such as adders, differentiation and multiplexers, etc. have been designed and implemented using these techniques, and published in various articles. In this study, we review and evaluate the advantages and disadvantages of these circuits.

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1. INTRODUCTION

Advances in low power consumption and high speed of embedded systems such as mobile phones, laptops and so on have made VLSI technology become smaller and smaller at the nanoscale, so that many functions can be implemented on a chip [1]. Previously, CMOS, TG, and PTL technologies were used to implement functions and logic circuits, but nowadays a new technique called infiltrators gate or GDI has solved problems of power consumption, speed, number of transistors and so on [1]. GDI technique is a low-power designing technique. This technique is very similar to CMOS technology, but with its help complex functions with fewer transistors compared with CMOS technology can be implemented. This method enables us to design circuits with high speed, low power consumption and fewer transistors. In this chapter, we review the research done in this regard, and circuits designed with this new technique.

Increase in the speed and reduction in power consumption in digital integrated circuits has always been considered as a main objective, so that in recent years, extensive research has been done in this area. With the advancement of technology and reduction in the size of chips, the chip power density (power per unit area) has increased significantly. Due to the high cost of using cooling on the chips, the importance of reducing power consumption in digital integrated circuits is determined.

With the rapid advancement in manufacturing technology of semiconductor devices, chip density and speed have increased. Controlling consumed power in portable devices is a fundamental issue. High power consumption reduces battery life on these devices. Reduction of power losses is important even for the non-portable device because increasing losses increases packaging density and the cost of cooling.

Portable electronic devices due to the complexity of the structure contain more than one VLSI chip. Most of the losses in a portable electronic device includes non-digital components. Effective techniques for reducing power losses in such systems that are related to the discontinuation or reduction of leakage components is called dynamic power management. In the old systems, several dynamic power management schemes may be used, integrating which is difficult and may need to be repeat many of the projects and debugging. IC power loss has different components and depends on the type of circuit performance. First, switching or dynamic power component becomes dominant during active mode operation. Secondly, there are two initial sources of the leakage: active leakage and standby leakage mode. Standby leakage may become smaller than active leakage by changing body bias may or intermittent outages. Reducing the supply voltage (VDD) is perhaps the most effective way of saving power due to square dependence of active power of digital circuit to voltage source. Unfortunately, reducing VDD reduces device speed because gate starter voltage decreases VGS VT. To deal with this problem, an optimization is performed on VDD and the least reduced VDD is used to meet the speed need of orbital velocity. Reduction in the voltage source, in any technology production, helps reduce power losses in dynamic CMOS logic circuits. Reduction in voltage supply increases the delay of gates unless the threshold voltage of transistors reduces that increases leakage of the transistor. Thus, VDD reduction reduces dynamic power dissipation, but increases the static power dissipation.

Therefore, there is a clear reconciliation between off-state leakage (static power) and active power (dynamic power), for specific applications, that result in the careful selection of VT and VDD. Device integration leads to a combination of many functions on a single chip, so the understanding the optimum and applicable point of VT and VDD for all circuit blocks on a chip are hard and difficult. As a result, designing techniques can change with circuit blocks.

As CMOS technology is continuously becoming smaller and smaller in nanoscale regimes, and circuit resistance to changes in the process for the design of the circuit is a major obstacle. Storage elements such as memory and flip-flops are particularly vulnerable to the change process. Power consumption is also another challenge in today's Digital IC Design. In modern processors, there are a large number of transistors, more than a billion transistors, which increases the temperature and the breakdown of its performance. Therefore, circuit design with low power consumption is a critical need for integrated circuits today. In this study, we deal with GDI techniques for designing logic and arithmetic circuits. We show that this logic in addition to low power consumption has little complexity so that arithmetic and logic circuits can be implemented with fewer transistors. Various circuits such as adders, differentiation and multiplexers, etc. have been designed and implemented using these techniques, and published in various articles.

2. MATERIALS AND METHODS

2.1. GDI techniques

GDI technique is based on using a simple cell as shown in Figure 1. At first glance, this basic cell is the same as a CMOS inverter, but there are differences between them:

- A GDI base cell has four entries that include a G input (common gate of PMOS and NMOS transistors), P input (PMOS source), N input (NMOS source) input and D input (the common drain of NMOS and PMOS).
- The bodies of both PMOS and NMOS transistors are connected to P and N respectively. In this structure, N, P and D may be used both as input and as output due to the circuit structure. It should be noted that there is no possibility of the realization of this issue in the process of single standard wells. However, it can be implemented in technologies such as twin holes, CMOS or SOI. Table 1 shows how a simple change in combination of inputs of a stem cell GDI gets corresponding outputs with different Boolean functions. As is specified in Table 1, we can see that by using these two simple transistors, one can implement complex functions such as Maltese multiplexer. In GDI implementations, using fewer gates is one of the most important design characteristics, which, in turn, will have fewer transistors and less power waste compared to designing standard with CMOS and PTL techniques. Further implementation of these functions in various techniques requires the use of 6 to 12 transistors, but the use of GDI technique allows us to do the intended design based on using fewer transistors and this brings about power dissipation, speed up, and reduction of complexity of Boolean functions. Moreover, multi-input gates can be implemented by combining several GDI cells.

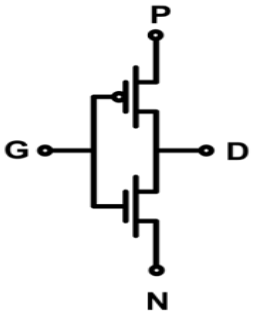

Figure 1. Base cells of GDI

Table 1. Making some logic functions with GDI cells

Logic functions	D	G	P	N
F1	$\overline{A}B$	A	B	'0'
F2	$\overline{A}+B$	A	'1'	B
OR	A+B	A	B	'1'
AND	AB	A	'0'	B
MUX	$\overline{A}B+AC$	A	B	C
NOT	$\overline{A}$	A	'1'	'0'

2.2. Designing ALU with GDI technique

Examples of GDI functions presented in Table 1 are only the development of single-input CMOS inverter structure to a three-input GDI cell so that the implementation of complete logic functions can be realized with minimum transistors. In fact, this method can be defined into a more complete and more general form. Extension of CMOS structure with n input to GDI cell of n+2 input can be realized by creation of a p input instead of V_{DD} power supply in PMOS block of a CMOS structure and an N input instead of V_{SS} in NMO as shown in Figure 2. The generalization can be expressed by:

$$Out=\overline{F}(x_1..x_n)P+F(x_1..x_n)N \quad (1)$$

Now, development of various logic gates by using GDI technique is presented here. For comparison of the gates in CMOS technology or transfer gate or TG, and transfer gate NMOS or N-PG is implemented. These gates have been designed with minimum transistors possible. Table 2 compares comparison circuit designed with GDI technique to circuit implemented with CMOS techniques.

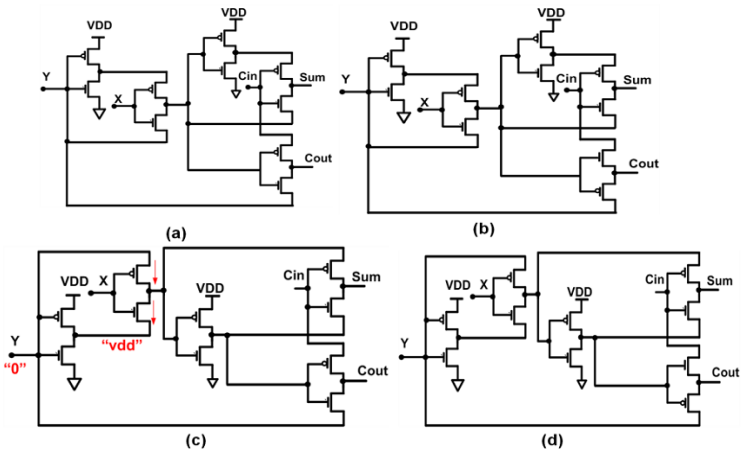

Figure 2. Implementation of adder circuit with GDI technique

Table 2. Comparison between GDI and CMOS stamdard

Designing technique	Power(pW)	PDF	The number of transistors
GDI	108/5	137/8	16
CMOS	282.4	254.16	36

3. RESULTS

3.1. Designing dynamic logic circuit

High-speed circuit structure (HS0) is shown in Figure 3. This circuit includes a reset transistor NMOS (M2) and the pull-up transistor PMOS (M1). M1 and M2 Transistors are controlled by the clock signals. The base of function of this circuit is that in the period when the clock is equal to 1, the output node is connected to earth by M2. When the clock is equal to zero, M2 is off and M1 guides. Depending on the quantities of input in M3, output node will be high or low. If the input is zero, the output node is connected to a power supply; otherwise, the land will be output. Table 3 describes the size of transistors. The length of all transistors is considered 0.18 um. Power consumption of this circuit is 10 mW. Table 4 a shown in Sizes of circuit transistors

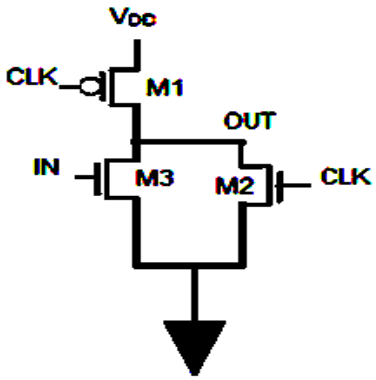

Figure 3. High-speed circuit (HS0)

Table 3. The zize of transistors of the circuit

Transistor number	W (um)
M1	90
M2	50
M3	50

Table 4. Sizes of circuit transistors

Transistor number	W (um)
M1	9
M2	5
M3	5
M4	15
M5	9
M6	5
M7	9
M8	5
M9	15
M10	5
M11	9
M12	5
M13	5
M14	5
M15	5
M16	9
M17	15
M18	9
M19	5

3.2. Designing comparator circuit

Comparator circuit is of one of the most important analog and digital circuit blocks. Therefore, it is necessary that its optimal circuit be designed and simulated. Figure 4 is recommended for comparison circuit. In fact, the proposed comparator circuit is a dynamic comparator that uses much less power. When the clock is "1", low NMOS transistor is turned on and the above PMOS transistors whose gates are connected to the clock are off. If VINN is larger than VINNP, outp is "1" and outn is "0" and vice versa. Despite the simplicity, this circuit has low number of transistors, low power consumption, and excellent performance that is shown below. Figure 5 shows the result of simulation of the proposed comparator circuit. One can see that in the rising edge of the clock comparison operation is done correctly. Figure 6 shows the graph of comparing the power consumption. We can see that this comparison uses power only when the clock switches, and at other times the power consumption is zero. Comparison of the comparator with previous works a shown in Table 5.

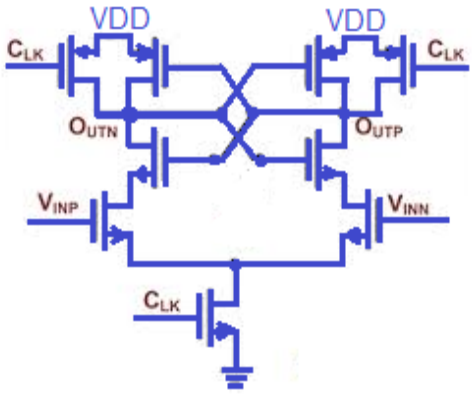

Figure 4. The proposed comparator circuit with GDI technique

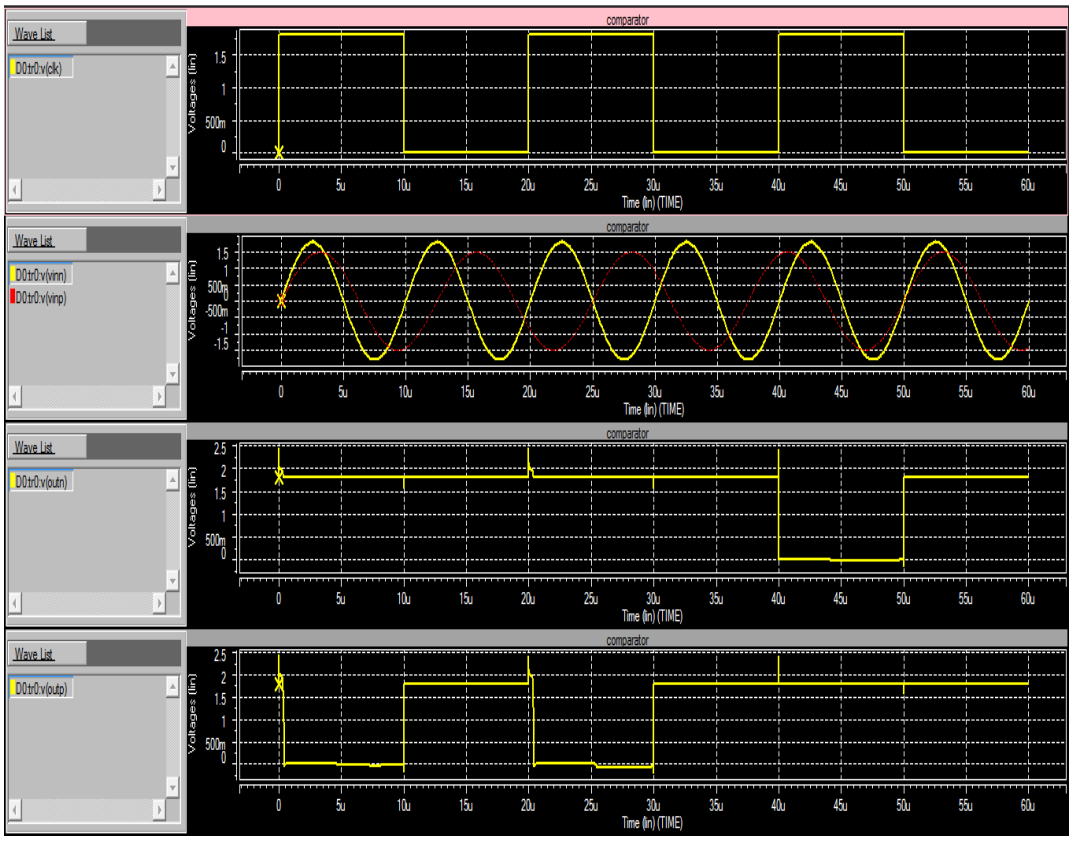

Figure 5. The result of time of the proposed comparator circuit with GDI technique

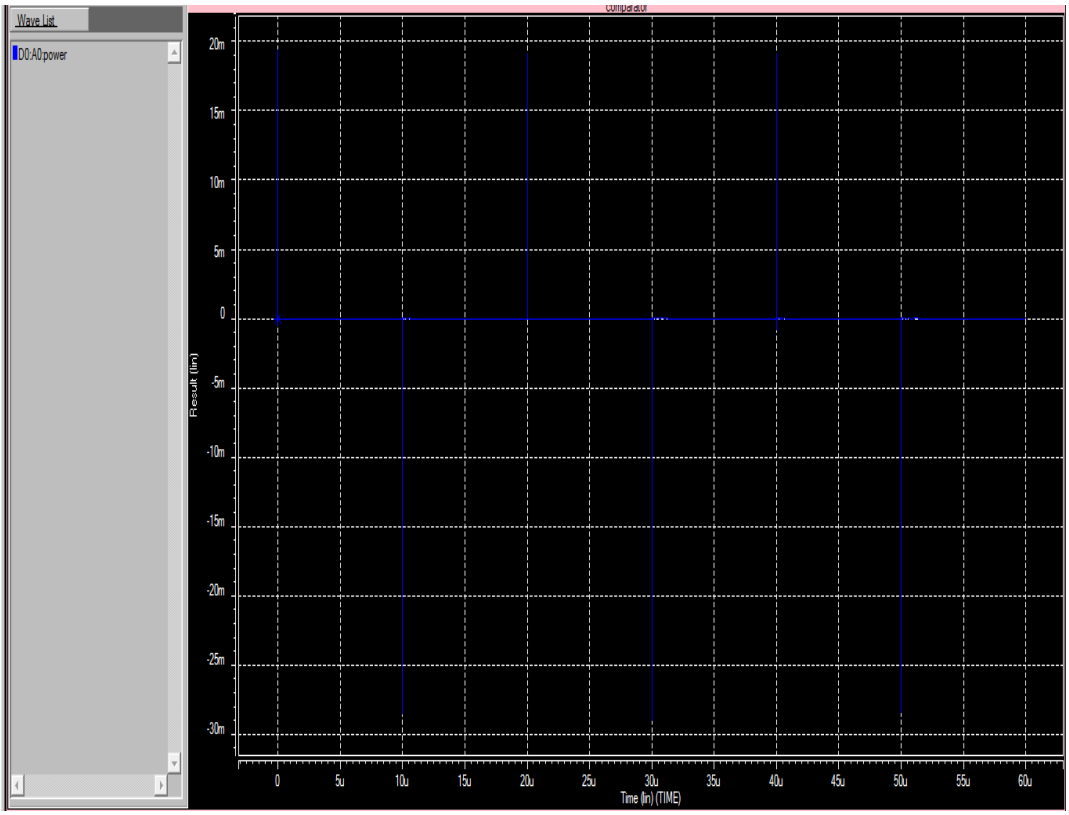

Figure 6. Power consumption of the proposed comparator circuit with GDI technique

Table 5. Comparison of the comparator with previous works

Delay	Power consumption	Comparison
2.8 ps	0.5 mW	This study
16 ps	0.61 mW	[2]
35 ps	0.461 mW	[3]

3.3. Designing the proposed sample and hold circuits

As used in the research we want to design with the least number of transistors, we design a sample and hold circuit using GDI logic. Moreover, capacitor switch technique is used to reduce power consumption. The input of sample and hold circuit is a sine wave with a 1 MHz bandwidth, and sample signal frequency is 100 MHz. Figure 7 shows the sample and hold circuits. The simulation result of this circuit is plotted in Figure 8. Now, using this technique, we design collector circuit. Figure 9 shows collector circuit using this technique. In [4], using GDI, a complete collector is designed whose circuit is plotted in Figure 9. Here, we first design and simulate the circuit and then propose a circuit with fewer transistors. Table 6 shows comparing sample and hold to the previous works.

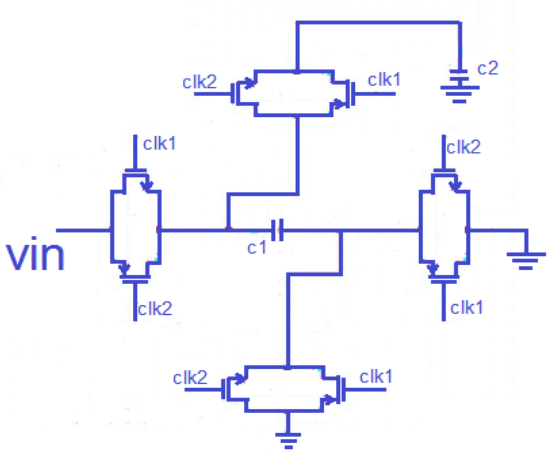

Figure 7. Sample and hold circuits using GDI technique

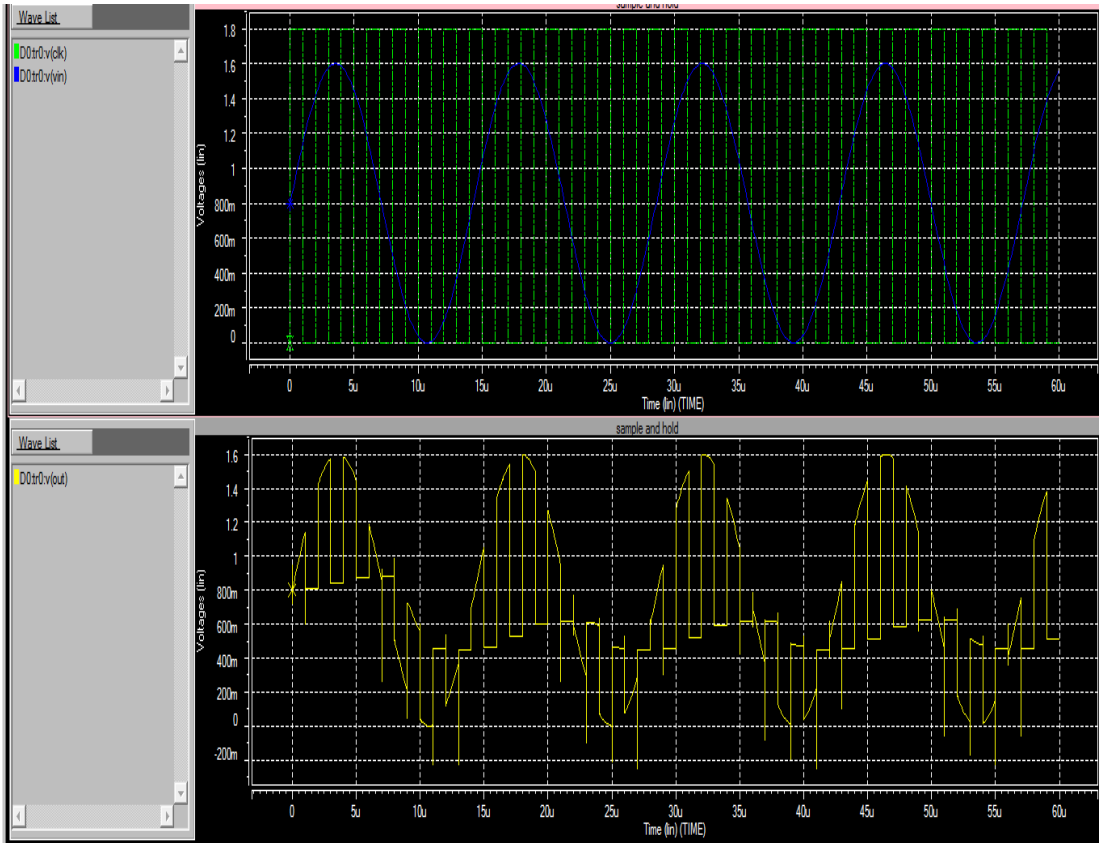

Figure 8. The results of simulation of sampling and hold circuit with GDI technique

Table 6. Comparing sample and hold to the previous works

Power consumption	Comparison
8 mW	This study
55 mW	[5]
20 mW	[6]
10 mW	[7]

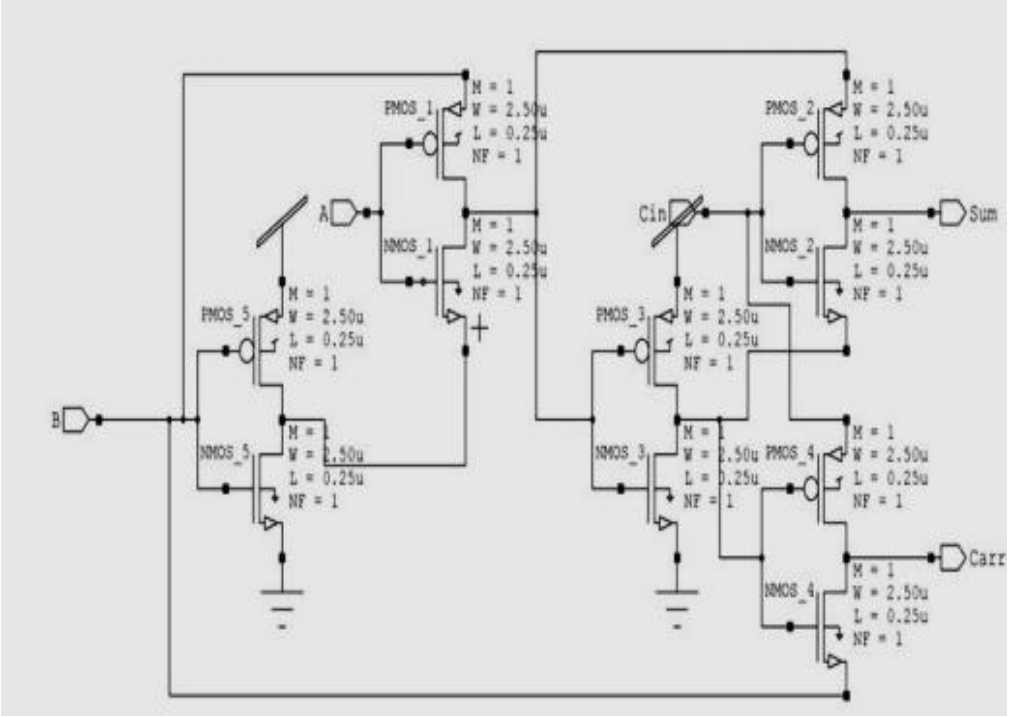

Figure 9. Collector circuit with GDI technique

3.4. The proposed collector circuit with GDI technique

Here, we offer a complete collector circuit designed using multiplexers designed with GDI. Figure 10 shows the circuit schematic of the proposed collector. Here, we have used three multiplexer and an inverter for designing the collector. The size transistors of the circuit shown in Table 7.

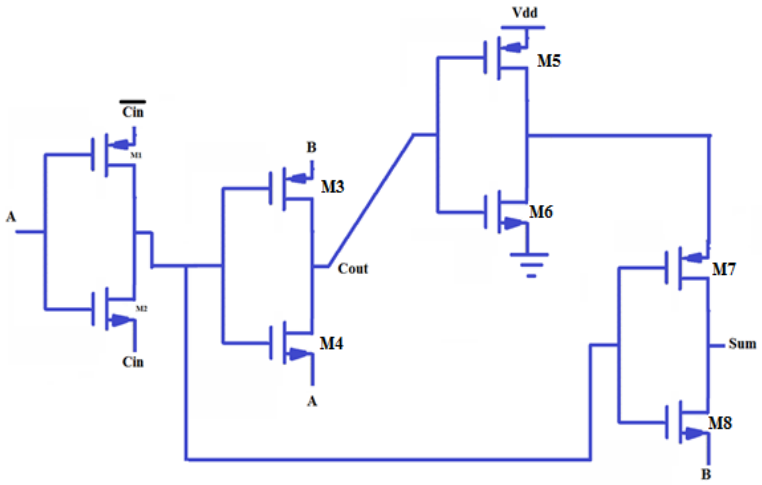

Figure 10. The proposed collector circuit with GDI technique

Table 7. The size transistors of the circuit (11)

Transistor number	W (um)
M1	9
M2	5
M3	5
M4	15
M5	9
M6	5
M7	9
M8	5

Figure 11 shows the result of time simulation of this collector. The proposed collector in addition to having a better time response has less power consumption as well. Delay graph of this collector is shown in Figure 12. From this figure, we can see that the proposed collector circuit has 40 ps delay, which is ten times less than the previous collector. The characteristics of the proposed collector circuit as shown in Table 8. Compares the results of the proposed collector compared to the previous ones as shown in Table 9.

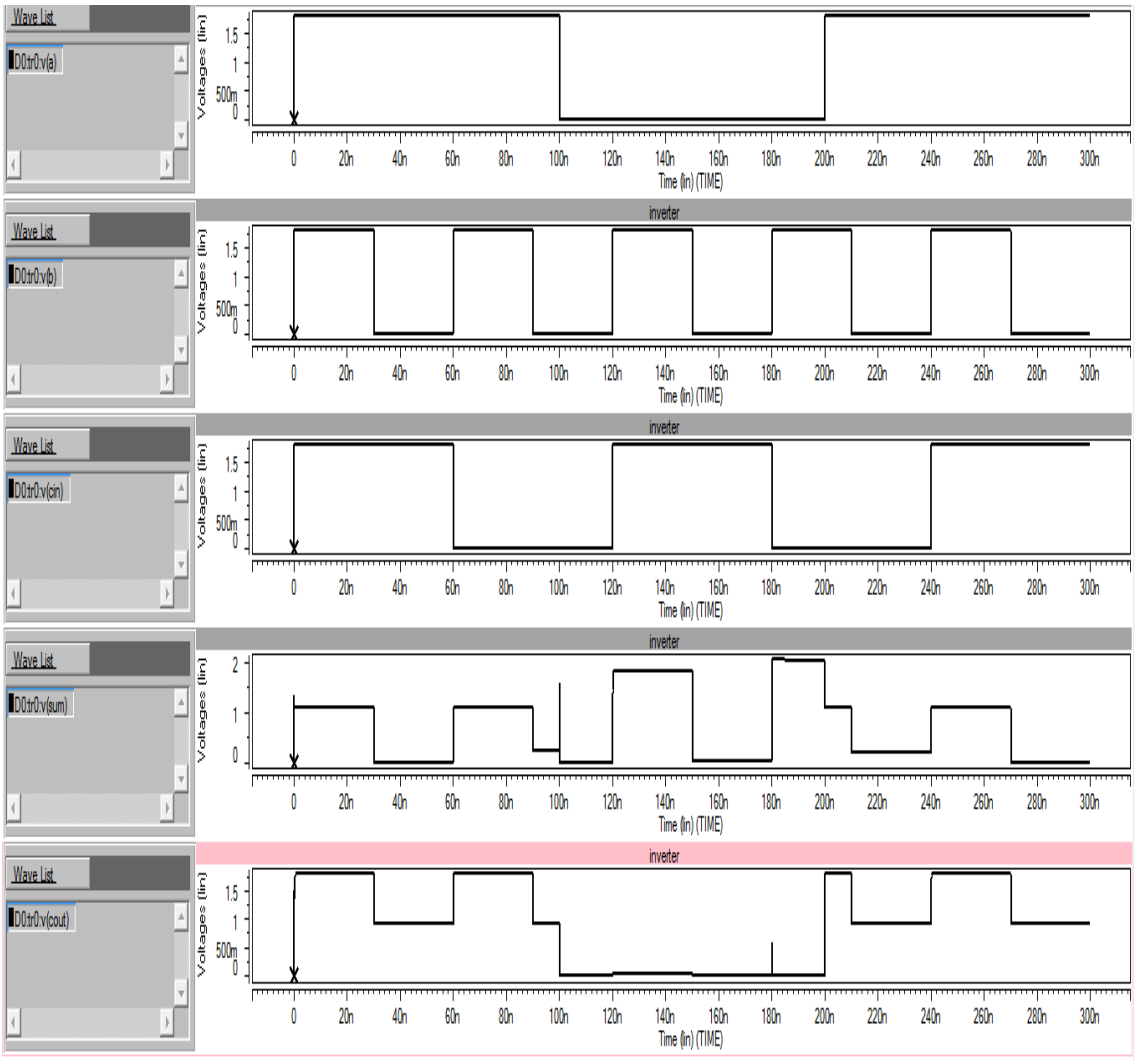

Figure 11. The simulation result of the proposed collector with GDI technique

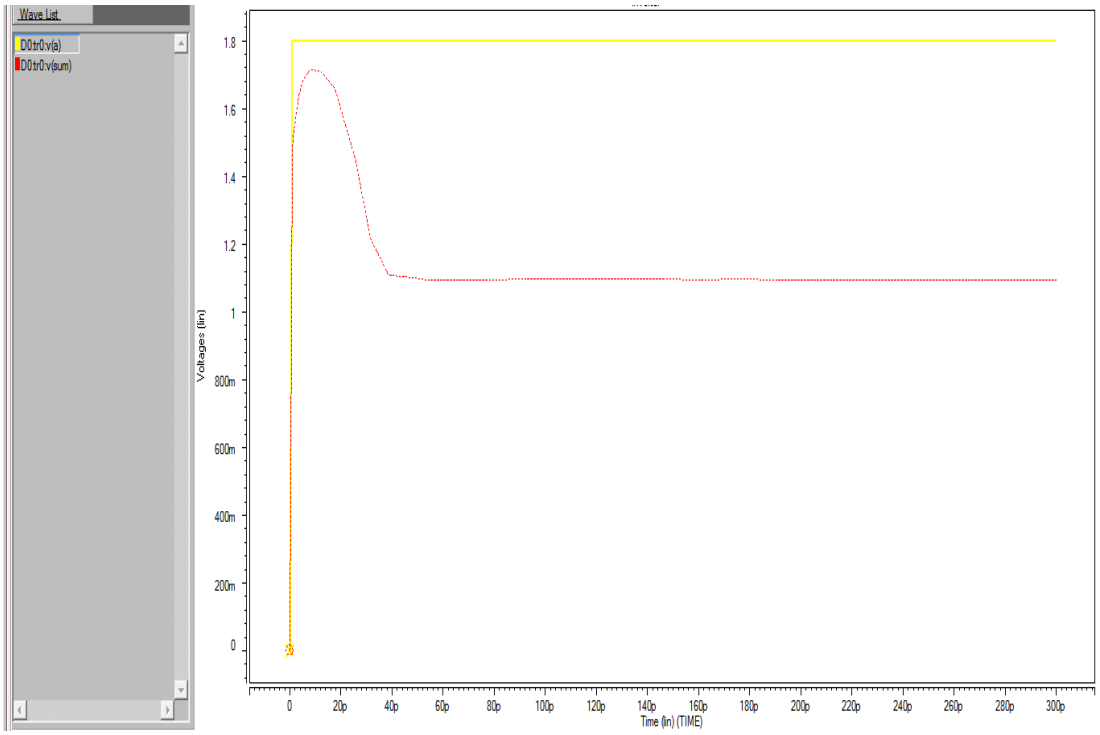

Figure 12. Delay of the proposed collector with GDI technique

Table 8. The characteristics of the proposed collector circuit

Values	Power consumption	Delay	PDP (ns*mW)
Temperature 0	200 u	0.04 n	5.74
Temperature 50	210 u	0.04 n	-
Temperature 120	220 u	0.04 n	-
0.9 V supply	100 u	0.08 n	-
1.8 V supply	200 u	0.04 n	-
3.3 V supply	430 u	0.03n	-
1 pF capacitor	200 u	0.02n	-
2 pF capacitor	200 u	0.04 n	-
5 pF capacitor	200 u	0.07n	-

Table 9. Comparison of the proposed collector to the previous ones

Collector	Power consumption	Delay	PDP (ns.mW)
Proposed collector	200 uW	0.04 ns	0.008
[8]	1.73 mW	1.009 ns	1.8
[9]	5.736 uW	0.179 ns	0.00126
[10]	127 uW	1.117 ns	129

4. CONCLUSION

Provide a statement that what is expected, as stated in the "Introduction" chapter can ultimately result in "Results and Discussion" chapter, so there is compatibility. Moreover, it can also be added the prospect of the development of research results and application prospects of further studies into the next (based on result and discussion).

ACKNOWLEDGEMENTS

In this study, we dealt with the simulation of different dynamics logic circuits, compared their results, and then offered a circuit for reducing power consumption. We saw that using the proposed buffer circuit power consumption was reduced sharply and its delay was lower. In the next level, we designed logic circuits in GDI techniques and designed logic circuits such as AND, OR, XOR and multiplexer with this technique. It was observed that this technique with fewer number of transistors, one can design logic circuits.

Then we dealt with designing collector circuit with this technique and offered a collector circuit using this technique. With examining the foregoing, we concluded that the proposed circuit compared to the previous works has much less delay and power consumption. To continue the study, the following suggestions are presented: Designing logic circuits with GDI technique and nanotube carbon transistor, Designing a CPU with GDI technique, Design a multiplier with GDI technique.

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