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Comparison analysis of three value logic 8T CNTFET SRAM cell with 6 CMOS SRAM cell at 32nm technology

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ABSTRACT

This paper proposed a new concept of highly SNM and low power SRAM cell using carbon nanotube FETs (CNTFETs) at 18nm technology node. As device physical gate length is reduced to below 65 nm, device non-idealities such as large parameter variations and exponential increase in Dynamic leakage current make the I-V characteristics substantially different from traditional MOSFETs and become a serious obstacle to scale devices. CNFETs have received widespread attention as one of the promising successor to MOSFETs. The proposed circuit was simulated in HSPICE using 32nm Stanford CNFET model. Analysis of the results shows that the proposed CNTFET based 3VL 8T SRAM cell, power dissipation, and stability substantially improved compared with the conventional CMOS 6T SRAM cell by 51% and 58% respectively at the expense of 4% write delay increase.

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1. INTRODUCTION

For the foreseeable feature, static random access memory (SRAM) will likely remain as the embedded memory technology of choice for many microproces-sors and systems on chips (SoCs) due to the speed ad-vantage and compatibility with standard logic process-es. With the advent of SoC, the design of highly static and Low power efficient SRAM structures has become high-ly desirable. Therefore, it is essential to develop a Dynamic low power SRAM design technique for the new device technology such as CNTFET.

Carbon Nanotube Field Effect Transistor (CNFET) is the most promising technology to extend or comple-ment the traditional silicon technology due to the fol-lowing three reasons: First, the operation principle and the device structure are similar to CMOS devices, and the established CMOS design infrastructure can be utilised. Second, the CMOS fabrication process can still be utilised. And the most important reason is that CNFET has the best experimentally demonstrated de-vice current carrying capability so far. Several re-searches have been done to estimate the performance of CNFET at a single device level in the presence of process related non-idealities and imperfections at the 32 nm technology node using compact CNFET SPICE model [1, 2].

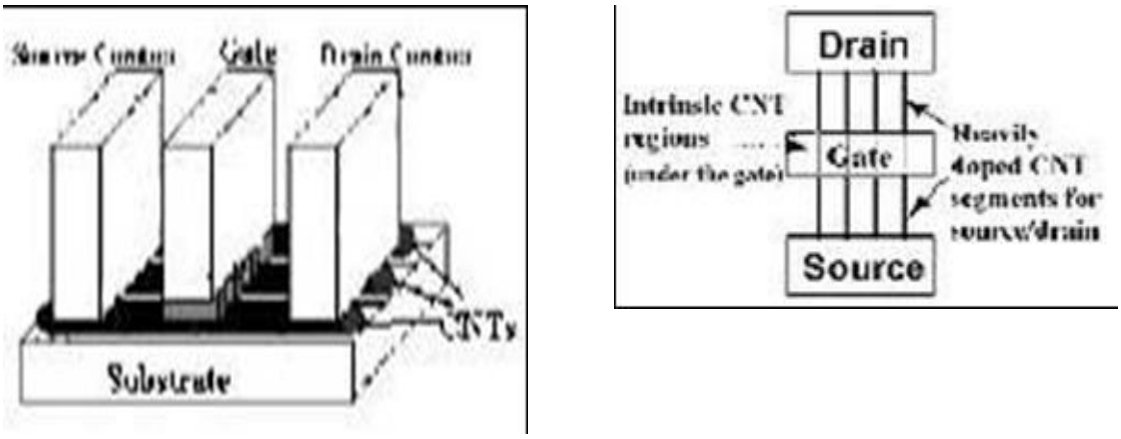
In this paper, as a circuit level design of CNTFET, a novel low power and highly stable 3 VL 8T SRAM cell design is proposed and its performance and viability are demonstrated by performing various simulations. The stability and power consumption of the 8T SRAM cell based on CNTFET are compared with that of the conventional CMOS 6T SRAM cell design to show the comparison of the CNTFET based SRAM cell design. Comparison. The circuit simulation in this paper uses a 32nm CNFET HSPICE model that includes the practical de-vice non-idealities for CNFET [3, 4] and the 32nm BSIM PTM (predictive technology model) for Si MOSFET [5].

This paper is organised in the following manner: The characteristics and physical features of CNTFET Tran-sistor are explained in section II, section III describes the 3value logic and section IV describes, the mecha-nisms of the read and write operations of the proposed 8T CNTFET SRAM cell and the schemes for deciding the number of nanotubes of each. The simulation re-sults are presented in section IV to compare the per-formance and viability of the CNTFET technology with that CMOS technology, and followed by the conclusion in Section V.

2. CNTFET TRANSISTOR

Carbon nanotube Field Effect transistors (CNTFETs) utilise semiconducting single-wall CNTs to assemble electronic devices; CNTFETs have been shown to have similar properties to MOSFETs. A single-wall carbon nanotube (or SWCNT) consists of only one cylinder, and the simple manufacturing process of this device makes it a very promising alternative to today's CMOS technologies. An SWCNT can act as either a conductor or a semiconductor depending on the angle of the atomarrangement along the tube. This is referred to as the chirality vector and is represented by the integer pair (n, m) [6]. A simple method to determine if a carbon nanotube is metallic or semiconducting is based on considering the indices (n, m), i.e. the nanotube is metallic if n=m or n-m=3i where i is an integer. Other-wise, the tube is semiconducting. The diameter of the CNT can be calculated from [6] as a function of m and n. Figure 1 shows the schematic diagram of the CNTFET [6]. Similar to the silicon device the CNTFET has four terminals, a dielectric film is wrapped around a portion of the undoped semiconducting nanotube, and a metal gate surrounds the dielectric. Figure 2 shows the equiva-lent circuit model implemented in HSPICE as proposed in [6]. Heavily doped CNT segments are placed be-tween the gate and the source/drain to allow for a low series resistance during the on-state [7]. As the gate potential increases, the device is electrostatic-ally turned on or off via the gate.

The current-voltage (I-V) characteristics of the CNTFET are shown in Figure 3, and they are similar to those of MOSFET. The CNTFET device current is sat- urated at higher Vds (drain to source voltage) as chan-nel length increases as shown in Figure 3, and the on-cur-rent decreases due to energy optimisation in the axial.



(a) (b)

Figure 1. Schematic diagram of a carbon nan-otube transistor (CNTFET):
(a) sectional view; (b) top view

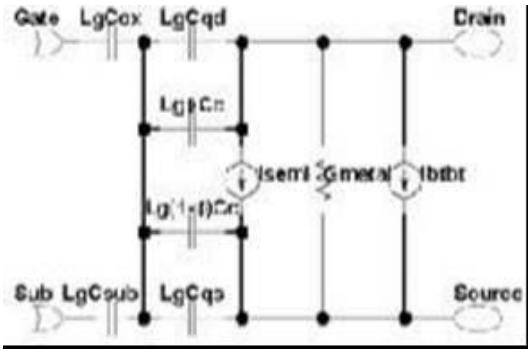


Figure 2. Equivalent circuit model for the in-trinsic channel region of a CNTFET

3. THREE VALUE LOGIC DESIGN

A three-value logic system was first developed by Jan Lukasiewicz, in 1920, in its popular paper O Log-ice Tr´ojwarkoscioewj [8], as abstraction of the tradi-tional binary logic. Three-value logic system has better characteristic compared to previous binary system such as increased bit handling capability per unit area, re-duced number and complexity of interconnections, as well as reduced number of active FETs inside a chip. Hence, in the circuit which designs base on three-val-ued logic, circuits will be simpler and more flexible also more easy. By using Three-VL higher SNM and less power Dynamic dissipation will be achieved [9, 10]. To obtain 3value logic system we need three values, in conven-tional binary system we have two logics values '0' and '1', these logics represented by 0V and Vdd respective-ly. By supplementing one state between these two log-ics of conventional binary system ternary logic system can be achieved. In 3value logic system values repre-sented by 0V, Vdd/2 and Vdd which denote '0', '1' and '2' respectively.direction at 32-nm (or less) gate length [6].

In principle, 3VL can provide a means of increasing data processing capability per unit chip area. The serial and serial-parallel arithmetic functions can be carried out faster if the 3value logic is employed. One of the main merits of 3value logic is that it reduces the num-ber of required computation steps. As each input can have three distinct values, the number of digits required in a 3VL family is log32 times less than that required in binary logic. It is assumed that 3value logic elements can operate at a speed approaching that of the corre-sponding binary-logic elements. However, if the 3VL and binary logic gates are used to take advantage of their respective merits, performance could be signifi-cantly improved because 3value logic gates are good candidate for decoding block since it requires less number of gates while binary logic gates are a good candidate for fast computation modules. Thus, 3value design technique combined with the binary logic gate design technique also provides an excellent speed and power consumption characteristics in memory circuits.

Three value logic functions are defined as the functions having convincing if a third value is introduced in to the binary logic. Here, 0, 1, and 2 denote the 3 logic values to represent true, intermediate, and false, respec-tively. Any n-variable {Z1 ,. . .,Zn} 3 value logic func-tion f(Z) is defined as a logic function mapping {0,1,2} n to {0,1,2}, where Z={Z1 ,. . .,Zn}. The basic opera-tions of 3value logic can be defined as follows, where Zi,Zj {0,1,2}

$$Zi \mid Zj = \max\{Zi, Zj\}$$
$$Zi \,\&\, Zj = \min\{Zi, Zj\}$$
$$\overline{Zi} = 2 - Zi$$

Where "−" denotes the arithmetic subtraction, the oper-ations "|," " &," and "−" are referred to as the OR, AND, and NOT in 3value logic, respectively. The 3 value logic gates are designed according to the conven-tion defined in above equation. Here work the set {0, 1, 2} is used, where 0=false, 1= intermediate, and 2=true. Table 1 shows the truth table of all the basic 3Val-ue logic gates. The choice of these values leads in a more natural way the adaptation of the ideas from the binary logic.

4. PROPOSED 8T CNTFET SRAM CELL

A new 3 VL 8T CNTFET SRAM cell structure is proposed in this paper to increase SNM and to reduce the power consumption of the SRAM cell.

4.1. 8T SRAM Cell Design

The need of 8T-SRAM has originated from the fact that the 6T SRAM has more power consumption and less immunity to noise voltage during read operation as a small noise voltage is enough to flip the data. Designing an efficient cache system with 8 transistors in basic SRAM cell provides increased stability and good effective memory speed. Figure 7 shows the 8T SRAM cell configuration based on CNTFETs, where the write and read bits are separated to improve read cycle. In 8T SRAM only the Write bit is used to write for both "0" and "1" data, while BIT and BIT lines are utilized for writing data in the conventional 6T SRAM.

The writing operation starts by breaking the feedback loop of the cross-coupled inverter. During read operation, the feedback loop is maintained. The feedback loop is disconnected by setting Write bit to"1".In this case, SRAM memory cell has just two cascaded inverters. The Wbit line voltage decides the data that is going to be written into SRAM cell. The Wbit line transfers the inversion of the input data to Q2 (cell data), which drives the other cascaded inverter to get Q_bar. The Wbit line has to be pre-charged before and after each write operation. When writing "0" data, there is no. Discharging at WBit line so negligible power is consumed. But writing '1' data at Q2, the dynamic power consumption is same as 6T SRAM cell because the WBit line has to be discharged to ground level. The proposed 8T SRAM cell is more power efficient in comparison with conventional ones because during write operation, the circuit does not require discharging for every write operation but discharges only when writing "1" data, and the discharging activity factor of the WBit line is less than 1.

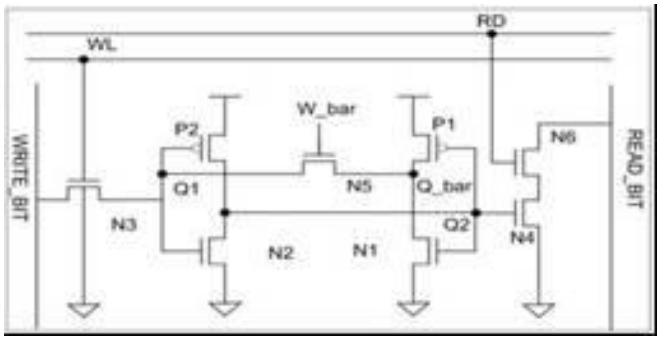


Figure 3. Circuit diagram for 8T CNTFET SRAM cell

The Rbit line has to be pre-charged before any read operation. During read operation, Read bit is "high" and Write bit is low, which set turning ON condition for N5 & N6. When Q2="0", the transistor N4 is OFF maintaining the Rbit line at the pre-charged value, which shows the cell data Q2 holds "0". On the other side, when cell data Q2="1", both the transistors N4 and N6 are ON which makes the Rbit line to be dropped at few millivolts, which is quite enough for detection in the sense amplifier. In the proposed 8T SRAM cell design, the device sizing of the read zero path with pull down transistor N4 and N6 is made 8 and 6 times larger to get a quicker discharge path to ground. In this design, two PCNTFET (P1,N5) with one tube, two NCNTFETs (N2,N3) with two tubes, one P-type CNTFET (P2) with two tube, one NCNTFET (N1) with one tube, are utilized for proper functionality and shorter delay at the minimal cost of the chip area overhead. Compared to CMOS SRAM cell with a transistor length of 32nm, a CNTFET SRAM cell offers a significant saving in chip area.

5. SIMULATION RESULTS

6T SRAM and 3VL 8T SRAM cells are designed using bulk CMOS and CNTFET transistors respective-ly. HSPICE simulations are performed at 18nm tech-nology node using the Stanford CNTFET model and the Predictive Technology Model **(**PTM) to compare the performance of the 3VL 8T CNTFET and 6T CMOS SRAM cells.

5.1. Simulation setup

The following technology parameters are used for simulation of 3VL 8T SRAM cell using CNTFET. Technology: Lch (physical channel length)=32.0nm, Lss (the length of the doped CNT drain-side/source-side extension region)=18.0nm, Efi (Fermi level of the doped S/D tube)=0.6 eV, Tox (The thickness of high-k top gate dielectric material)=4.0nm, (n1, n2) (chirality of tube)=(19,0), pitch=10nm, Vfbn

and Vfbp (Flat-band voltage for n-CNTFET and p-CNTFET)=0.0eV and 0.0eV, physical gate length=32.0nm, Lgeff (the mean free path in intrinsic CNT channel region due to non-ideal elastic scattering) =200.0nm, Lss/Ldd (the length of the doped CNT source/drain extension region)=32.0nm, the mean free path in p+/n+doped CNT=15.0nm, the work function of Source/Drain metal contact=4.6eV, and CNT work function=4.5eV.

The minimum transistor sizes used for CMOS and CNTFET technologies are W=48nm and L=18nm for bulk CMOS, and L=18nm and the number of tubes=1 for CNTFET. A Power supply of 0.9 V is used [11]. Table 1 shows the summarised results to compare the proposed 3VL 8T CNTFET SRAM characteristics with the conventional CMOS 6T SRAM cell.

5.2. Dynamic power consumption

The newly proposed 3VL 8T CNTFET SRAM cell achieves 41% writing power saving while maintaining the cell performance, read/write delay, and stability of the conventional cell. The power saving comes from the fact that the cell keeps Write_Bit "high" instead of discharging when it writes "0", which reduces the ac-tivity factor of the Write_Bit. Figure 4 shows the dynamic low power consumption with VDD variation. Figure 5 shows Leakage power and SNM consumption with VDD variation.

Table 1. Summarised simulation results

	6T CMOS SRAM	3 VL8T CNTFET SRAM
Dynamic Power (W)	1.98E-06	1.602E-06
Leakage Power (nW)	110	107.64
Write Delay (pS)	34.0	32.54
Read Delay (pS)	23.87	22.37
SNM (mV)	120	141.76

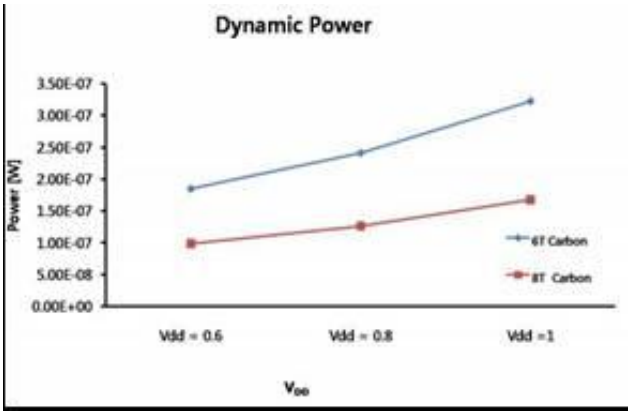


Figure 4. The dynamic low power consumption with VDD variation

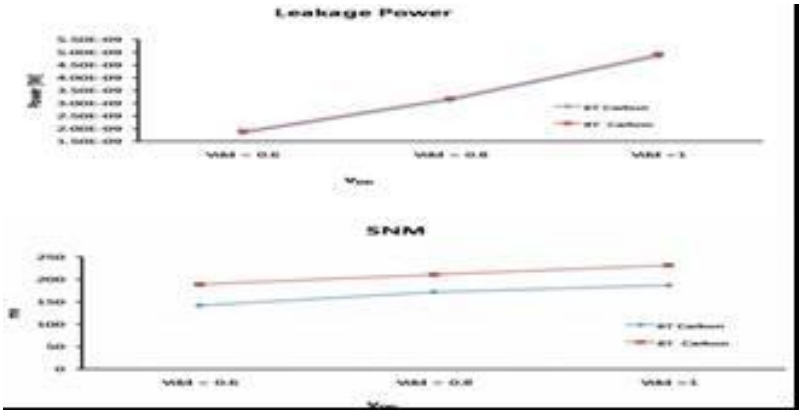


Figure 5. Leakage power and SNM consumption with VDD variation

While conventional 6T CMOS SRAM always dis-charges one of the bit lines to write a data into the cell, the proposed 8T CNTFET SRAM discharges the Write_Bit only when it writes "1". As the probability of writing '0' gets higher, the power dissipation due to the bit line discharging is reduced comparing to the con ventional case. Figure 4 shows the dynamic power con-sumption of the CNTFET 8T SRAM cell for different VDD. As shown in the Figure 4, the power saving of the 8T CNTFET SRAM cell becomes greater as V DD in-creases since the dynamic power difference between the 6T CMOS SRAM and the proposed 9T CNTFET SRAM cell increases exponentially as VDD increases.

5.3. Leakage power consumption

The leakage power of the 6T CMOS SRAM cell and 3VL8T CNTFET SRAM cell. In the 3VL8T CNTFET SRAM cell, the bit line leakage is significantly reduced by adding a NMOS transistor (N8), because of the so-called "stack effect" between N7 and N8. The reduced bit-line leakage makes it possible to have more SRAM cells on a bit-line for high-density SRAM designs. 8T CNTFET SRAM cell, the bit-line leakage is signifi-cantly reduced by adding a NMOS transistor (M9), because of the so-called "stack effect" between M8 and M9. The reduced bit-line leakage makes it possible to have more SRAM cells on a bit-line for high-density SRAM designs.

5.4. Static noise margin

Static Noise Margin (SNM) is the standard metric to measure the stability in SRAM bit-cells. The SNM of SRAM cell is defined as the minimum DC noise volt-age necessary to flip the state of the cell. The voltage transfer curves (VTCs) of the back-to-back inverters in a bit-cell are used to measure SNM. Separating the Read and Write bit offers wider SNM during read oper-ation as shown in Figure 7. When reading the stored data, only Read_Bit affects inverter1 (N1/N2) output volt-age. Consequently, this fact makes the cell hard to flip. Table 1 shows 8T CNTFET SRAM cell has the highest SNM because of the relatively higher Vth and lower leakage current than CMOS based SRAM cells.

5.5. Write and read delay

For write operation, the write delay is defined as the time from the 50% activation of the WL to the time when Q_bar becomes 90% of its full swing. The write delay is approximately equal to the propagation delay of the inverter2 (M3/M4) and inverter1 (N1/N2). Be-cause the inverter1 is only driving the diffusion capaci-tor of M7, it is desirable to reduce the input capacitance of the inverter1 as much as possible to reduce the load capacitance on inverter2. The proposed 3VL 8T CNT-FET SRAM cell is slightly slower than 6T SRAM in writing operation because of this reason.

The read time depends on the READ path's transis-tors' sizes. The proposed 3VL 8T CNTFET SRAM cell READ delay is almost same as the conventional 6T CMOS SRAM cell since the transistor sizes are very similar. The READ access time at the cell level is de-termined by the time taken for the bit-lines to develop a potential difference of at least 100mV.

6. CONCLUSION

This paper has investigated the use of MOSFET-like CNTFET in place of the conventional CMOS in the design of SRAM cell. This new 8T CNTFET SRAM cell is compared with CMOS based 6T SRAM cell. This new 3VL 8T CNTFET SRAM cell cuts off the feedback connection between the two back-to-back inverters in the SRAM cell when data is written and separates the write and read port with 8 transistors. Compared to 6T SRAM structure, the proposed 3VL 8T CNTFET SRAM saves power up to 51% and ob-tains 58% higher SNM during read operation at the minimal cost of 4% delay increase. These Simulation results show that the CNTFET based 8T SRAM cell design achieves improvements in stability and power consumption, especially at a low power supply.

REFERENCES

[1] R. Chau, S. Datta, M. Doczy, B. Doyle, B. Jin, J. Kavalieros, A. Majumdar, and M. Radosavlijevic, "Benchmarking nanotechnology for high-perfor-mance and low-power logic transistor ap-plications," *IEEE Trans. Nanotechnol*., vol. 4, no. 2, pp. 153-158, Mar. 2005.

[2] Jie Deng, "Device modeling and circuit perfor-mance evaluation for nanoscale devices: silicon technology beyond 45 nm node and carbon nan-otube field effect transistors," Dissertation, June. 2007.

[3] J. Deng and H.-S. P. Wong, "A Circuit-Compatible SPICE model for Enhancement Mode Carbon Nanotube Field Effect Transistors," Proc. *Intl. Conf. Simulation of Semiconductor Processes and Devices*, pp. 166 - 169, Sept., 2006.

[4] I Amlani, et al., "First Demonstration of AC Gain From a Single-walled Carbon Nanotube Com-mon-Source Amplifier," Proc. *Intl. Electron De-vices Meeting*, Paper 20.7, Dec., 2006.
[5] Berkeley Predictive Technology Model website [Online]. Available: http://www eas.asu.edul-ptm/latest.html
[6] Stanford University CNFET Model website [On-line]. Available: http://nano.stanford.edu/mod-el.php?id=23
[7] J. Appenzeller, "Carbon Nanotubes for High-Performance
[8] J. Deng and H.-S. P.Wong, "A Compact SPICE model for carbon-nanotube field-effect transistors including non idealities and its application—Part II: Full device model and circuit performance benchmarking," IEEE Trans.Electron Device, vol. 54, no. 12, pp. 3195–3205, Dec. 2007.
[9] J. Deng and H.-S. P.Wong, "A Compact SPICE model for carbon-nanotube field-effect transistors including non idealities and its application—Part II: Full device model and circuit performance benchmarking," *IEEE Trans.Electron Device*, vol. 54, no. 12, pp. 3195–3205, Dec. 2007.
[10] Lucasiewicz, Jan O Logice Tr´ojwarkoscioewj English translation: On three-valuedlogic, in L. Borkowski (ed.), Selected works by Jan Lukasiewicz, North-Holland, Amsterdam, 1970, pp. 87-88
[11] S. Lin,Y. B. Kim, and F. Lombardi, "The CNTFET-based design of ternarylogic gates and arithmetic circuits,"*IEEE Trans. Nanotechnol.,* vol. 10,no. 2, pp. 217–225, Mar. 2011.