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New Optimized Reconfigurable ALU Design Based on DG-CNTFET Nanotechnology

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ABSTRACT

The heart of the microprocessor and responsible for the execution of logical and arithmetic operations, the arithmetic and logical unit is constantly optimized. The performance is improved to allow the development of more powerful and smaller circuits. This paper describes simple ALU but contains the essentials functions. It is a reconfigurable ALU based on double-gate carbon nanotube field effect transistor (DG-CNTFETs). This transistor has an interesting property, it can switch from p- to n- type behavior and vice-versa dynamically. This opens the opportunity for building novel and complex functions in fine-grain reconfigurable logic inaccessible to MOSFETs and reaching a good performance levels. In literature there are several problems related to signal quality. In this paper, we will propose a new solution that allows us to improve the quality of the output signal without affecting the number of transistors used. This improves the overall performance of ALU. We will show the improvement in signal level and quality. First, an overview of carbon nanotube field-effect transistor (CNTFET) and state of the art Reconfigurable ALU based on DG-CNTFET is given. Then an explication of signal integrity issues of the actual Reconfigurable DG-CNTFET cell is done. After we will present and explain the proposed solution. The solution is first applied on the cnt_9T circuit then will show its effect on the ALU. Finally, a performance comparison is made.

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1. INTRODUCTION

In order to maintain the technological growth, integrated circuits are still improving. It needs high performance in terms of speed, integration density, power and reliability. In parallel, as expected by Semiconductors professional community CMOS will reach its limits in 2020 (Moore's law) due to intrinsic device problem like leakage and quantum effects [1]. Semiconductor industry are pushed to enter in a new era called "Beyond CMOS". They are exploring the use of new materials and devices that can solve this problem, for example by adopting high mobility materials to improve mobility, reduce noise, or increase electrostatic currents, reducing parasites or increasing electrostatic current. The carbon nanotube field-effect transistor (CNTFET) is the most promising alternative thanks to his specific physical characteristics (high carrier mobility, ballistic electron transport and current density) [2], [3]. Several families of CNTFET were manufactured and studied but a one of them called DG-CNTFET has an interesting property, the ambipolarity. In contrast of others CMOS devices whose polarity (n-type or p-type) is determined during fabrication, DG-CNTFETs are ambipolar, they lead electrons and holes mutually, presenting a coexistence of electron and hole currents.

DG-CNTFET allow the creation of completely novel circuit which are inaccessible with MOSFET-based circuits. One of the most critical Integrated Circuits (ICs) today's is Arithmetic logic. Indeed, arithmetic operations are the basis of data paths that form the reasoning core of logic applications in silicon. Several works proposed the implementation of ALU with DG-CNTFET for example in [5] but we believe that these works suffer from the problem of signal integrity. Motivated by these observations, this paper make contribution in output signal quality improvement without affecting the density of circuit. Simulation will prove the improvement of signal level and the overall of ALU performance. In Section II, an overview of different types of existing CNTFET transistors are presented and we will focus on DG-CNTFET to explain his ambipolarity. The state of art of reconfigurable ALU based on this transistor will be described in section III. In next section, we will explain the signal quality issue which pushed us to do this work .The proposal solution is specified in section V and simulation is done to demonstrate the benefit of this solution on CNT_9T first and reconfigurable ALU. Finally a conclusion is made.

2. OVERVIEW OF AMBIPOLAR CNTFET (DG-CNTFET)

This section presents the most important types of CNTFET. Almost, transistors operate on the same principle: current passed between the source and drain electrodes through the nanotube channel depends on the polarization of the gate electrode. Nature of the contact between nanotube and the source/drain metal electrodes is the main difference between the transistors described below. We differentiate three categories of CNTFET: SB-CNTFET, C-CNTFET and DG-CNFET. In SB-CNFET source and drain electrodes are deposited directly on the nanotube channel, this metal-nanotube junction creates the Schottky-barrier. Conductivity of this barrier depends on gate polarization who acts on the variation of the contact resistance. SB-CNTFETs have an ambipolar characteristics, which is not suitable for conventional CMOS-like logic circuits but very useful for building new logic architectures different from conventional CMOS logic. Also, the ratio Ion/Ioff is rather small [3]. C-CNTFET also called CMOS-Like CNTFET have ohmic contact between the source/drain metal and the nanotube channel. The performance of this transistor are improved compared to the SB-CNFET: current Ion is higher thanks to his low barrier height and ambipolarity is often suppressed. Double Gate carbon nanotube field effect transistor DG- CNTFET is a CNTFET with double gate [4]. A front gate that plays the same function of a CNTFET Gate and a back gate called also primary gate Figure 1 which is used to dynamically change the type of transistor N or P, hence its ambipolarity. This additional back gate BG which contributes to attenuate the Schottky-Barriers, SB, at the drain and source contacts so Ion/Ioff is higher. It opens a new horizon for reconfigurable circuits [4].

DG-CNTFET show an interesting property for reconfigurable device: the ambipolarity. We will show in the following how DG-CNTFET can be used to design reconfigurable circuits. Figure 2 explain how double gate carbon nanotube field effect transistors work.

DG-CNTFET can switch from N type to P type and vice-versa depends on back gate polarity:

a. If Back Gate (BG) is polarized at 1 V transistor will have N type behavior.
b. If Back Gate (BG) is polarized at -1 V transistor will have P type behavior.

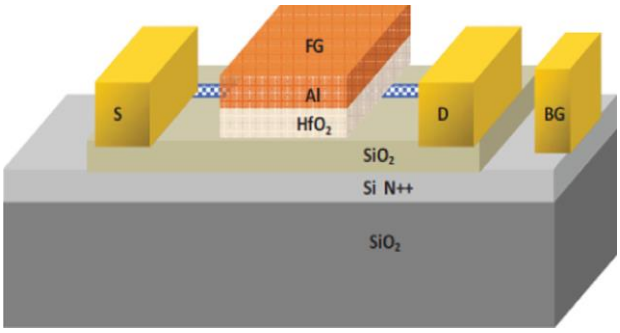

Figure 1. DG-CNTFET cross-section

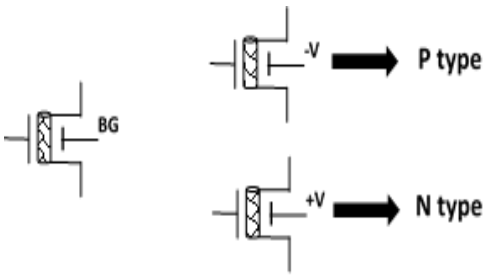

Figure 2. Behavior of DG-CNTFET depending On BG polarization

This feature can be used to design a logic circuit capable of performing several logic functions just by configuring the "back gates" of the CNTFETs network. In the next section we will describe the state of the art of reconfigurable circuit using this type of transistor.

3. STATE OF THE ART RECONFIGURABLE ALU BASED ON DG-CNTFET TRANSISTORS

The CNTFET can be used to construct logic circuits according to two possible approaches

a. In CMOS-Like designs the CNTFET replaces the MOSFET by directly transposing the architectures of the existing logical functions on this new technology. This approach has been proved experimentally both with resistive-load gates [7] and complementary logic [8].
b. In specific approach, the specific properties of the CNTFET are exploited. They allow the creation of completely new logic functions that are inaccessible (or hardly feasible) to conventional MOSFET-based circuits. Specific CNTFET properties have also been used in multiple-valued logic [9], [10] and in single transistor XOR gates [11].

As demonstrated previously DG-CNTFET offer a complete ambipolar behavior, this characteristic can be used to design revolutionary reconfigurable circuits, The CNT_DRC_9T showed in Figure 3 represent the most representative of this kind of circuits. This circuit is based on dynamic CMOS design, a pre-charge phase is needed to initialize the different blocks then we evaluate the block output. This circuit is composed by 9 DG-CNTFET transistors. As explained in Table 1, this circuit could realize 6 different functions including XOR functions (A⊕ B) and XNOR (A⊕ B)' commonly used. They allow the realization of the sum operator (in the Adders) with a reduced number of gate [5].

To explain how this logic gate works we can take as example all transistors are configured as n-type (OP1=OP2=OP3=+V):

a. Pre-charge of logic stage: The C node voltage is forced to 0 V.
b. Evaluation of logic stage: the logic part is powered on and *f* (A, B) function is evaluated.
c. Pre-charge of follower/inverter stage: The Y node voltage is forced to Vdd.
d. Evaluation follower/inverter stage: The Y node takes A NAND B.

Here in Figure 4 there is schematic of reconfigurable 3 functions ALU based on DG-CNTFET transistors.

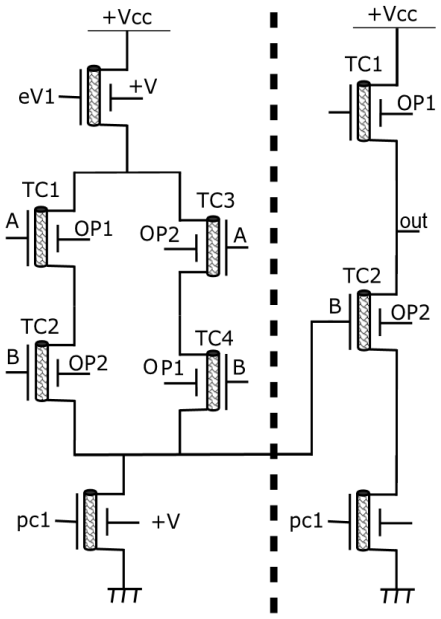

Figure 3. 9T sub-block

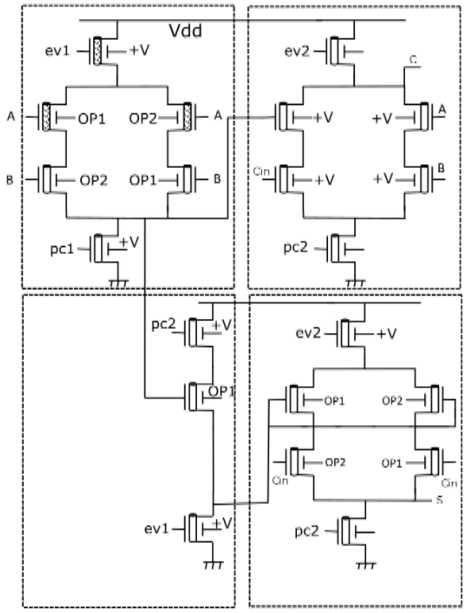

Figure 4. State of the art reconfigurable 3 functions DG-CNTFET ALU [5]

Table 1. Functions of cnt-drc_9t Cell

OP1	OP2	OP3	Y
+V	+V	+V	$\overline{A.B}$
+V	+V	-V	$A.B$
-V	-V	+V	$A+B$
-V	-V	-V	$\overline{A+B}$
+V	-V	+V	$\overline{A \oplus B}$
+V	-V	-V	$A \oplus B$

The ALU3F block is constituted of 4 different sub-blocks connected together to constitute a 1-bit full adder [12]. The most used sub-block is the 9T sub-block described in Figure 3 [5], [13].
To explain how this ALU works we can take as example all transistors configured as N type (OP1=OP2=+V):

a. The calculation of S is done in three stages, with block 1, 3 and 4. Each stage requires a pre-charge step and then evaluation.
b. Block 3 enables a follower or an inverter between the output of the area1 and the input of block 4, according to the configuration signal OP1 as explained in Table 2 [14]

Table 2. Functions of cnt-alu_3f Reconfigurable Circuit

OP1	OP2	**S**	**C**
+V	+V	A.B. Cin	$A.B$
+V	-V	$A \oplus B \oplus Cin$	$A.B + Cin(A + B)$
-V	-V	$\overline{A + B + Cin}$	$\overline{A.B} + A.B + Cin$

We will simulate the ALU in full adder configuration @250MHz. Simulation result is given in Figure 5. Note that there is a voltage drop (100mV) related to the dissymmetry between the block consisting of NMOS and that of PMOS. This will be discussed in next section.

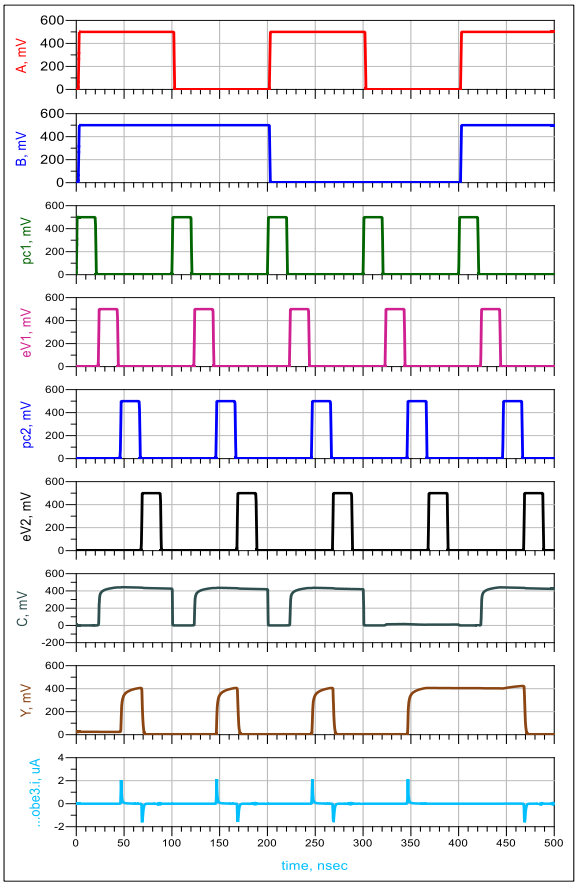

Figure 5. Simulation result

4. SIGNAL INTEGRITY ISSUES OF THE ACTUAL RECONFIGURABLE DG-CNTFET CELL

The actual implementation of the reconfigurable ALU based on DG-CNTFET [14] present some signal integrity issues which a serious barrier to real physical implementation can be. The following simulation result Figure 6 shows the high signal degradation especially if we use 500 mV power supply which is common value at modern technological nodes.

First implementations of this cell were @ 1V power supply which may explain why no major issues observed with cell because the electrical level loss still far from switching value. This signal degradation is due to the fact that n type transistors are poor Vcc provider and p type transistor are poor gnd passer. We can observe this effect especially in inverters where p type is always connected to Vcc and n type always connected to GND in order to avoid signal degradation. In figure 6 we can clearly see the degradation of output signal, the value is 400mV instead of 500mV.

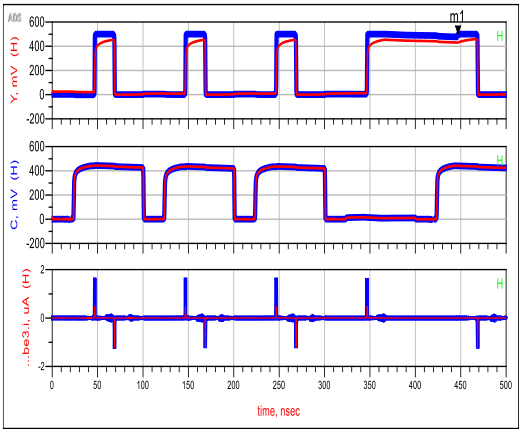

Figure 6. Signal integrity issues

Motivated by this observation, we have worked on possible solutions to resolve this issue and try to find a way to reduce the signal degradation. First and basic solution is to add buffer in output stage, but this solution increases the delay significantly. Then better solution consists to modify the architecture to ameliorate signal quality without affecting the delay and the density of circuit. These two solutions will be explained next section.

5. DESCRIPTION OF THE PROPOSED SOLUTION

In this work we will propose two possible solutions for this issue.

5.1. Buffers Insertion

First solution consists of inserting intermediate buffers between the different ALU stages. Those buffers composed by two successive inverters, will improve the quality of signal and amplify it. As 9T cell is the major sub-block of ALU we will use it to simulate and test this solution Result is shown in Figure 7.

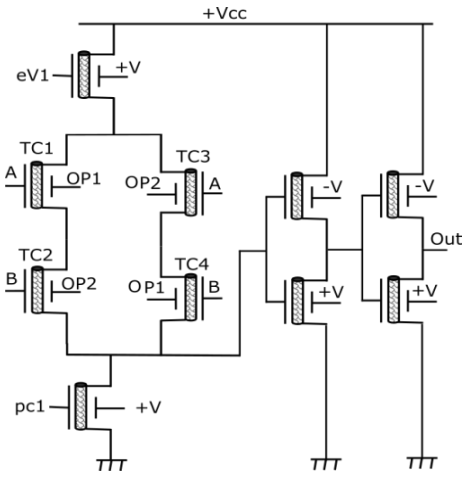

Figure 7. Proposed 9T stage with buffer stage added

Here is the result of buffers insertion just after the 9T block: We note clearly that 9T output without buffers is largely below 500mV, depending on logical state it's varying from 300 to 350 mV, of course these values are considered as a logical state High since they are higher than VDD/2= 250 mV but may decrease if we use higher load values. With buffer stage output signal is ameliorated and equal to 500mV now. However, this solution has one disadvantage, delay increase because we add two stages, so PDP is directly impacted.

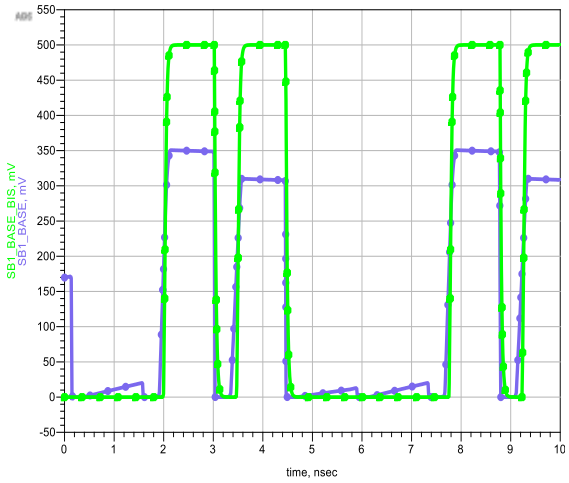

Figure 8. 9T block output with/without output buffer

5.2. Proposed Architecture Modification

The second solution proposed is to resolve the dissymmetry between NMOS (poor Vcc provider) and PMOS transistor (poor gnd passer). It consists to modify architecture so Vcc signal will be passed by PMOS transistor and gnd will be passed by NMOS transistor. Modification of the proposed architecture are:

a. EV1 transistor replacement with p type transistor to which needs of course an inversed control signal (which can be easily generated for the whole circuit).
b. Logical function transistors shadowing by a complementary type transistor with an inverted command of course.

This gives the new 9T cell described by Figure 9. By this modification, we can resolve dissymmetry between the block consisting of NMOS and that of PMOS. Simulation result in Figure 10 confirm. As shown in Figure 10, after modification output signal is ameliorated and its amplitude is equal to Vdd (Vdd=500mV). Figure 10 shows the proposed architecture of ALU including modification of 9T block. As shown in Figure 11, after modification output signal is ameliorated and value is equal to 500mV. This solution resolve signal integrity problem without deteriorating other performance (no impact on delay and power).

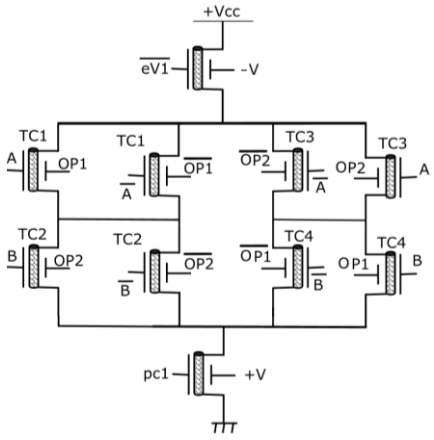

Figure 9. 9T cell Architecture modification

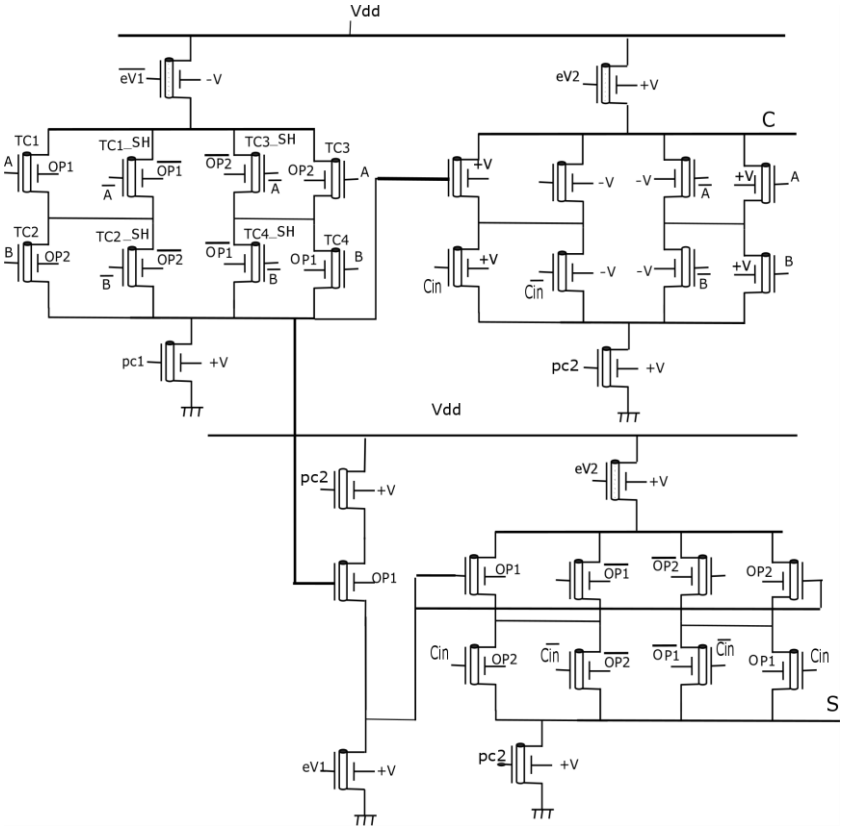

Figure 10. ALU proposed architecture

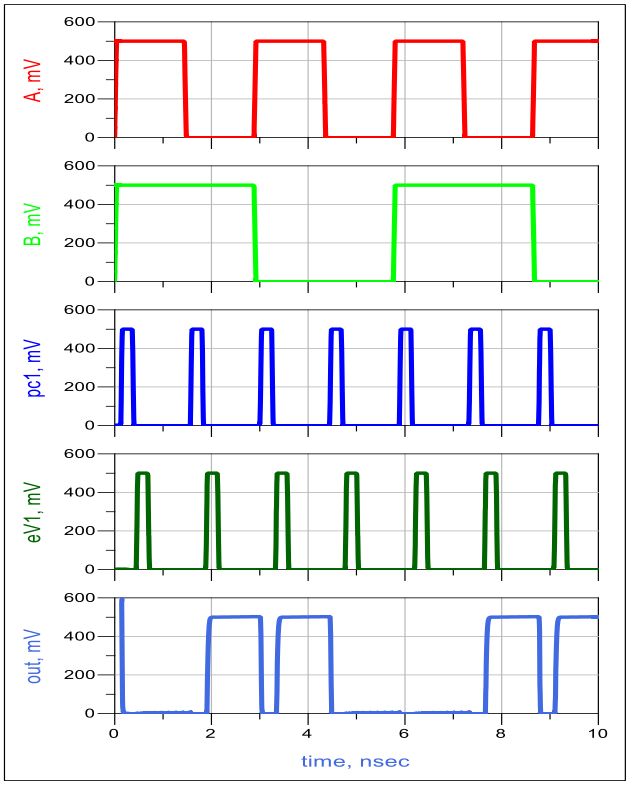

Figure 11. Simulation results of 9T block in XOR configuration with modified architecture

6. CONCLUSION

In this paper we have presented an improved reconfigurable ALU circuit using carbon Nano-tube field effect transistors. First an overview of CNTFET transistor is given and state of the art of DG-CNTFET based reconfigurable circuit is done. Then a signal integrity issue faced on those circuit is explained and simulated. This solution is proposed to resolve this integrity problem by modifying the architecture and propose a new one which give a significant improvement in signal quality. We showed that we can improve simulation result by using complementary type transistor with an inverted command without affecting the delay and the density of circuit.

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