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Design of a 60 GHz power amplifier in a 45nm CMOS

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ABSTRACT

This Paper presents a design and implementation of class-AB power amplifier which works at 60GHz unlicensed frequency band. This power amplifier uses a MOSFET from gpdk45 technology library. The design simulation is done by cadence Analog Design Environment. This proposed power amplifier yields a power added efficiency of 23.45% and a power gain S21 of 10dB at 60GHz. The output impedance of proposed power amplifier is needs to be matched with 73Ω antenna impedance. The S22 output matching of the simulated power amplifier is -18dB at 60GHz. The input side is matched to arbitrary impedance of 50Ω the resulting S11 of simulated result is noted to be -15dB at 60GHz. The proposed circuit has a noise figure of 3.85dB. The proposed circuit has a Pout-1dB of 8.5dBm. the designed class AB power amplifier is an important component in 60GHz transceiver. The layout of the associated circuit is drawn with the total size of 0.107um^2.

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1. INTRODUCTION

In the last few years we have seen an increased interest in millimeter-wave CMOS circuits and communication systems both in academic and industry research activity. The 60GHz frequency band finds attractive for mm-wave designers for world wide availability of unlicensed spectrum around 60GHz. Currently in the normal frequency bands the increasing number of wireless devices and their rising performance requirements, the usable frequency spectrum is very crowded. Large parts of the spectrum are licensed, and the allocated bands for specific applications require very advanced modulation techniques to enable high data transfer rates. Communication is also heavily encoded to reduce interference between different channels in the same band [1]. Advances in technology increase the useable spectrum by enabling wireless systems to utilize frequencies far into the GHz-range, at fairly low cost. The globally un-licensed 60 GHz band varies in some regions, as shown in Figure 1, but most of these regions have a total bandwidth of 7 GHz. This enables very high data transfer rates. Dependent on the modulation scheme, 7 GHz bandwidth is capable of tens of gigabits per second 3. Higher carrier frequency increases the free space path loss and the signal attenuation in materials. This means shorter transmission range and that the receiver should be in the line of sight from the transmitter.

These disadvantages are considered advantages in applications with short transmission ranges; high attenuation reduces the likelihood of interference of separate systems. Short range transmission is also less susceptible to eavesdropping since the receiver has to be fairly close to the transmitter. The short wavelength of 60 GHz (5 mm in vacuum), enables very small antenna dimensions. In some applications, the antenna can be integrated on chip, acquiring a remarkably small form factor of the wireless system. The feasibility of CMOS transceiver circuits at 60 GHz provides a platform for achieving low cost, highly integrated, high bandwidth, high data rate communication systems. In recent years, a number of 60 GHz CMOS building blocks and integrated receivers have been demonstrated. However, the low supply

voltage, thin gate oxide, low breakdown voltage, Lossy silicon substrate, and power gain-output power tradeoff of CMOS technology result in the millimeter wave power amplifier being the most difficult block to implement in CMOS. A number of 60 GHz CMOS power amplifiers employing different topologies have been reported to date, however the output power has been relatively low, limiting the amplifiers to short-range applications. It is increasingly important to use more efficient power combining techniques in order to increase the output power capability of power amplifiers in order to enable medium and long-range applications. This research aims at exploring the challenges facing the design and implementation of 60 GHz power amplifiers in standard 45 nm CMOS processes. The design, modeling, and layout optimization of both passive structures such as inductors, capacitors, as well as active devices operating at 60 GHz are investigated. Different power combining topologies for generating high output power from low RF power is presented. A Power amplifier is an electronic device that receives an electrical signal from the previous stage such as modulator and reprocesses it to amplify or increase its power output. RF Power Amplifiers are used in a wide variety of applications including Wireless Communication, TV transmissions, RADAR and RF heating. The basic block diagram of transceiver is as depicted in Figure 2 the power amplifier is the final active component in transmitter chain [2-4].

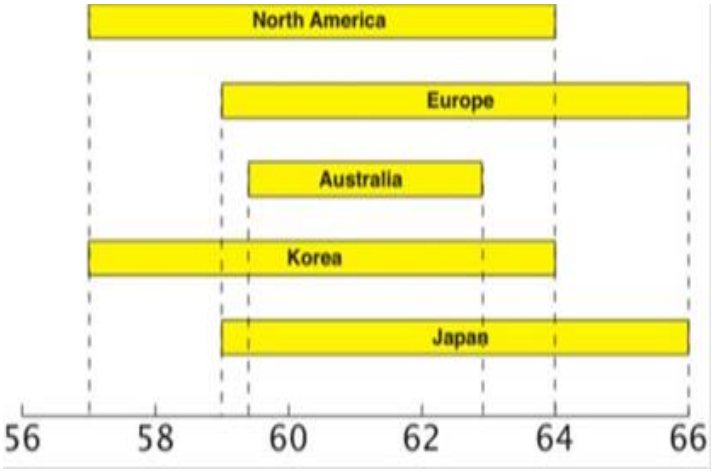

Figure 1. 60GHz frequency band

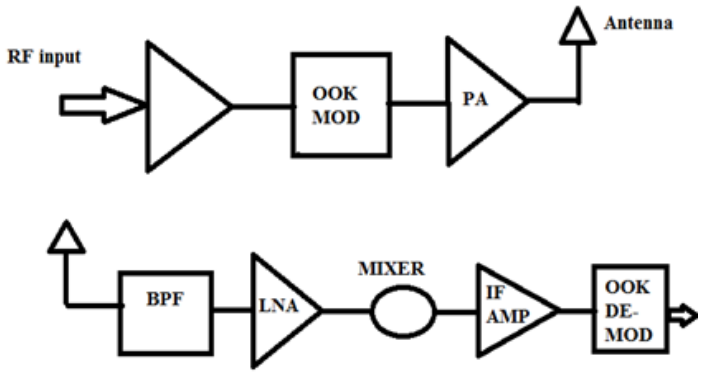

Figure 2. Generic block diagram of transceiver

Power Amplifier is part of the transmitter front-end and is used to amplify the signal being transmitted so that it can be received and decoded without error. The design of PAs, especially for linear, low-voltage operation, is still a difficult task. In practice, PA design has involved a substantial amount of trial and error, that is why discrete and hybrid implementations have traditionally been utilized. The main objective of designing a power amplifier is to achieve power gain, the output impedance of power amplifier need to be matched with the input impedance of antenna for maximum power transfer and finally the output impedance of previous stage need to be matched with input impedance of power amplifier [5, 6].

2. DESIGN METRICS FOR POWER AMPLIFIER

The main performance parameters for the power amplifier are the level of output power it can achieve, depending on the targeted application, linearity, and efficiency. There are two basic definitions for the efficiency of the PA.

2.1. Efficiency

Generally the efficiency is defined as the ratio of output parameter to the input parameter. In power amplifier there are basically two types of efficiency.

a. The drain efficiency: The drain efficiency is the ratio between the RF output power to the dc consumed power.

b. The power added efficiency(PAE): The power added efficiency is the ratio between the difference of the RF output power and the RF input power to the dc consumed power. PAE is defined by (1).

$$PAE = \frac{P_{RF,OUT} - P_{RF,IN}}{P_{DC}} \tag{1}$$

The PAE is a more practical measure as it accounts for the power gain of the amplifier. As the power gain decreases, more stages will be required. Since each stage will consume a certain amount of power, the overall power consumption will increase, thus decreasing the overall efficiency.

2.2. 1-dB Compression Point

This parameter quantifies the linear power handling capability of an amplifier. It is referred as signal power at which the small signal gain is compressed by 1-dB. If the signal power is output it is called as output 1-dB compression point(OP_{1dB}). If signal power is referred as input it is called as input 1-dB compression point (IP_{1dB}). The output and input compression points are related by (2).

$$OP_{1dB} = G + IP_{1dB}$$

2.3. Power Gain

Power Gain is defined as

$$G = \frac{P_L}{P_{in}} = \frac{power\ dissipated\ at\ load}{power\ delivered\ to\ input} \tag{2}$$

Transducer gain G_T is defined as

$$G_T = \frac{P_L}{P_a} = \frac{power\ dissipated\ in\ load}{power\ available\ from\ source} \tag{3}$$

Available gain G_A is defined as

$$G_A = \frac{P_{AT}}{P_a} = \frac{power\ available\ from\ two\ port\ network}{power\ available\ from\ source} \tag{4}$$

2.4.Linearity

The linearity issue existed depending the type of modulation scheme incorporated in modulation. In transmitter section if the amplitude modulation is incorporated then the power amplifier need to be linear region. In power amplifier the trade-off exist between efficiency and linearity. Assume that the input given to designed power amplifier is amplitude modulated wave($V_{in}(t)$), if the power amplifier is highly non linear in nature. Then output of the amplifier V_d is given by;

$$V_d = AV_{in}(t) = a_1 V_{in}(t) + a_2 V^2{}_{in}(t) + a_3 V^3{}_{in}(t) \tag{5}$$

This non linearity need to be minimized in amplitude modulated output for recovering the information present in the envelop of the output.

2.5. Adjacent Channel Power Ratio; ACPR

This specification parameter is in association with linearity. It is given by;

$$ACPR = \frac{P}{P(\Delta f)} \tag{6}$$

It is defined as the ratio of the power transmitted in the channel of interest to the power transmitted in the certain offset frequency.

2.6.Heating

Battery operation is one important reason for increasing power efficiency. The higher the efficiency, the longer the standby time and talk time. Along with these issues one more important reason to improve up on optimal efficiency is the heating problem. The maximum output power is not limited by heat it can dissipate. The ratio of output power to the heat it can dissipate is$\frac{\eta}{1-\eta}$. If a transistor is able to dissipate 1W power safely, then class A PA can output a power of 0.53W. if class C PA is chosen then it can output 3W output power at same heating. It is clearly demonstrates that compared to class A, class C can produce highest output power. The thermal resistance is defined as

$$\theta_{JC} = \frac{T_j - T_c}{P_{diss}}$$

whereT_j is maximum junction temperature, T_c is case temperature.

In designing a power amplifier, the designer has to choose the number of stages, the operating class of each stage, determine the optimum load of the output stage, and decide whether to use differential or single ended structure. These issues depend on the used technology, the kind of modulation (constant envelope or non constant envelope technique) and whether the amplifier will be integrated with the whole transceiver or will be on a separate chip.

3. TRANSISTOR MODEL

In RFIC's design transistors are normally biased at a constant drain current density. The transistor's power consumption normally a resultant of current and drain-source voltage V_{DS}. Further VGS is applied to achieve desired current density and it has no effect on dissipated dc power.

3.1. Testing Accuracy, Precision, and Recall

To characterize transistors RF performance at a chosen bias point following figure of merit are employed.

a. Cut-off frequency f_T
b. Maximum oscillation frequency f_{max}

An evaluation of f_T and f_{max} performance for selected MOSFET from gpdk45 library. Figure 3 depicts the f_T is plotted against different gate-source voltage Vgs. Figure 4 shows the current density is plotted against cutoff frequency f_T. This plot ensures the maxima of fT is achieved for a current density ofmA/um. This proves the selected MOS can yield a low power consumption and high frequency gain.

Figure 5 shows the simulated DC transfer characteristics of a nmos1v n-channel MOSFET with L=45nm gate length. The graph depicts the pinch-off voltage of MOSFET is around 250-280mV. Figure 6 output characteristics of 45nm nmos1v n-channel MOSFET based on the simulation using gpdk models. Here to bias the power amplifier in class AB configuration it need to be biased at Vgs=0.4V and Vds=1V which yields a current density of 500uA/um.

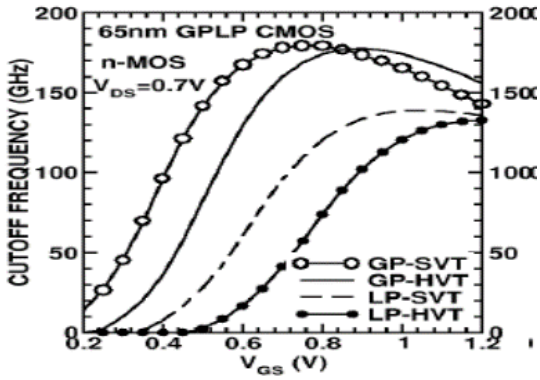

Figure 3. f_T versus gate source voltage

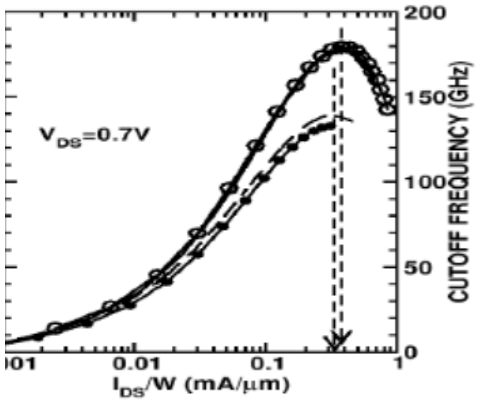

Figure 4. Current density versus cut-off frequency

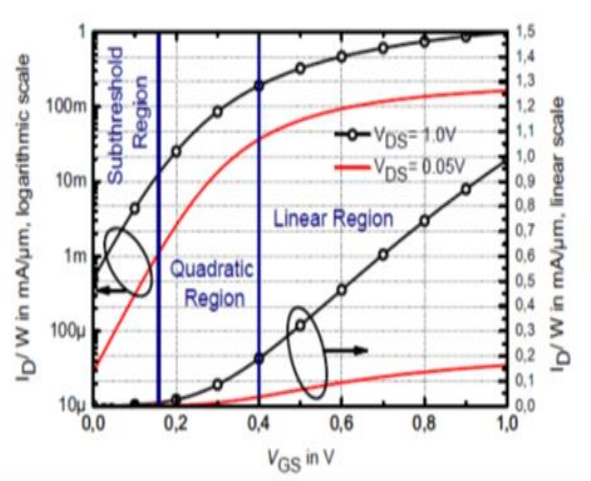

Figure 5. Normalized DC transfer characteristic of 45nm nmos1v n-channel MOSFET based on simulation using gpdk models

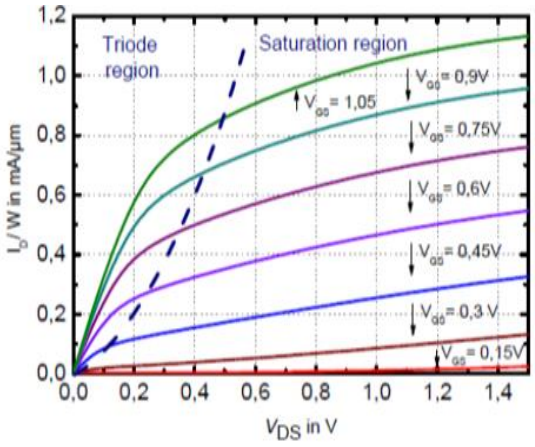

Figure 6. Output characteristics of 45nm nmos1v n-channel MOSFET based on the simulation using gpdk models

4. PROPOSED METHODOLOGY

The general design process of proposed power amplifier is conceptualized as depicted in Figure 7. In section 3 DC biasing issues were addressed for designing class AB power amplifier for low power dissipation. The circuit diagram of proposed class AB power amplifier without dc biasing circuit using nmos1v n-channel gpdk45 model file is shown in Figure 8.

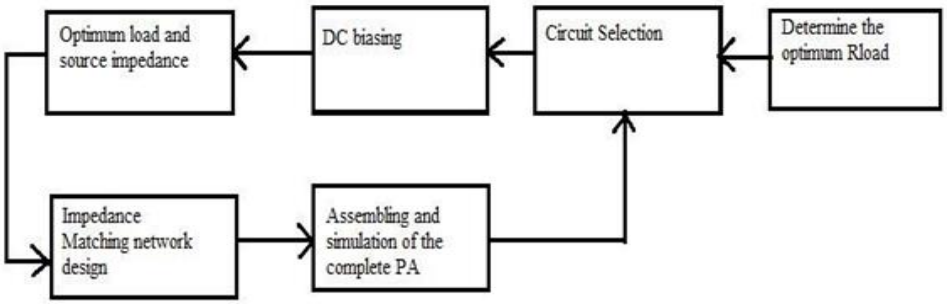

Figure 7. Design processes for power amplifier design

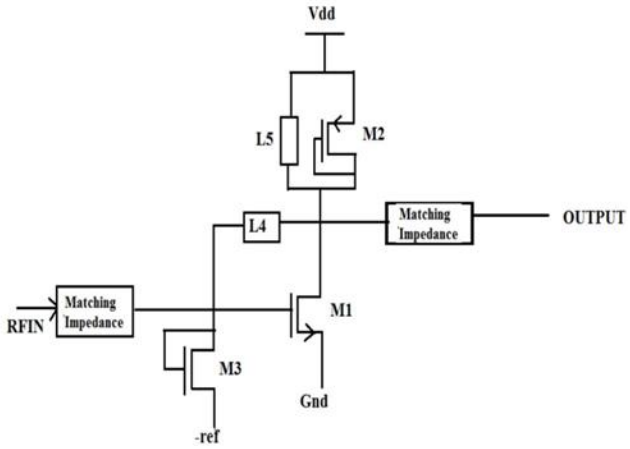

Figure 8. Proposed class AB power amplifier (without dc biasing)

The circuit diagram of Class AB power amplifier is depicted in Figure 8 for the unlicensed frequency of 60GHz. It endures three FETs namely M_1, M_2, and M_3.The proposed PA comprises of common source driver stage proceeded by tank circuit. This anatomy shows better results operating at 60GHz with matching input and output impedance. The input side of the power amplifier is matched to an arbitrary impedance of 50ohms and output side is matched to antenna impedance of 73ohm. In the interest of minimizing DC voltage drop and to elevate the AC gain of the amplifier a tank circuit is used which embodies L5 and M2. Transistor M_1 is biased in saturation region to work as a current device by delivering a large value of current. The selection of biasing voltage is decked accordingly to the necessary circumstances for operating in Class AB. The common source configuration induces high gain which is entailed for the amplifier. The large input AC signal (V_{in}) is given to transistor M1 then the output (V_{out}) is drawn from the drain of M1 and tank circuitry respectively. Since silicon Metal oxide semiconductor is an imperfect current drive mode of production, where it can modify the performance of circuit either by increasing the amplitude of the input signal or by decreasing the device area. Impedance matching at input becomes very predominant at high frequencies; the signal might fairly reflect back in future from load to source if matching happens.

The input impedance matching circuit for the proposed circuit comprises of L1, L2, L3, C1, C2, and C3. The detailed matching network is as depicted in figure. Finally an input matching network is assimilated for maximum power transfer (dBm). The output matching is a simple L network to address the area issue of power amplifier. Performance parameters of PA such as gain, efficiency, linearity. Substantial bypass capacitors are used to isolate bias circuit and supply. C1 is the coupling capacitor at the input stage. The MOSFET M3 can operate as the diode connected resistor if the gate and drain of MOS are shorted. The resistance of diode connected load M3 is equal to 1/gm. The small signal model of nmos1v MOSFET from gpdk45 technology at radio frequency is shown in Figure 9.The input and output matching network is shown in Figures 10 and 11 respectively.

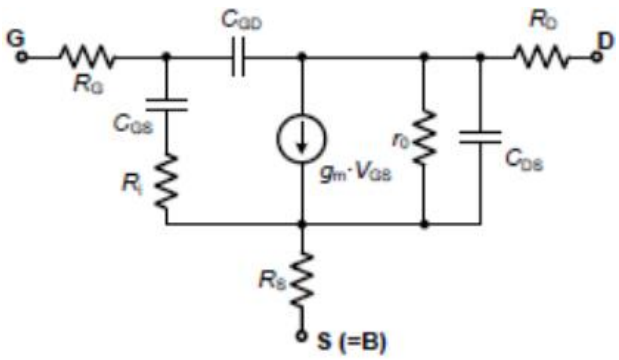

Figure 9. Small signal model of nmos1v MOSFET at RF

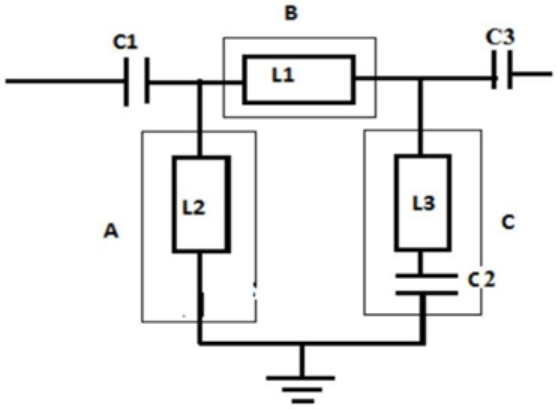

Figure 10. Input matching network

In designing amplifier the flexibility given to designer is input and output matching. The input side should be matched to source and output side is matched to load in order to deliver maximum power to load. Once the input and output matching network is designed the reflection coefficient at each port is correlate to the complex conjugate as shown in (7) and (8).

$$\Gamma_{IN} = \Gamma_S^{\ *} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \tag{7}$$

$$\Gamma_{OUT} = \Gamma_L^{\ *} = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \tag{8}$$

To get minimum noise Figure using transistor the power reflection coefficient should match with $\Gamma_{out}^{\ *}$ and load reflection coefficient should match with $\Gamma_{out.}$

$$\Gamma_s = \Gamma_{opt}$$

$$\Gamma_L = \Gamma_{out}^* = \left(S_{22} + \frac{S_{12}S_{21}\Gamma_s}{1 - S_{11}\Gamma_s} \right) \tag{9}$$

The overall performance of power amplifier is determined by calculating GT. The proposed power amplifier MOSFET works at a power supply voltage of 1.8V. It is designed to deliver a output power of 10mW. It ensures the P1dB of 11.7dB and Γ_{opt} of 0.815+j0.2209. The stability of the design is ensured with the equation given (10) and (11).

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}||S_{21}|} = 1.57 > 1 \tag{10}$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} = 0.19 < 1 \tag{11}$$

The equation for K and Δ ensures the unconditional stability of the circuit. From the figure it arbitrary assumed that the current density considered for class AB power amplifier is 450uA/um. To enhance the gain and maintain the P1dB and noise figure number of active amplifying stages are increased. For output matching a simple L shape network is designed. The output impedance of power amplifier is given by;

$$Z_{out} = r_0 \parallel Z_m \parallel Z_t \parallel Z_{para} \tag{12}$$

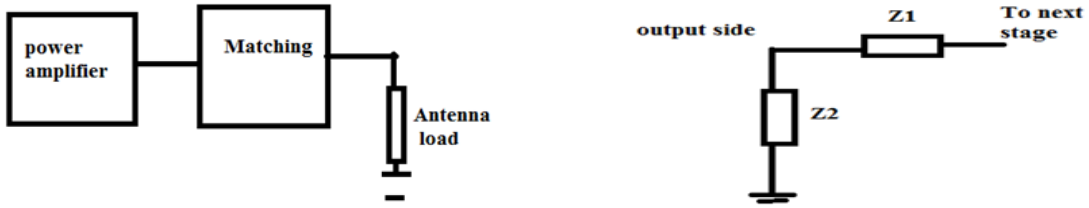

Figure 11. Output matching network

To match this impedance to antenna load impedance the following LC components are tabulated in Table 1.

Table 1. LC Components Output Matching

L	C
80PH	5fF
125PH	8fF

5. SIMULATION RESULTS

The simulation of proposed power amplifier is done by using 45 nm CMOS technology using Cadence virtuoso.

5.1. S-parameter Analysis

The abbreviation S refers to scattering. Throughout the high frequencies, it is favorable to construct a given network in terms of microwaves than with voltages or currents. In occurrence, if we have 2 ports, then S11, S12, S21 and S22 represents input voltage reflection, reverse voltage gain, forward voltage gain and output voltage reflection respectively. S-parameters interpret the input-output analogy in the midst of ports in an electrical system. S11.

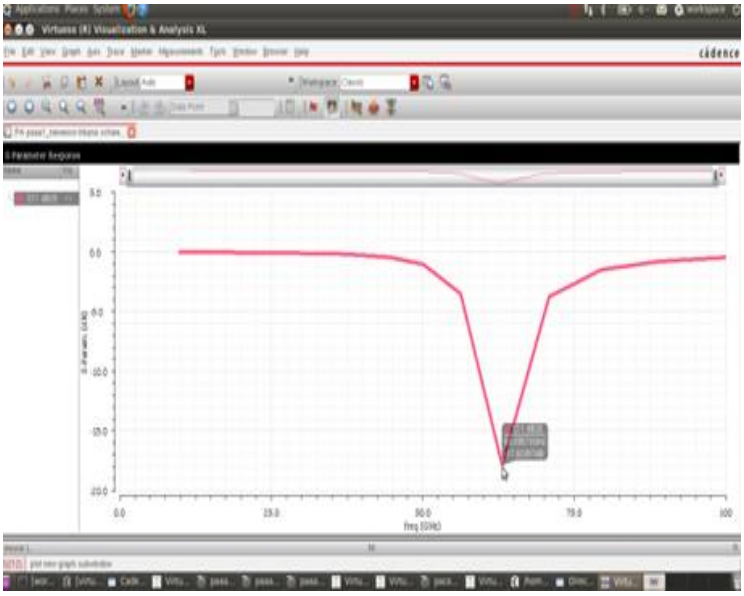

Figure 12. Simulation result of S11

Expresses power echoed from the antenna, Accordingly the input return loss (S11) simulated is-18dB at 63GHz as depicted in Figure 12. Through designing input matching circuit foolproof maximum S11 can be accomplished. Extended with the above framework, the proposed PA attains an average gain S21 of 10dB at 63GHz which is recognized as forward transmission coefficient. Is depicted in Figure 13.

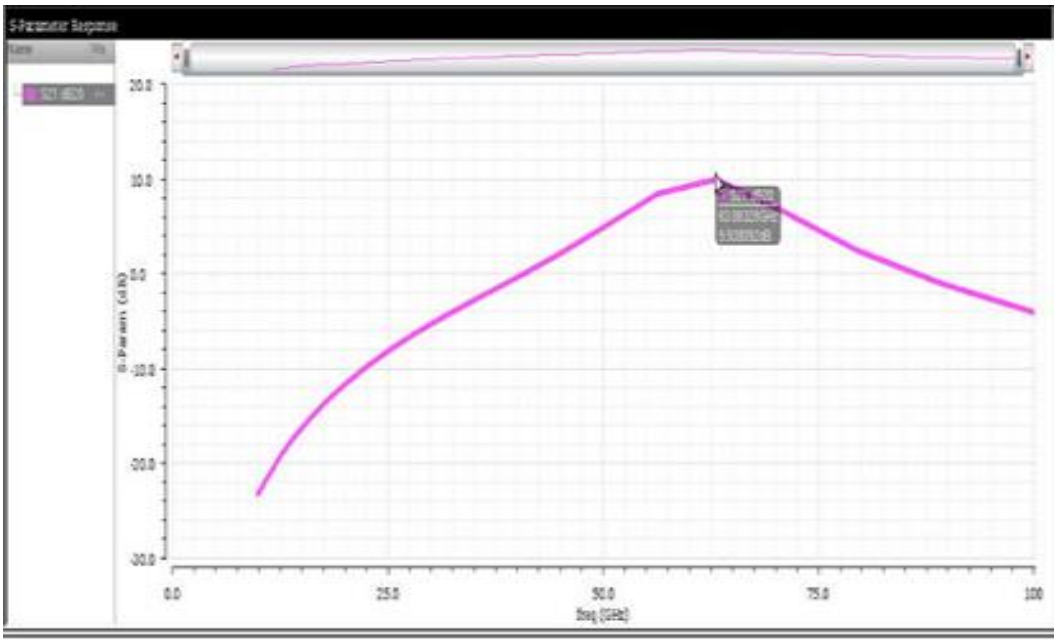

Figure 13. Forward gain S21

5.2. Power Analysis

5.2.1.PAE

Power added efficiency is the efficiency of the network to convert input dc power in to output power with additional RF power the analogous exterior plot of PAE is given in Figure 14. For the proposed PA the achieved PAE is about 23%.

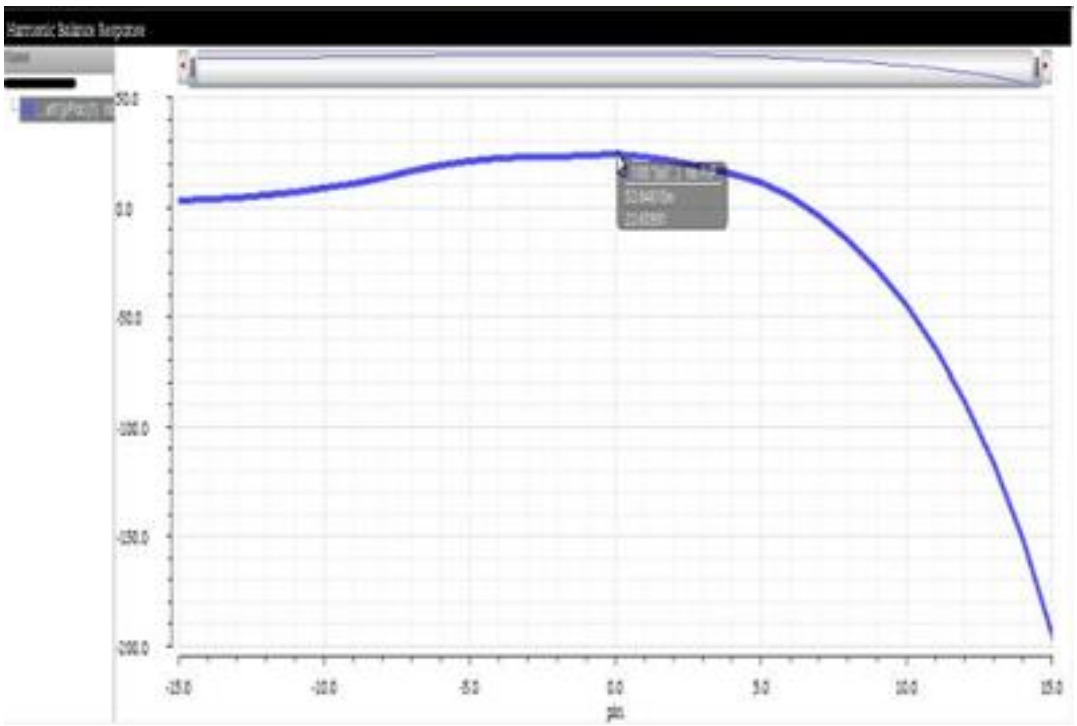

Figure 14. Power added efficiency output

5.2.2. Power Spectrum

The proposed power amplifier produces an moderate power at the designed frequency as shown in the Figure 15.

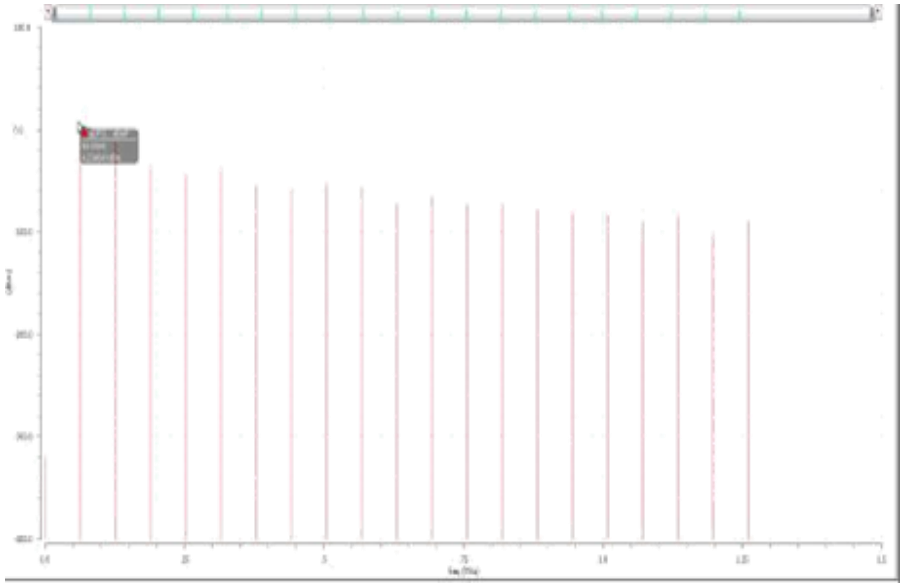

Figure15. Plot of power

5.2.3. Power Gain

It is the ratio of the power delivered to the load to the power input. The sole input and output circuits have been weighed for the load powers. They occasionally designate to be the ratio of the signal amplitude or power at the output port to the amplitude or power at the input port. They are frequently indicated using the logarithmic decibel (dB) units ("dB gain") of 4dBm has been achieved as shown in the Figure 16.

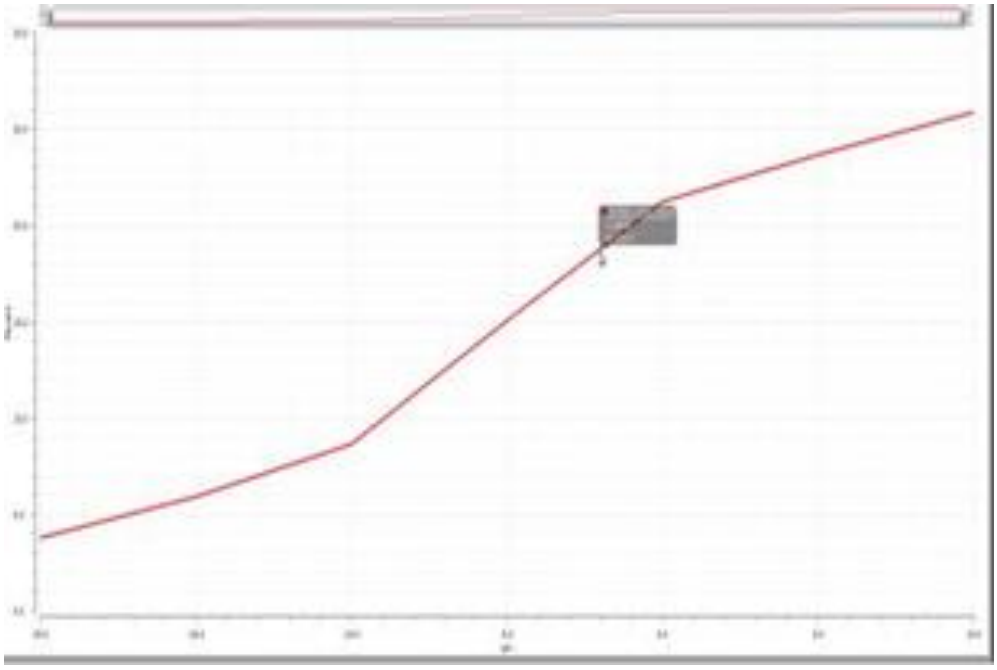

Figure 16. Plot of power gain

5.2.4. Total Harmonic Distortion

The total harmonic distortion, of a signal is a survey of the harmonic distortion present. This refers to the aggregate of all harmonic components of voltage waveform correlated across the fundamental components of voltage waveform.The plot of total harmonic distortion is shown in Figure 17.

$$THD_F = \frac{\sqrt{V_2^2+V_3^2+V_4^2+---}}{V_1} \quad (13)$$

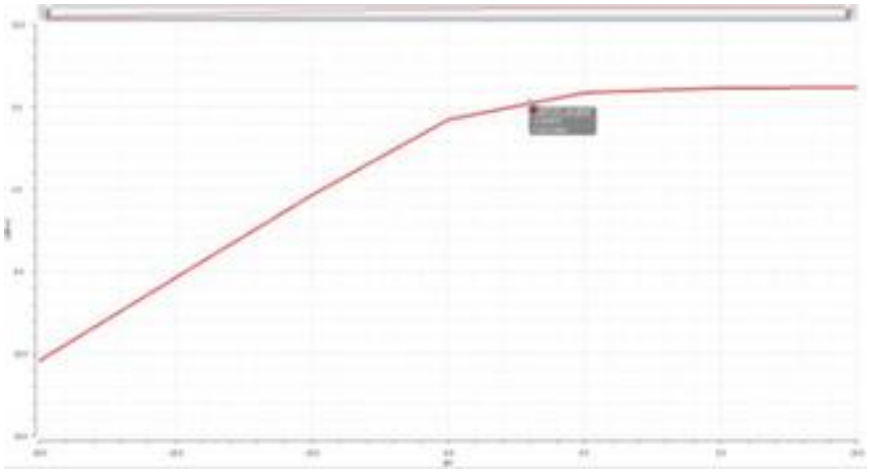

Figure 17. Plot of THD

5.3. Transient and AC analysis

A transient phenomenon is a fleeting eruption of endurance in a arrangement elicit by a quick transformation of state. Transient Analysis is used to have the glimpse of input and output with respect to time. For the proposed PA a phase shift can be scrutinized which is depicted in the Figure 18. Through, AC analysis the circuit bandwidth, low cut off frequency, the gain, the role-off can be realized through this analysis. The output can be achieved by engaging AC supply to the proposed circuit. The tuned frequency response which is in the range of 56GHz has been achieved as shown in the Figure 18. Finally the proposed PA is unconditionally stable over the range of 60GHz.

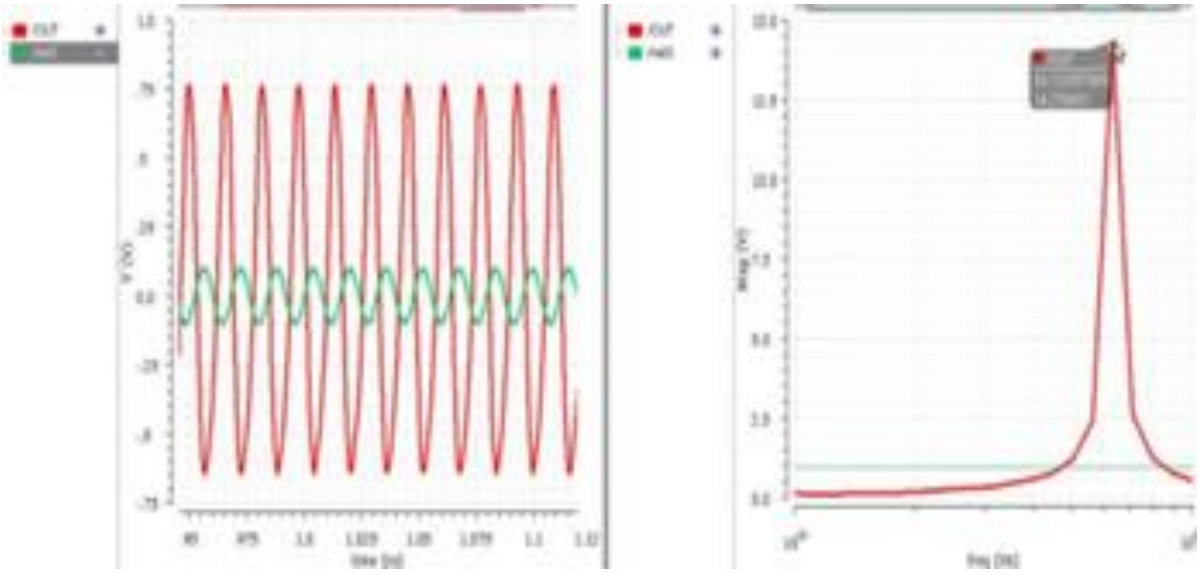

Figure 18. Plot of Transient and AC analysis

5.4. Efficiency

The efficiency of the PA plays an critical part in wireless communication. In the mathematical terms it is defines to be the ratio of output to the total input accessed. The following equation can be used to determine efficiency,

$$\eta_{max} = \frac{2y - \sin(2y)}{4[\sin(y) - y\cos(y)]} \quad (14)$$

Since, the achieved efficiency of the proposed circuit is between 50% to 75%, thus the proposed circuit can be claimed as Class- AB power amplifier. This is shown in the Figure 19.

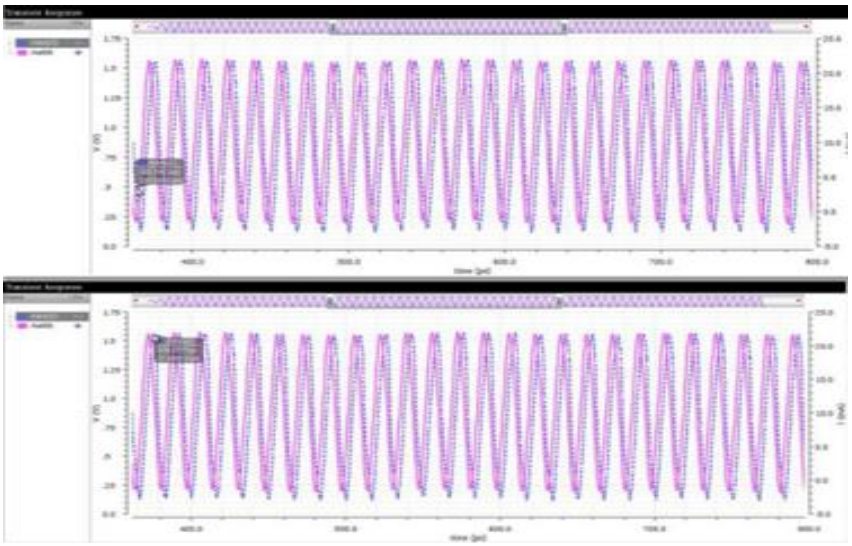

Figure 19. Efficiency of class AB power amplifier

5.5. Layout

Figure 20 shows the layout of the proposed PA using cadence virtuoso layout editor in 45nm technology. The die area of the proposed PA occupies 0.1075µm^2.

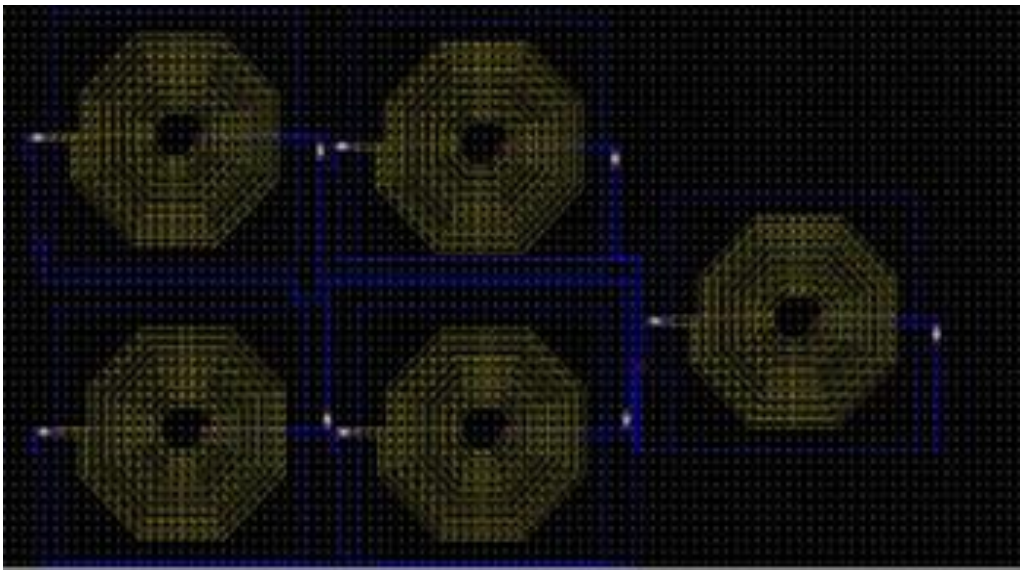

Figure 20. Layout of PA

6. CONCLUSION AND FUTURE SCOPE

A class AB power amplifier of frequency 60GHz is designed and implemented with software 45nm Cadence Virtuoso. The results show that the gain with 10dB. Even with few deviations exist and the work needs further improvement in the future, so that it can be applicable for other application requirements. Table 2 shows comparision to recently published pa.

Table 2. Comparision to Recently Published pa

Ref	Tech (nm)	Frequency (GHz)	Gain (in dB)	PAE_{max} (%)	Area (in mm^2)	Vdd(v)
[1]	130	40-65	18.8	15.7	1.02	-
[2]	65	60	11	16.3	0.0675	-
[3]	65	55-65	21	14	0.675	-
[4]	65	60	12.1	11.1	-	-
[5]	65	60	23.2	16.3	0.611	1.2
[6]	65	60	24.5	12.8	0.7	1.2
This work	45	60	10	23	0.107	1

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