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A Power Efficient Self Biased OTA Design based on g_m/I_D Methodology with Considering Load Variation, Temperature Variation and Power Supply Variation

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ABSTRACT

The present work addresses the design of power efficient fully self biased OTA using a design methodology based on the g_m/I_D transistor characteristics. This analog module was analyzed, designed and prototyped in TSMS 0.35μm CMOS technology. Simulation results are presented, in order to validate the methodology. The OTA has Gain of 41.35 dB and 3db bandwidth of 138.73 kHz and the UGB of 12.40MHz with the current consumption of 65.50 μA. The circuit does not have need of any DC external biasing circuit, only need to apply VDD (3.3 V). Here self biasing has been introduced with power consumption of 216.15μW. The results have been taken with load variations, temperature variations, and power supply variations. This circuit used in real time high frequency applications as in RF communication.

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1. INTRODUCTION

The development of ultra-scaled VLSI technologies, coupled with the demand for more signal processing integrated in a single chip, has resulted in a tremendous potential for design of analog circuits. Most VLSI systems require analog sub-systems such as amplifiers, comparators, filters, oscillators, digital-to-analog and analog-to-digital converters. Most often the target technology process imposes design tradeoffs, some of them taken based on designer's experience with the target technology to achieve a successful analog design. More critical in deep sub-micron CMOS mixed-signal ICs are the specifications of analog circuits that are sensitive to the random variations of the size and technology parameters. This work focuses on the analysis, design and implementation of a low power OTA using the g_m/I_D design method [1]. In this method, we consider the relationship between the g_m/I_D ratio and the normalized drain current I_D/(W/L) as a fundamental design information to explore in the design space. In several analog blocks [2, 3], including the Gm-C filter [4], were designed using this methodology. Preliminary simulation results shows that a conventional design approach (using first-order Spice level 1 transistor models) achieves a similar performance with similar area, hence incurring in much larger power dissipation than that obtained in the g_m/I_D design method. The process parameters were obtained through the library files of TSMC 0.35μm CMOS technology [5]-[10].

2. SELF BAISED OTA ARCHITECTURE

Self biased circuit is the circuit in which there is no need of any external biasing circuit at any stage; means we made circuit in such a way that it take the biasing voltage from any node of the present circuit. Self Biased Circuit is able to bias its output to an equivalent bandgap voltage without using any external voltage reference or extra pin. A self-biased architecture which has an operating point independent of the process technology and environmental variations hence rendering a more robust design [11], [12]. The self-biased architecture also gives a constant ratio of the bandwidth to reference frequency and a constant damping factor. These ensure the stability of a OTA while at the same time keeping the phase noise low across the entire reference frequency range [13]. Fixed bias circuits get their bias voltages from independently designed reference voltage sources (or even something as simple as a voltage divider). Often in that case the bias may be left for the end-user to give some control over the operation point of the circuit. Self biased circuits get their bias voltages from the circuit itself often in the form of a negative feedback. This is very useful when a circuit is extremely sensitive to bias points and it becomes impractical to provide external biases that are correct to very high accuracies. This can happen in high gain amplifiers with very high impedance output nodes such as a common source amplifier with an active load [14], [15]. The operation of the circuit depends on the bias of the active load. It would therefore be desirable to sacrifice some of this gain by providing a negative feedback from the output to the gate of the active load. This way you would not have to bias the circuit yourself but will lose some of the gain of the circuit as a price. This is one of the trade off of analog circuits [17]-[19]. The circuit for self baised OTA is shown in Figure 1.

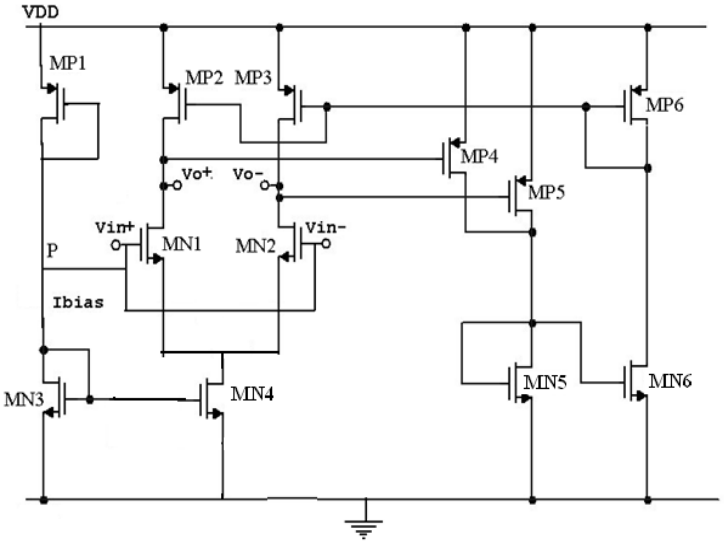

Figure 1. Self biased OTA

The biasing for the input transistors MN1 and MN2 are provided by the drain terminal (node P) of MP1, there is no need of external biasing circuit is required for operating this OTA. Here, there is only need to apply AC input. Designing is in such a manner that the voltage at point P is 1.6534volt. Here MP1 is using also as a current source for providing current to MN3 and which is mirroring in MN4.

3. DESIGN IMPLEMENTATION OF OTA

Considering the OTA design specifications and the chosen OTA architecture, the transconductor was designed using the g_m/I_D methodology [20]-[25]. For each transistor, the g_m/I_D factor is chosen, and then the normalized current I_D/(W/L) is determined for each transistor from the g_m/I_D vs. I_D/(W/L) curve for the target technology. Then, with the drain current value found, the W/L of each transistor can be obtained. The complete design procedure is demonstrated as follows:

a. Considering SR specification, the bias current is determined:
   Ibias ≥ SR.C_L, Ibias →=75µA;
b. From the transconductance gain requirement of 35 dB and I_{D1}=12.5µA, the g_m/I_D ratio of the NMOS differential pair (MN1-MN2) can be determined:

$(g_m/I_D)_{N1}=(g_m/I_D)_{N2}=5 \rightarrow (W/L)_{N1}=(W/L)_{N2}=1.29$;

c. The current mirror transistors (MN3-MN4) are operated in strong inversion to guarantee
d. good matching and noise properties. Thus we choose:
$(g_m/I_D)_{N3}=(g_m/I_D)_{N4}=1.70 \rightarrow (W/L)_{N3}=(W/L)_{N4}=0.5$;
e. The load transistors (MP2-MP3) should also operate in strong inversion :
$(g_m/I_D)_{P2}=(g_m/I_D)_{P3}=9.09 \rightarrow (W/L)_{P2}=(W/L)_{P3}=7.50$;
f. For the CMFB circuitry (MP4, MP5, MP6, MN45, MN6), to guarantee stable bias conditions we have: $GWB_{CMFB} \geq GBW_{M1,M2}$. Thus,
$(g_m/I_D)_{P4,P5}=2$, $(g_m/I_D)_{P6}=3.5$ and $(g_m/I_D)_{N5,N6}=2$;
g. Here transistor MP1 provides the biasing voltage of 1.65 V at input and giving the bias current of 75 µA, the value of $(W/L)_{P1}=1.43$

Figure 2 shows OTA implementation. The required plots for obtaining the values of (W/L)'s from g_m/I_D Methodology are giving in the Plots Figure 3 and Figure 4.

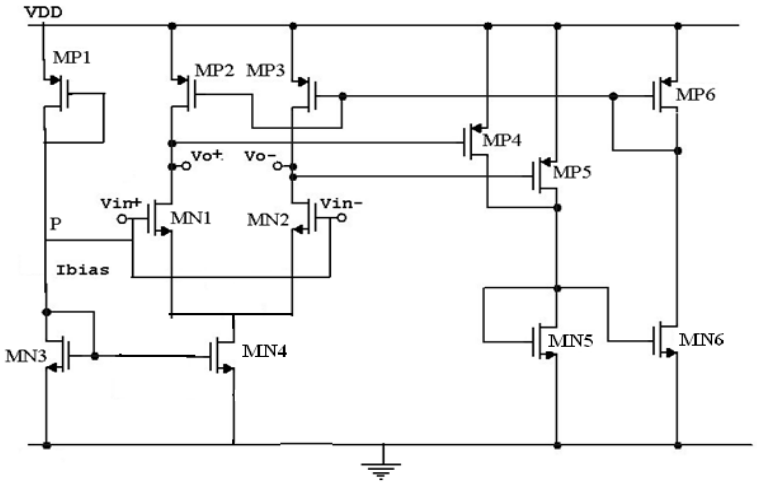

Figure 2. OTA implementation

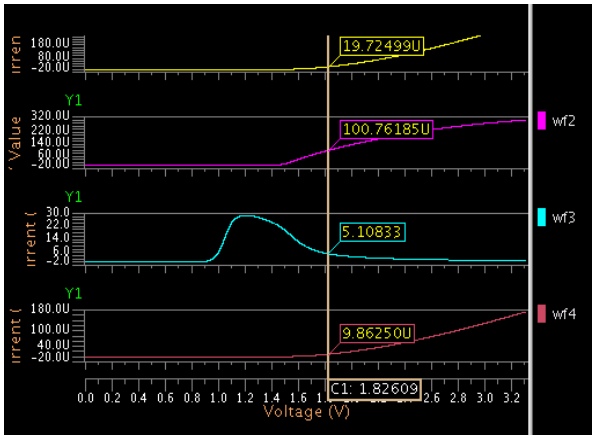

Figure 3. Getting the value of MN1, MN2

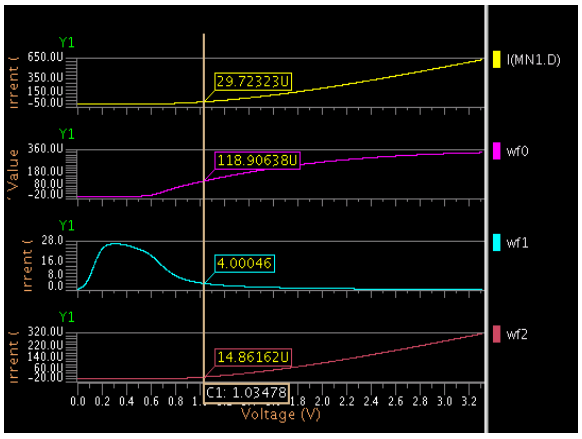

Figure 4. Getting the value of MN3, MN4

By the same way the values of all (W/L)'s have been gotten. The designed values for the transistors sizes are shown in Table 1 after iterations. Here after iterations the circuit have made circuit in such a way that the DC voltage of output node of the first stage is on 1.65 V. This will provide a DC input to the next OTA stage.

Table 1. OTA transistor dimensions obtained through the design methodology

Name of Transistor	(W/L)
MN1, MN2	71.3
MN3, MN4	0.714
MN5, MN6	0.714
MP1	1.428
MP2, MP3	1.285
MP4, MP5	0.714
MP6	2

The fully self biased OTA was then implemented according to the topology showed in Figure 3. All transconductors operate with one common bias generating circuit, which improves the matching between the OTA's stage.

4. LAYOUT

4.1. Analog Layout

When low-level or high-precision circuitry is being designed, a lot of care is usually given to the details of the circuit schematic and how the signal runs are routed. In layouts for digital circuits, the speed and the area are the two most important issues. In contrast, the layout for analog circuits, everything should be considered simultaneously [26]. In addition to the speed and the area, other equally critical considerations should be taken into account. In analog layout more care has to be given as the circuit performance changes drastically due to noise, mismatches, crosstalk and shielding required to protect critical nodes from being disturbed [27]. Without proper layout, the mismatches and the coupled noise would be quite large and would significantly degrade the performance of the amplifiers [28].

4.2. Layout of OTA

Due to huge aspect ratio, some transistors are divided into multiple fingers [29]. Figure 5 shows all the transistors with fingerings. Aspect ratio of MN1 and MN2 is 100/1.4. Since $100=2\times 50$, so a single transistor is divided in to 2 fingers with width of 50µm. There is no need to make fingers of other transistors of OTA, because sizes of these transistors are very small.

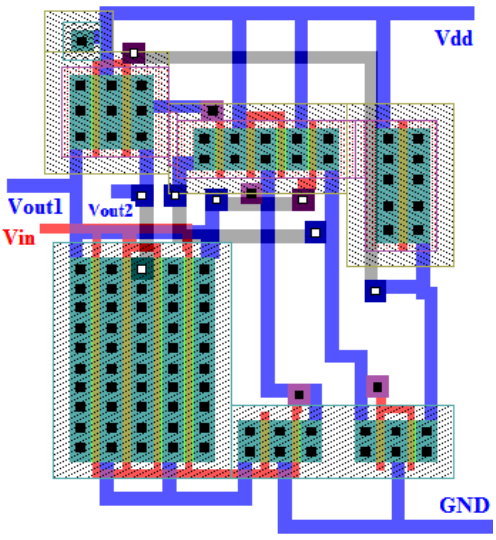

Figure 5. Layout of OTA

5. SIMULATION AND RESULTS

In this Chapter the schematic of the circuit has been simulated for various parameters. All values have been measured at load capacitance of 3pF. Prepared circuit of OTA is simulated at Tanner, T-SPICE tool at 0.35µ technology. This OTA is to be powered from a 3.3 volts power supply and with a power dissipation of 216µW. The current sources/sinks required for biasing are used from output stage.

Based on the OTA, input stage is fully self biased, an OTA has been designed. The simulations include AC response, Transient analysis, DC Response. The responses have been checked for temperature variation, Load capacitance variation and power supply variation. There is no need to give any DC at the input because this circuit is fully self biased that's why there is no need to make any biasing circuit.

5.1. AC Analysis:

On applying AC of 10 mv and DC of 0 V at input terminal of designed filter. (Here VDD is 3.3V with respect to ground). Figure 6 shows AC Analysis for OTA. The netlist and the simulated AC results for the gain (magnitude in dB) with respect to frequency(Hz) has been plotted by using TSMC 0.35µm on T-SPICE tool (Tanner), is given in Figure 7. From Figure 7 plotted waveforms, the following parameters have been obtained as in Table 2.

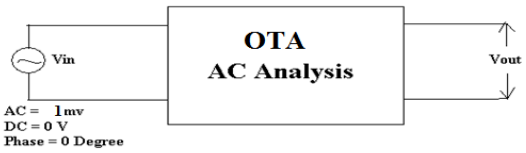

Figure 6. AC analysis for OTA

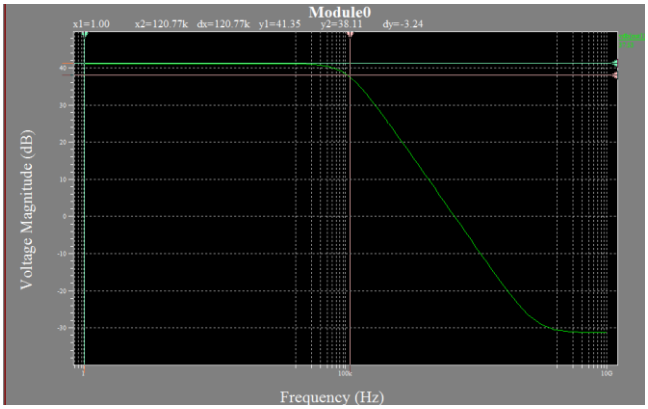

Figure 7. Plotted AC response of OTA

Table 2. Obtained Parameters for AC Analysis

Gain	41.35 dB
3dB Bandwidth	138.73 kHz
UGB	12.40 MHz
Power Dissipation	216.15 µW

5.2. Transient Analysis

For observing the transient response of the filter the test setup of Figure 8 must be used. In this setup sinusoidal signals are applied to the two inputs and the effective value of input signal is the difference of the voltage at the two terminals. No DC potential is applied along with the sinusoidal signal because the circuit is fully self biased.

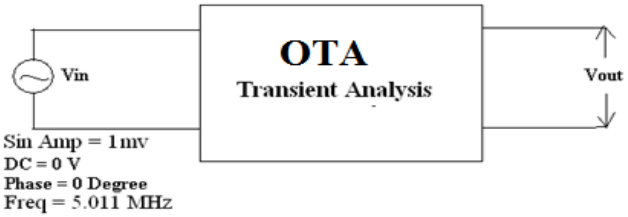

Figure 8. Transient analysis for a OTA

The simulated transient results for the magnitude in volt with respect to time (sec) have been plotted in Figure 9. On applying the input voltage peak to peak of 1mv, output voltage peak to peak of 220mv has been obtained. Here max voltage swing is 1.72V and min voltage swing is 1.50V. The simulated transient results for the magnitude in volt with respect to time (sec) have been plotted in Figure 9. On applying the input voltage peak to peak of 1mv, slew rate of 9.992 µs has been obtained.

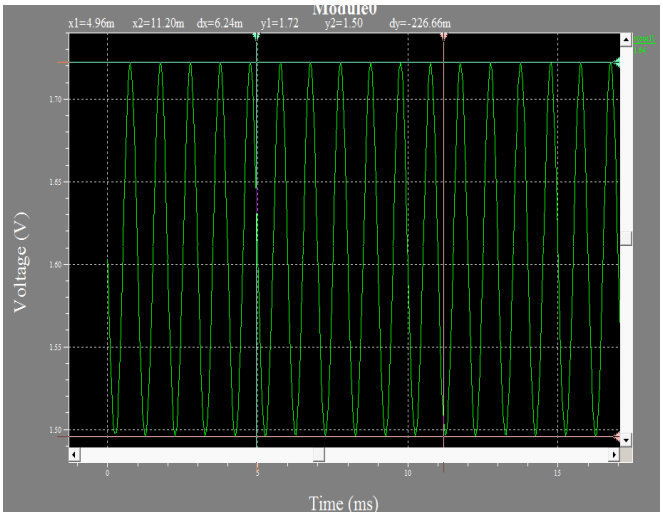

Figure 9. Simulated transient responses

5.3. DC Analysis

The main response of this circuit is the DC response. As no biasing voltage at the input is used, single voltage source i.e. power supply (VDD) provides the necessary DC voltage at the input. Here the voltage of every node is almost equal to 1.65 volt.

a) DC Value of V_{OUT1}

The voltage of node VOUT1 is plotted in Figure 10, when the value of VDD is 3.3 volt, then on this value, the voltage at node VOUT1 is 1.61 Volt.

b) DC Value of VOUT2

The voltage of node VOUT2 is plotted in Figure 11, when the value of VDD is 3.3 volt, then on this value the voltage at node VOUT2 is 1.61 Volt.

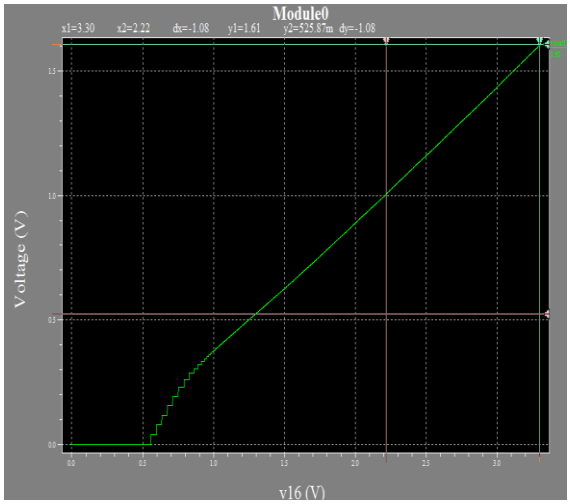

Figure 10. Voltage of Node VOUT1

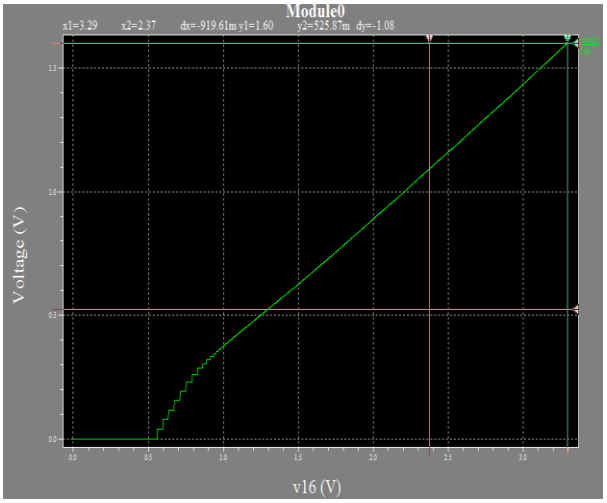

Figure 11. Voltage of node V_{OUT2}

5.4. Load Variations:

On applying different values of load capacitance differences in all the achieved parameters have been obtained. The achieved parameters have been plotted in the following figures for three different (2.5 PF, 3 PF, 3.5 PF) values. From Figures 12, 13 and 14 plotted waveforms, the following parameters have been obtained as in Table 3.

At C_L=2.5 PF

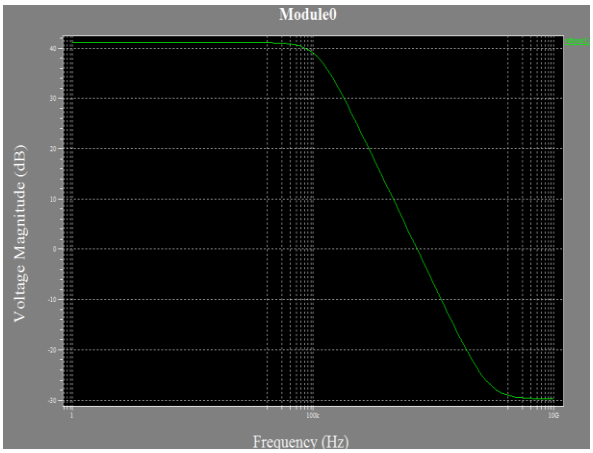

Figure 12. AC Analysis at C_L=2.5 PF

At CL=3 PF

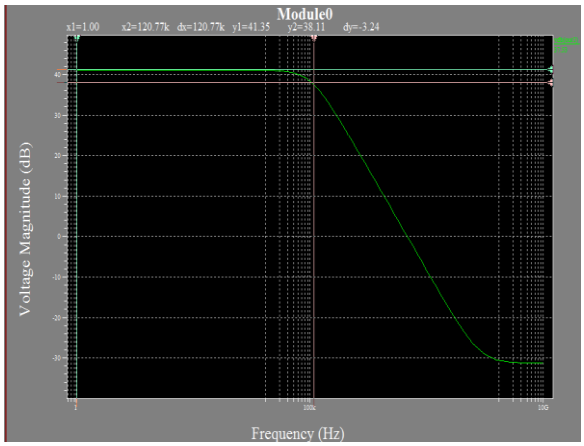

Figure 13. AC Analysis at C_L=3 PF

At CL=3.5 PF

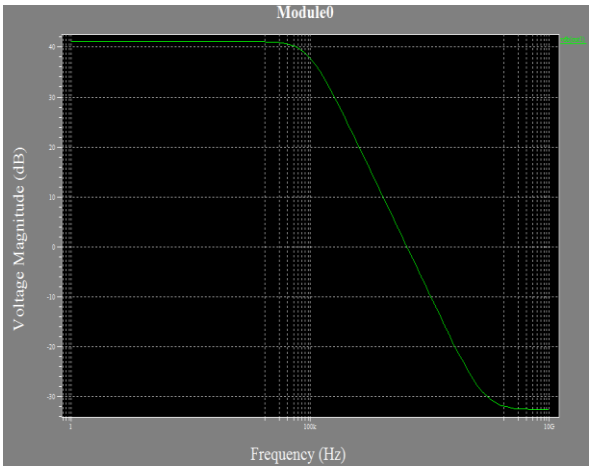

Figure 14. AC Analysis at C_L=3.5 PF

Table 3. Obtained Parameters for different Loads

Achieved Parameters	Gain	3dB Bandwidth	UGB	Power Dissipation
C_L=2.5 pF	41.27 dB	155.33 kHz	15.66 MHz	216.15 µW
C_L=3 pF	41.35 dB	138.73 kHz	12.40 MHz	216.15 µW
C_L=3.5 pF	41.13 dB	112.68 kHz	9.84 MHz	216.15 µW

5.5. Temperature Variations

On applying different values of temperature there are changes in all achieved parameters. The achieved parameters has been plotted in the following figures for three different (200C, 300C, 400C,) values temperatures.i.e.

5.5.1. AC Analysis

AC analysis has been done first for all three temperatures. From Figure 15, plotted waveforms, the following parameters have been obtained as in Table 4. According to Table 5 this has to be seen that as temperature is increasing, each parameter is improving. Gain and Bandwidth is maximum at 300C.

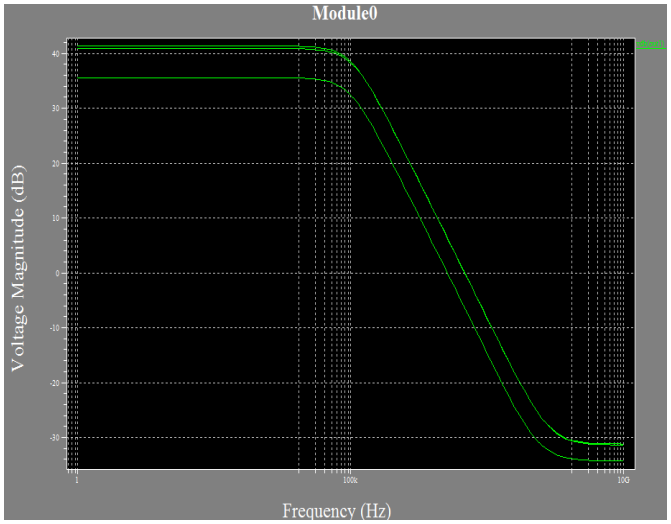

Figure 15. AC Analysis at Different Temperatures

Table 4. Obtained Parameters for different Temperatures

Achieved Parameters	T=20^{0}C	T=30^{0}C	T=40^{0}C
Gain	40.92 dB	41.45 dB	28.28 dB
3dB Bandwidth	121.98 kHz	121.98 kHz	121.78 kHz
UGB	12.69 MHz	12.69 MHz	5.88 MHz
Power Dissipation	216.15 µW	216.15 µW	216.15 µW

Table 5. Obtained Parameters for different Power Supplies

Achieved Parameters	V_{DD}=3 V	V_{DD}=3.3 V	V_{DD}=3.6 V
Gain	37.03 dB	40.92 dB	38.12 dB
3dB Bandwidth	83.17 kHz	121.98 kHz	157.47 kHz
UGB	2.39 MHz	12.69 MHz	11.65 MHz
Power Dissipation	196.5 µW	216.15 µW	235.8 µW

5.5.2. DC Analysis

The DC analysis has been done for all three temperatures and the values for all three nodes have been plotted. According to the Figure 16 and Figure 17 this has to be seen that there is no effect on the DC voltages of all nodes. So this has to be said that the circuit is resistant for common mode signal and can be operated on different temperatures.

Effect on V_{OUT1}

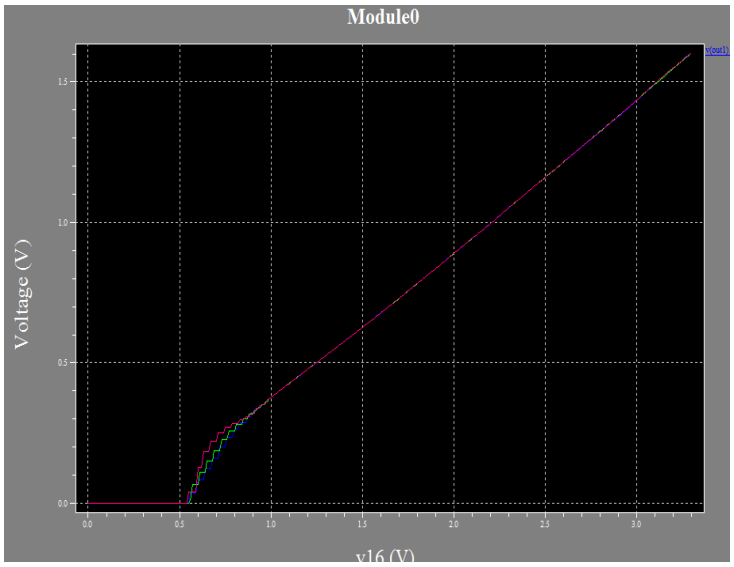

Figure 16. DC Analysis on Node V_{OUT1}

Effect on VOUT2

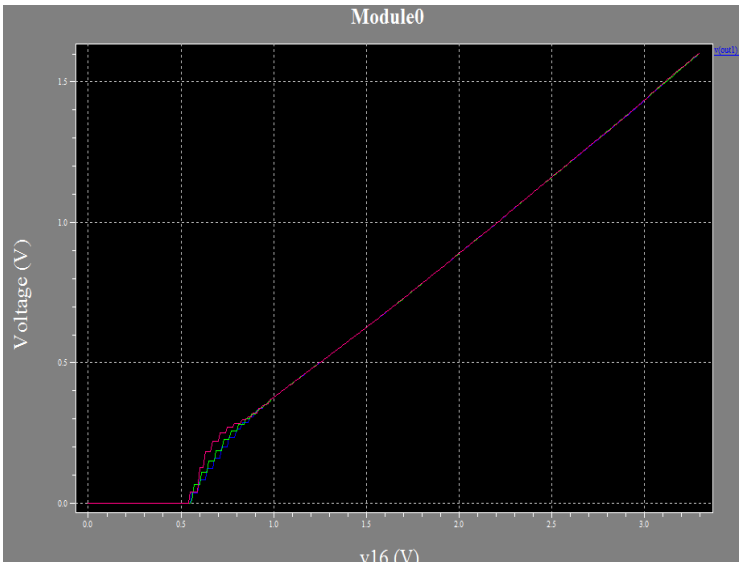

Figure 17. DC Analysis on Node V_{out2}

5.6. Power Supply Variations

The effect of the variation in power supply has been plotted. From Figure 18, plotted waveforms, the following parameters have been obtained as in Table 5. According to the Table 5 this has to be seen that the overall performance of the circuit is increasing for lesser value of power supply.

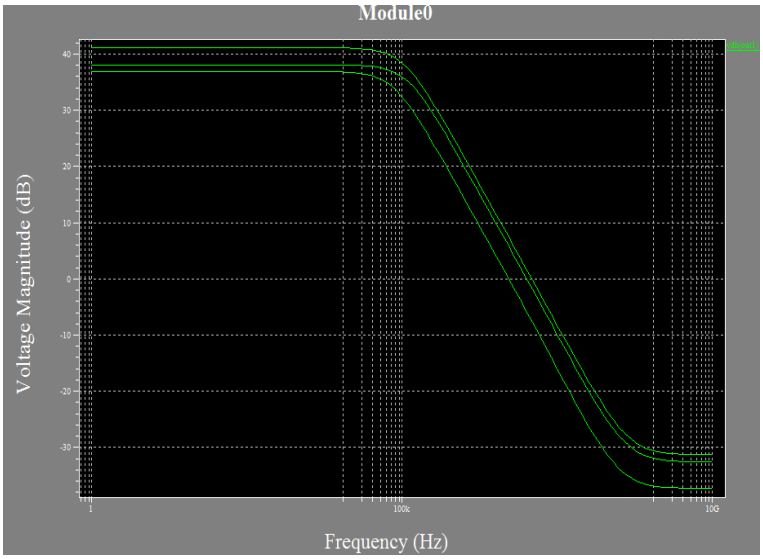

Figure 18. AC Analysis of Power Supply Variation

6. CONCLUSIONS

Self biasing is the area of biasing, which reduces the area requirement of the circuit. As the technology is scaled down it is more important for a filter to work at any CM level. Here in this thesis work, fully self biased OTA using a design methodology based on the g_m/I_D transistor characteristics is designed and simulated with the schematic of the circuit.

The OTA has Gain of 41.35 dB and 3db bandwidth of 138.73 kHz and the UGB of 12.40MHz with the current consumption of 65.50 µA. The circuit does not have need of any DC external biasing circuit, only need to apply VDD (3.3 V). Here self biasing has been introduced with power consumption of 216.15µW.

The operation of the input stage under different supply voltages and temperature are simulated and analyzed. Simulation result for temperature variation, power supply variations and load variations shows that the circuit can be used for wide range of temperature, power supply and load variation. The main feature of the circuit is the self biasing with low current consumption of 65.5µW.

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