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FPGA Implementation of DS-CDMA Transmitter and Receiver

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Article Info	ABSTRACT
	Direct sequence spread Spectrum (DSSS) is also known as direct sequence code division multiplexing. In direct sequence spread spectrum the stream of information to be transmitted is divided into small pieces each of which is allocated across to a frequency channel across the spectrum. Data signal at the point of transmission is collaborated with a higher data-rate bit sequence (also called chipping code) that divides the data according to a spreading ratio. A redundant chipping code helps the signal resist interference and also enables the original data to be recovered if data bits are damaged during the transmitting. In this project direct sequence spread spectrum principle based code division multiple access (CDMA) transmitter and receiver is implemented on SPARTAN 3E FPGA. The Xilinx synthesis technology (XST) of Xilinx ISE tool used for synthesis of transmitter and receiver on FPGA Spartan 3E.

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1. INTRODUCTION

In communication systems an attractive approach for high quality digital cellular and personal communication services the technique used is Direct sequence code division multiple access (DS-CDMA). Because of its improved privacy and security. VHDL implementation of DS-CDMA transmitter and receiver has been proposed in this paper. Every mobile handset and every wireless base station operates on the same frequency spectrum. To discriminate one conversation from the other every handset broadcast a unique code sequence is called as pseudo noise code. The pseudo noise code is generated by using two six bit LFSRs. The code signal is called as chip signal. These chips are modulated by the carrier using a digital modulation technique BPSK. A carrier is generated by using the technique called discrete digital frequency synthesizer.

The CDMA base stations must be able to discriminate this different code sequences in order to distinguish one transmission from other. Thus it is accomplished by means of a matched filter. Matched filter is a filter whose frequency spectrum is exactly designed to match the frequency spectrum of the input signal. Pseudo noise code is generated by matched filter, the generated noise code is correlated with the received code and detecting original data.

In recent years the CDMA on FPGA platform has attracted attention of academic research and industry. Spartan 3E family of Field-Programmable Gate Arrays (FPGAs) is specifically broadband designed to meet the needs of high volume and cost-sensitive consumer electronic applications. Due to low cost Spartan -3E FPGAs are ideally suited to a wide range of consumer electronics applications, home networking, including access, display/projection and digital television equipment.

2. LITERATURE SURVEY

In 1947 the cellular concept originated at Bell Labs. The first automatic analog cellular system started operation in 1979 in Japan and in 1981 in the Nordic countries. The first commercial AMPS wireless cellular system in the United States started in October 1983 in Chicago. Analog cellular service operates on

the 800 MHz frequency band and is based on FDMA (Frequency Division Multiple Access). A period of few years after analog cellular systems were introduced which became apparent, more reliable and lower cost wireless systems were. The predictions were made that system capacity would be saturated by the 1990s, by first in the largest cities and then in other regions. Hence, when consumer demand saturates the capacity of a cellular system, the there are three ways to expand it: move into new spectrum bands and splitting existing cells into smaller cells or introduce new technology to make more efficient use of existing bandwidth. So, since no new radio spectrum would be available and the splitting cells requires very expensive additional network infrastructure, hence new technology seemed to be the best route.

3.   MULTIPLE ACCESS TECHNIQUES

Multiple access schemes are used to allow many simultaneous users to use the same radio spectrum with constant bandwidth. The bandwidth allocated in any radio systems is always limited. And the total bandwidth allocated mobile phone systems is typically 50 MHz and which is split in half to provide the forward and reverse links of the system. The sharing of same spectrum is required in order to increase the user capacity of any wireless network. TDMA, FDMA and CDMA are the three major methods of sharing the available bandwidth to multiple users in wireless system. CDMA provides less interfered and more secured type communication among these multiple access techniques.

3.1. Frequency Division Multiple Access

In Frequency Division Multiple Access (FDMA) the overall bandwidth is divided into a number of narrower band channels. And each user is allocated with a unique frequency band for transmitting and receiving. During a call, other user cannot use the same frequency band. In which each user is allocated with a forward link channel (from the base station to the mobile phone) and a reverse channel (back to the base station). The transmitted signal on each of the channels is continuous allowing analog transmissions. In most FDMA systems the channel bandwidth used is typically low (30 kHz) as each channel only needs to support a single user. Figure 1 shows FDMA systems.
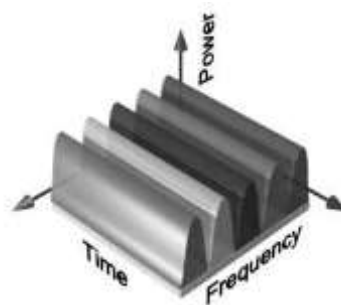

Figure 1. FDMA systems

3.2. Time Division Multiple Access

Time Division Multiple Access (TDMA) divides the available spectrum into multiple time slots, each user is allocated with a separate time slot in which they can transmit or receive TDMA systems. Figure 2 shows TDMA schemes where each user is allocated with a small time slot.
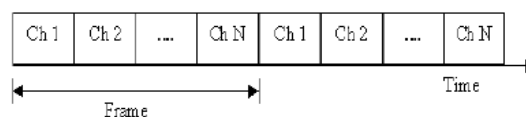

Figure 2. TDMA schemes where each user is allocated with a small time slot

The transmission of each channel is non-continuous. Thus the input data to be transmitted is buffered over the previous frame and burst transmitted at a higher rate during the time slot for the channel. A TDMA cannot send an analog signal directly due to the buffering required so it is only used for transmitting.

3.3. Code Division Multiple Access

Code Division Multiple Access (CDMA) is a spread spectrum technique that uses neither frequency channels nor time slots. Using CDMA the narrow band message (typically digitized voice data) is multiplied by a large bandwidth signal that is a pseudo random noise code (PN code). In CDMA system all users transmit with the same frequency band. The transmitted signal is recovered by correlating the received signal with the PN sequence code used by the transmitter. Figure 3 shows code division multiple access (CDMA).
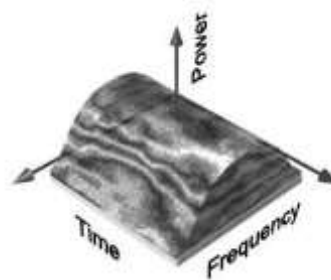

Figure 3. Code division multiple access (CDMA)

CDMA technology was first developed by the military during World War II. They were looking for different ways of communication with secure and without jamming while in work. Some of the properties that have made CDMA useful are:

- Anti-jam and interference rejection
- Information security
- Accurate Ranging

4.   RESULTS AND ANALYSIS
4.1.   Direct Sequence CDMA Generation

DS-CDMA is achieved by spreading the data signal by a pseudo random noise sequence (PN code) which has a chip rate higher than the bit rate of the data. Pseudo Noise code sequence is a sequence of ones and zeros (called chips). PN code used to spread the data can be of two main types. A short PN code (typically 10-128 chips in length) can be used to modulate each data bit. For the synchronization of the receiver a short PN code is then repeated for every data bit. Alternatively a long PN code can be used. Figure 4 shows direct sequence signals.
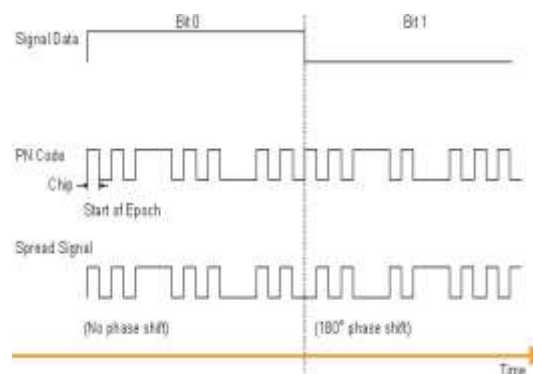

Figure 4. Direct sequence signals

In DS-CDMA, the spreaded signal is modulated by a RF carrier.

4.1.1. CDMA Transmitter

In CDMA transmission user data is combined with a PN sequence and then modulated using BPSK modulation where in the carrier is generated using digital frequency synthesizer principle. Then the modulated signals from different users are combined and transmitted. Figure 5 shows block diagram of multiple user CDMA transmitters.
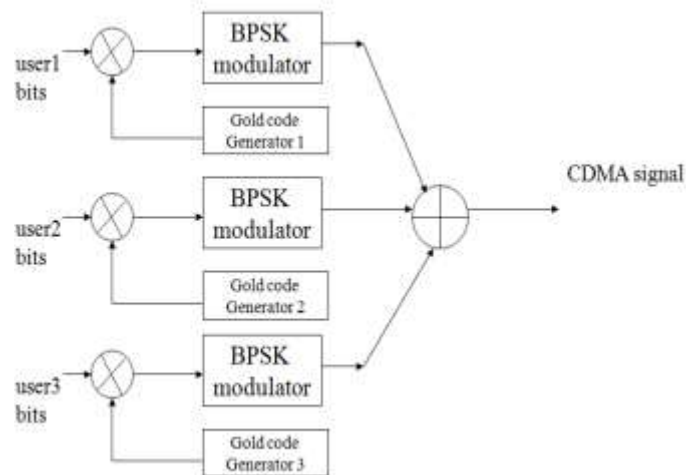
Figure 5. Block diagram of multiple user CDMA transmitters

4.1.2. PN Sequence Generation

The PN sequence generator is the most important block of DS-CDMA communication system. It is implemented by using Linear Feedback Shift Registers to generate several types of PN sequences. Figure 6 shows the flow chart of the PN generator.
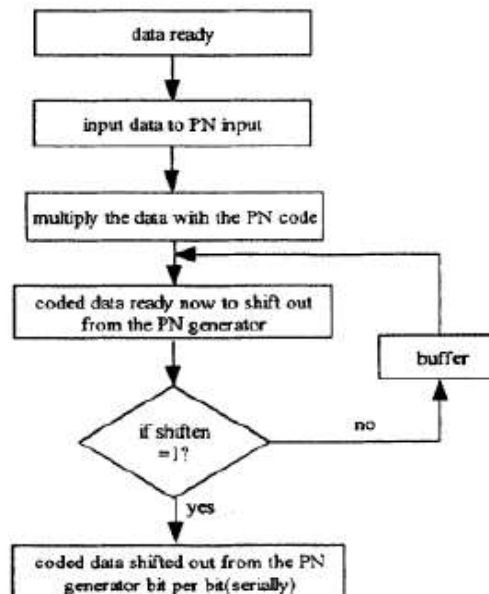
Figure 6. The flow chart of the PN generator

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4.1.3. Signal Spreader

The use of signal spreader is to generate PN sequence when the information bit is '1' and generate the complement of the PN sequence if the information bit is '0'. The digital implementation of signal spreader is achieved by using XOR gate controlled inverter action. And the spreaded chip signal is used for modulation by BPSK modulator.

4.1.4. BPSK Modulator

The BPSK modulator produces the band pass spread spectrum signal which is suitable for transmission from the spreaded signal. It is implemented using pure digital architecture. Direct Digital Frequency Synthesis (DDFS) technique with phase shifting provision is used for the signal generation.

4.1.5. DS-CDMA Receiver

The CDMA receiver receives the transmitted data and using matched filter it correlates the received data with PN code. The matched filter can distinguish the PN sequence and the passes the data to the respective user. Figure 7 shows block diagram of multiple user CDMA receivers.
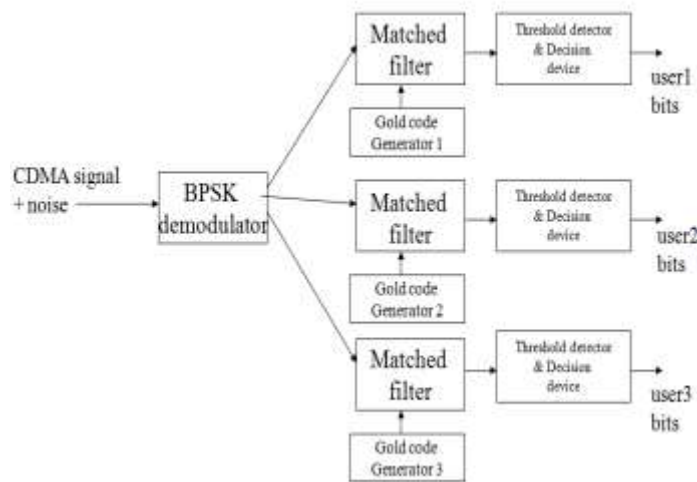

Figure 7. Block diagram of multiple user CDMA receivers.

5. RESULTS

5.1. Simulation Results

The above simulation result shows the DS CDMA top level module transmitter and receiver. And observed that the received data is same as the user data with some amount of delay. Figure 8 shows simulation result for DS CDMA top level module. Figure 9 shows simulation result for DS CDMA top level module for second data.
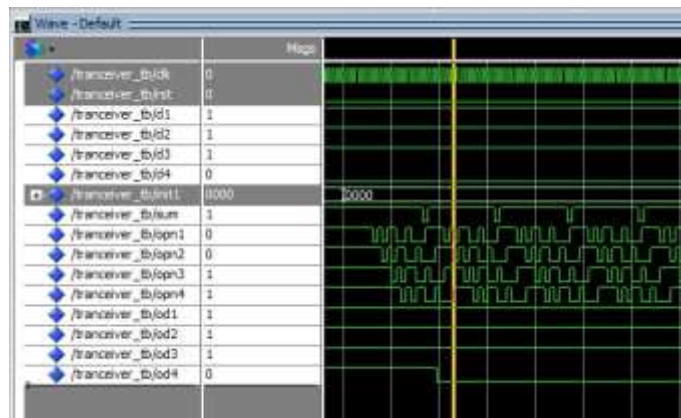

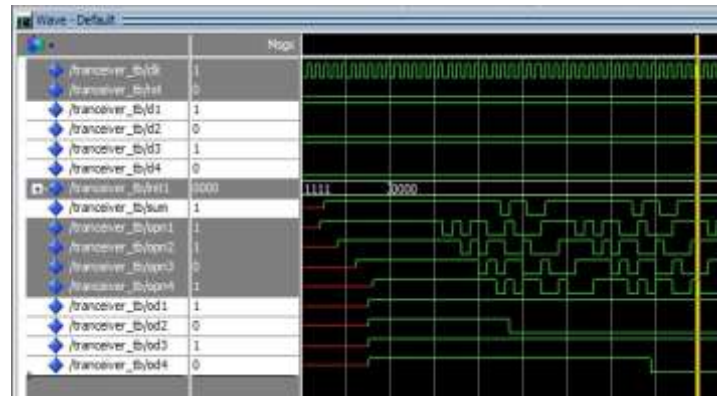Figure 8. Simulation result for DS CDMA top level module

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Figure 9. Simulation result for DS CDMA top level module for second data

5.2. Synthesis Results

The synthesis have been done by using XILINX XST tool and targeted for SPARTAN 3E FPGA device. Figure 10 shows DS CDMA top level RTL schematic. Figure 11 shows DS CDMA power report.
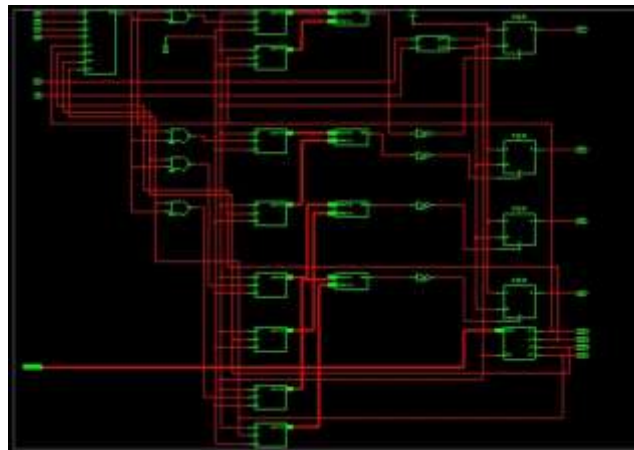

Figure 10. DS CDMA top level RTL schematic

Power summary:	I(mA)	P(mW)
Total estimated power consumption:		52
Vccint 1.20V:	15	19
Vccaux 2.50V:	12	30
Vcco25 2.50V:	2	4
Clocks:	0	0
Inputs:	0	0
Logic:	0	0
Outputs:		
Vcco25	0	0
Signals:	0	0
Quiescent Vccint 1.20V:	15	19
Quiescent Vccaux 2.50V:	12	30
Quiescent Vcco25 2.50V:	2	4

Figure 11. DS CDMA power report

6.   CONCLUSION

In this paper, we have observed the simulation results of DS CDMA using Modelsim simulator and synthesized by using XILINX XST tool and also implemented on SPARTAN 3E FPGA device. The implemented architecture supports for 4 users communication. The proposed DS CDMA system provides efficient area utilization on FPGA. Further the proposed project can be extended by implementing with multiple transmitters and receivers. And various techniques can also be implemented to improve the multipath interference effect.

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