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FPGA Based Symmetrical Multi Level Inverter with Reduced Gate Driver Circuits

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ABSTRACT

Multilevel converters tender advantages in terms of the output waveform quality due to the increased number of levels used in the output voltage modulation and have been widely accepted for high-power high-voltage applications. This paper introduces topology in multilevel dc link inverter (MLDCLI), which can significantly reduce the switch count and improve the performance. The preferred topology provides a dc voltage with the shape of a staircase approximating the rectified shape of a commanded sinusoidal wave, to the bridge inverter, which in turn gives the required alternating waveform**.** This topology requires fewer components compared to traditional Multi level Inverters (MLI).Therefore, the overall cost and complexity are significantly reduced particularly for higher output voltage levels. Finally, Matlab/Simulink and XILINX are used as a simulation and compiler architecture of control circuit embedded in FPGA. Simulation and experimental results for fifteen-level inverter are presented for validation

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1. INTRODUCTION

Multi level converter technologies are receiving increased attention recently, especially for use in high power applications [1-2]. This increased attention is probably due to the fact that the output waveforms are much improved over those of the two-level converter technologies, and that the voltage rating of the converter is increased due to the series connection of the devices. Figure 1 shows one way to classify multilevel converters, similar to the classification by Lai and Peng [3].

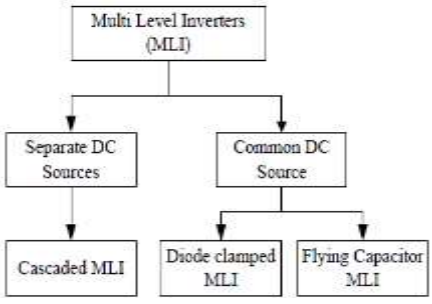

Figure 1. Types of basic multi level inverters

The general concept in MLI's involves utilizing a higher number of active semiconductor switches to perform the power conversion in small voltage steps. There are several advantages to this approach when compared with the conventional power conversion approach. The smaller voltage steps lead to the production of higher power quality waveforms and also reduce voltage (dv/dt) stress on the load and the electromagnetic compatibility concerns [4].

In recent years, there has been a substantial increase in interest to multilevel power conversion. Recent research has involved the introduction of novel converter topologies and unique modulation strategies. Some applications for these new converters include industrial drives [5]-[7], flexible ac transmission systems (FACTS) [8]-[10], and vehicle propulsion [11]-[12]. One area where multilevel converters are particularly suitable is that of renewable photovoltaic energy that efficiency and power quality are of great concerns for the researchers [13]. Some new approaches have been recently suggested such as the topology utilizing low-switching-frequency high-power devices. Although the topology has some modification to reduce output voltage distortion, the general disadvantage of this method is that it has significant low-order current harmonics [14]. The multilevel output is generated with a multi winding transformer. However, the design and manufacturing of a multi winding transformer are difficult and costly for high-power applications. Equal valued dc supplies are employed for preferred configuration which causes the topology into symmetrical that have flexibility to arrange the dc supplies easily to get the required output voltage levels and it is also effortless on the way to increase in the direction of any number of levels. Ebrahimi has proposed a new multilevel converter topology with reduced number of switch to obtain maximum levels at the output [15]. It is observed that the multi-levels are achieved through cascaded arrangement of cells, in which the successive addition of individual cells may bear equal blocking voltage, and the outset cell in the topology undergoes high blocking voltage that causes device failure which reduces efficiency. It is studied that topologies with assymetrical dc voltages will cause complexity in deriving the required voltages levels by adding and subtracting the available voltage sources to achieve particular level [16].

The topology in this paper is a symmetrical topology since all the values of all voltage sources are equal and consists of a multilevel output which is named as level generation part (LGP) and a single phase full-bridge (SPB) inverter which is named as reversing voltage part (RVP). This topology requires less number of components compared to conventional topologies. It is also more efficient since the inverter has a component which operates the switching power devices at line frequency. The devices in the LVP alone operate at higher frequencies; device in RVP will operate at line frequency. Therefore, there is no need for all switches to work in high frequency which leads to simpler and more reliable control of the inverter.

The successful operation of any topology will depends on the selection of proper control strategy and switching states. The gating pulses are derived by using sinusoidal pulse width (SPWM) and the advantages of PWM are given as (i) Control over output voltage magnitude, (ii) Reduction in magnitudes of unwanted harmonic voltages, (iii) Improved power factor with unity displacement factor. Lowest order harmonic elimination is possible by proper choice of the number of pulses per half cycle. In this paper multi carrier SPWM techniques are used. Three alternative carrier PWM strategies with differing phase relationships for a multilevel inverter are as follows:

a. In-phase disposition (IPD),
b. Phase opposition disposition (POD),
c. Alternative phase opposition disposition (APOD).

IPD or PD strategy is used most frequently because it produces minimum harmonic distortion compare to other PWM strategies [17]-[21]. In this paper a general method of multicarrier modulation (IPD) SPWM is utilized to drive the preferred inverter topology and can be extended to any number of voltage levels.

2. REVERSING VOLTAGE PART MULTI LEVEL DC LINK INVERTER

In traditional multilevel inverters, the power semiconductor switches are combined to produce a high-frequency alternating waveform. However, there is no need to utilize all the switches for generating bipolar levels. The topology in this paper is a hybrid MLI which separates the output voltage into two parts as shown in Figure 2. One part of the topology is used for generating the levels only in positive polarity. This part requires high-frequency power semiconductor switches to generate the required number of levels. And other part is called reverse voltage part and is responsible for generating alternating output voltage at line frequency, this part require low-frequency power semiconductor switches and this part will operate at line frequency.

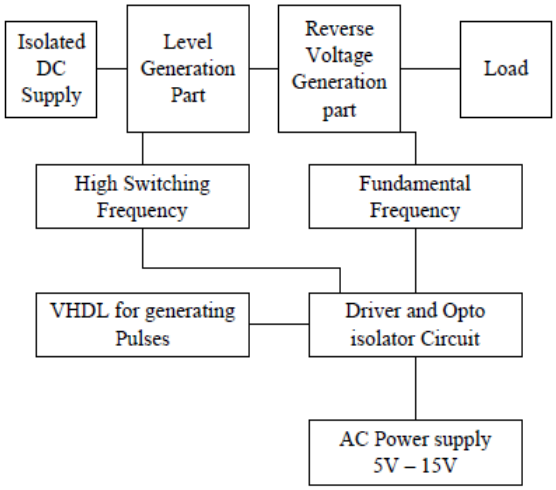

Figure 2. Block diagram of the preferred MLDCLI topology

The topology combines the high frequency and low frequency parts to generate the necessary multilevel output voltage. In order to generate a complete multilevel output, the positive levels are generated by the LGP, and then, this is fed to a SPB inverter for RVP, which will generate the required polarity for the output. The RV topology for fifteen levels is shown in Figure 3. As can be seen, it requires seven switches, six diodes and seven isolated sources. Left part of circuit is used to generate the required output levels with positive polarity and the right part of circuit is SPB inverter, decides about the polarity of the output voltage i.e. alternating waveform with required levels. It reverses the voltage direction when the voltage polarity requires to be changed for negative polarity. The preferred topology easily extends to higher voltage levels by duplicating the module as shown in Figure 3. It can also be applied for three-phase applications with the same principle. Comparison between preferred topology and conventional topologies is given in Table 1. It can be clearly seen that the preferred topology requires less number of components. So an added advantage of this topology is that it will occupy less space and produce the required output with lesser distortions. The maximum output voltage is obtained by adding the amplitude of all the DC sources connected in the circuit. Therefore the output voltage levels are derived by selection of individual DC source and by proper switching action of the power semiconductor switches.

$$V_{Output\max} = \sum_{k=1}^{n} V_k \tag{1}$$

The LG part provides a dc bus voltage, with the shape of a staircase that approximates the rectified waveform of the commanded sinusoidal voltage, to the RV part, which in turn alternates the voltage polarity to produce an ac voltage of a staircase shape with required levels.

The active number of switches in preferred topology

$$= \left[\left(\frac{\mathrm{m}-1}{2} \right) + 4 \right] \tag{2}$$

Number of dc sources

$$= \frac{(\mathrm{m}-1)}{2} \tag{3}$$

Number of Diode

$$= \frac{(m-3)}{2} \quad (4)$$

Where, m is the number of levels.

Table 1. Comparison of number of components for fifteen level single phase MLI Inverters

Sl.No	MLI structure	CHB	DC	FC	MLDCLI			Preferred MLDCLI
					CHB	DC	FC	
1	Main switches	28	28	28	24	18	18	11
2	Bypass diodes	0	0	0	0	0	0	7
3	Clamping diodes	0	24	0	0	12	0	0
4	DC Split capacitors	0	6	6	0	6	6	0
5	Clamping capacitors	0	0	12	0	0	6	0
	Total	35	59	47	25	37	31	18

This topology uses isolated dc supplies. Therefore, it does not face voltage-balancing problems due to fixed dc voltage values, the isolated dc supplies can be replaced by renewable sources by properly designed control ciruit to avoid voltage balancing problems [22]. The topology can extend to three phase applications and shown in Figure 4, the complete three-phase inverter for fifteen levels is shown with a three-phase delta connected system [23].

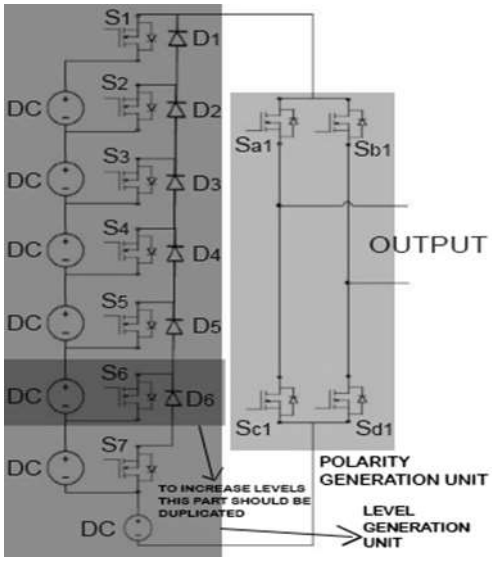

Figure 3. Schematic of preferred MLDCLI 15 level in single phase with duplicating module to increase level

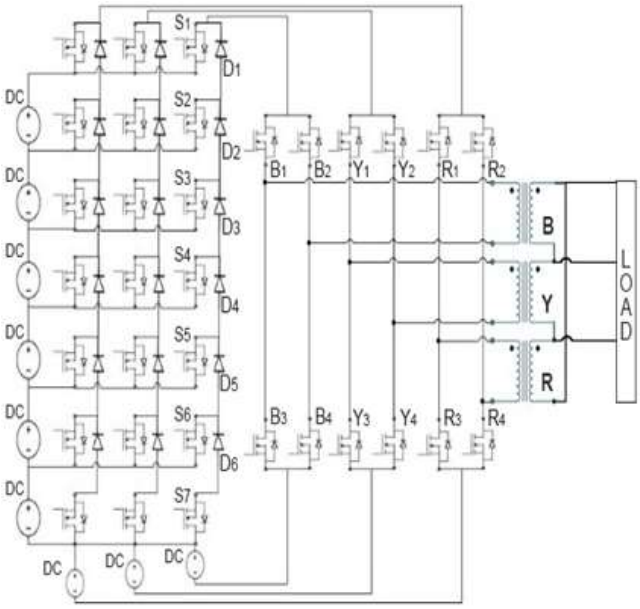

Figure 4. Schematic of a fifteen-level inverter in three phase

According to Figure 4, the multilevel positive voltage is fed to the full-bridge converter to generate its alternating waveform. Then, the o/p of the each full bridge converter is connected to the primary of a transformer. The secondary of the transformer is delta connected and can be connected to a three-phase system. This topology requires fewer components in comparison to conventional inverters. Another advantage of this topology is that it just requires half of the conventional carriers for SPWM controller. SPWM for fifteen-level conventional converters consists of fourteen carriers, but in this topology, seven carriers are sufficient. The reason is that, according to Figure 3, the concept of generating multilevel works

only in LG part. Therefore, it implements the multilevel inverter with a reduced number of carriers, which is a great achievement for inverter control.

The preferred topology does not need fast switches for the reverse generation part. Switching sequences in this converter are easier than its counter parts. According to its inherent advantages, it does not need to generate negative pulses for negative cycle control. Thus, there is no need for extra conditions for controlling the negative voltage. Instead the single phase full bridge converter performs this task and generates the reverse polarity. Table 2 gives detail description of the switching states of the topology for 15-level inverter with both LG part and RV part.

Table 2. Switching States of the Hybrid Fifteen Level Topology

Level	Output Voltage	Switch Status of the LG Part							Switch Status of RV Part				Fundamental Cycle
		S7	S6	S5	S4	S3	S2	S1	Sa	Sb	Sc	Sd	
1	0	0	0	0	0	0	0	0	1	1	0	0	0-π
2	1*V_{DC}		0	0	0	0	0	0	1	1	0	0	
3	2* V_{DC}	x		0	0	0	0	0	1	1	0	0	
4	3* V_{DC}	x	x		0	0	0	0	1	1	0	0	
5	4* V_{DC}	x	x	x		0	0	0	1	1	0	0	
6	5* V_{DC}	x	x	x	x		0	0	1	1	0	0	
7	6* V_{DC}	x	x	x	x	x		0	1	1	0	0	
8	7*V_{DC}	x	x	x	x	x	x		1	1	0	0	
9	6* V_{DC}	x	x	x	x	x		0	1	1	0	0	
10	5* V_{DC}	x	x	x	x		0	0	1	1	0	0	
11	4* V_{DC}	x	x	x		0	0	0	1	1	0	0	
12	3* V_{DC}	x	x		0	0	0	0	1	1	0	0	
13	2* V_{DC}	x		0	0	0	0	0	1	1	0	0	
14	1*V_{DC}		0	0	0	0	0	0	1	1	0	0	
15	0	0	0	0	0	0	0	0	1	1	0	0	
1	0	0	0	0	0	0	0	0	0	0	1	1	π-2*π
2	1*V_{DC}		0	0	0	0	0	0	0	0	1	1	
3	2* V_{DC}	x		0	0	0	0	0	0	0	1	1	
4	3* V_{DC}	x	x		0	0	0	0	0	0	1	1	
5	4* V_{DC}	x	x	x		0	0	0	0	0	1	1	
6	5* V_{DC}	x	x	x	x		0	0	0	0	1	1	
7	6* V_{DC}	x	x	x	x	x		0	0	0	1	1	
8	7*V_{DC}	x	x	x	x	x	x		0	0	1	1	
9	6* V_{DC}	x	x	x	x	x		0	0	0	1	1	
10	5* V_{DC}	x	x	x	x		0	0	0	0	1	1	
11	4* V_{DC}	x	x	x		0	0	0	0	0	1	1	
12	3* V_{DC}	x	x		0	0	0	0	0	0	1	1	
13	2* V_{DC}	x		0	0	0	0	0	0	0	1	1	
14	1*V_{DC}		0	0	0	0	0	0	0	0	1	1	
15	0	0	0	0	0	0	0	0	0	0	1	1	

In order to produce fifteen levels by SPWM, seven saw-tooth waveforms for seven carriers are required and a one sinusoidal reference signal as modulating signal is required as shown in Figure. 5.

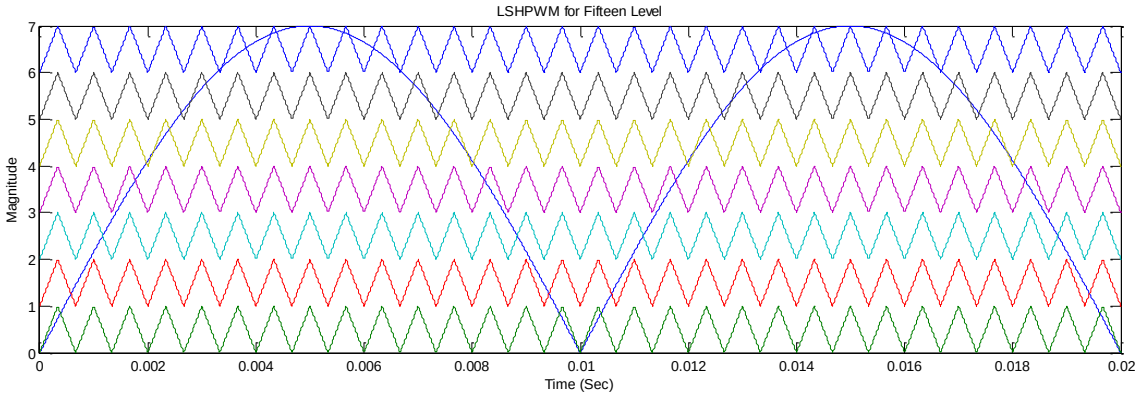

Figure 5. SPWM carrier and modulator for positive voltage level generation.

3. FIELD PROGRAMMABLE GATE ARRAY

Field Programmable Gate Arrays (FPGAs) are semiconductor devices that are based around a matrix of configurable logic blocks (CLBs) connected via programmable interconnects. FPGA can be programmed by different stages. Design entry is the stage of implementing a required design of the programmer in soft format on FPGA. Xilinx ISE 12.1 software is used to write a program to generate PWM pulses using VHDL (Very High Speed Integrated Chip Hardware Description Language). Once the code is written the entire code is verified for syntax. After the code is synthesized it will convert into equivalent logic gates and produces a net-list. In implementation stage, the design is used for Placing and Routing which places the logic blocks of the design into FPGA and route them together so that they occupy minimum area and meet timing requirements. Then the code is converted in to the digital bits as FPGA can understand only digital language this process is used to transfer the code from system to kit using joint test action group cable. Figure 6 shows the various steps involved in writing a program on FPGA kit [24], [25].

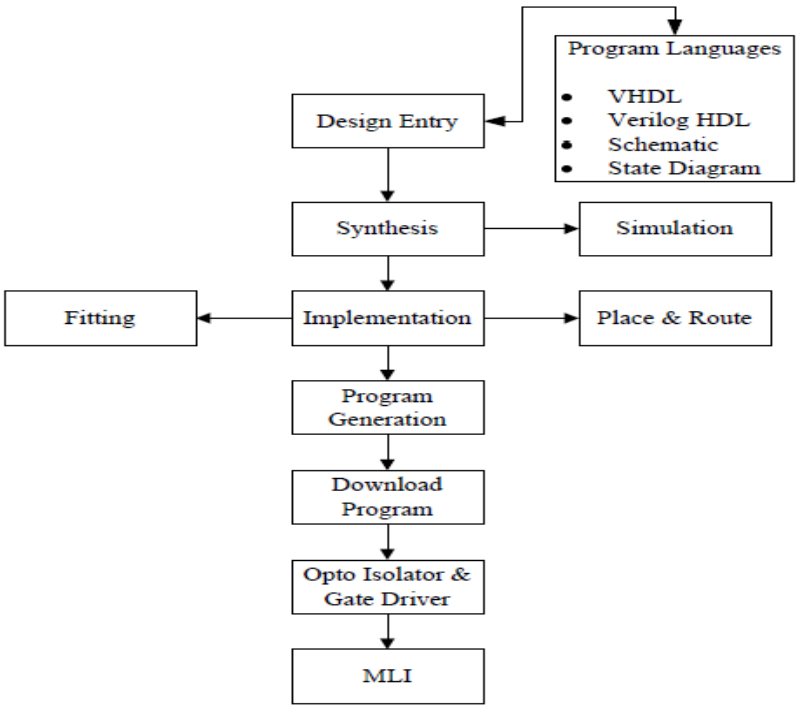

Figure 6. Stages of FPGA coding

Advantage of the FPGA is

- Operating Speed
- Reduce in design cycle time
- power consumption is less
- Increase in Design flexibility and security

ModelSim simulator is used to test the design of PWM pulses of suggested MLI before transforming the pulses into hardware. Below Figure shows the flowchart of the PWM pulse generation

4. SIMULATION RESULTS

The topology discussed in the section 2 is tested using Matlab/Simulink software 7.9.0 (R2009b) version. The Sim-powersystems block in the Matlab/Simulink is used to test the prototype of preferred topology and the results are studied. The performances of topology have been tested with R, RL loads and extended to three phase with same principal of operation and tested for three phase induction motor by giving step torque. Figure 7 shows the simulation diagram of the topology. Figure 8 shows the output waveform of the Level Generation Part. Figures 9 to 13 shows the output waveforms for R and RL load with and without filter. Figure 14, 20, 23 shows the simulation diagram of three phase fifteen level inverter for R, RL, Induction motor loads respectively; Figure 15 and 16 shows the output waveform of voltage and current for R load. Figure 17 shows simulation diagram of the topology for R load with filter for three phase fifteen level. Figure 18 and 19 shows the output voltage and current waveforms with filter for R load with filter. Figure 21 and 22 shows output voltage and current waveforms for RL load with filter. Figure 24 shows the three phase stator current, Figure 25 shows the speed of the induction motor in rpm, and Figure 26 shows the electromagnetic torque of the induction motor. Tables 3 and 4 gives the performance analysis of the topology by varying the switching frequency with and without filter, the results clearly shows the %THD value has been decreased almost 50% by using filter. And % THD values falls in acceptable range by IEEE standard. Table 5 and 6 give the results of the topology by varying the modulation index and the %THD is better when the Modulation index is one.

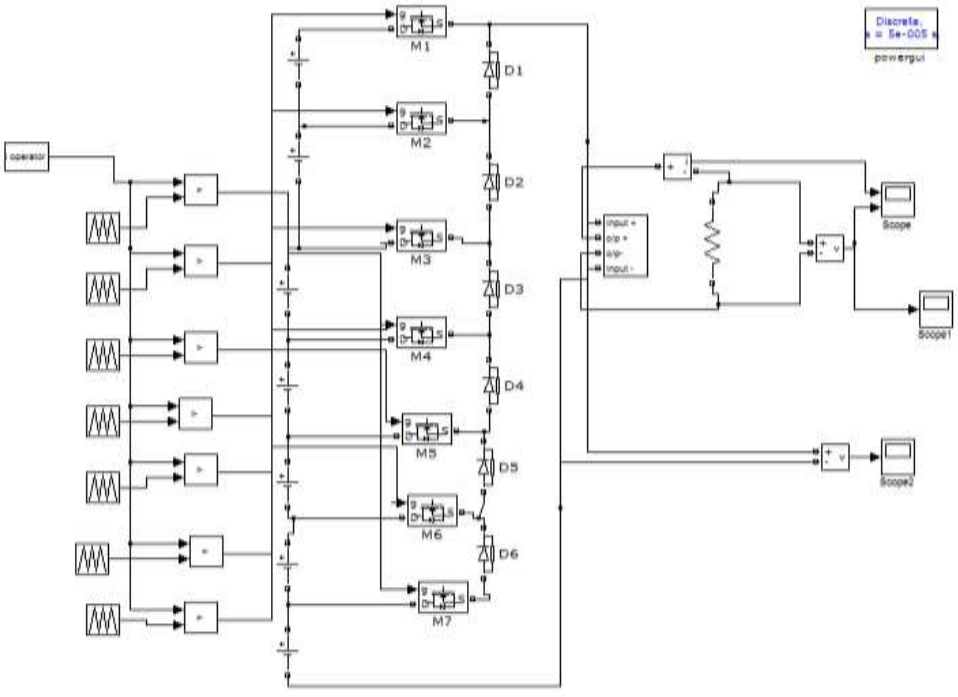

Figure 7. Simulation circuit of proposed single phase fifteen level topology

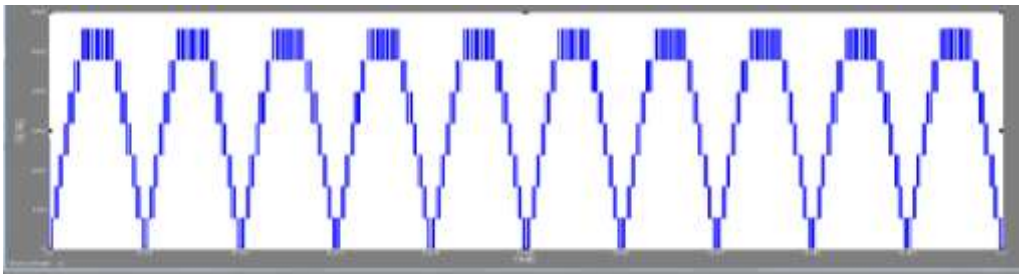

Figure 8. Output voltage waveform of level generation part

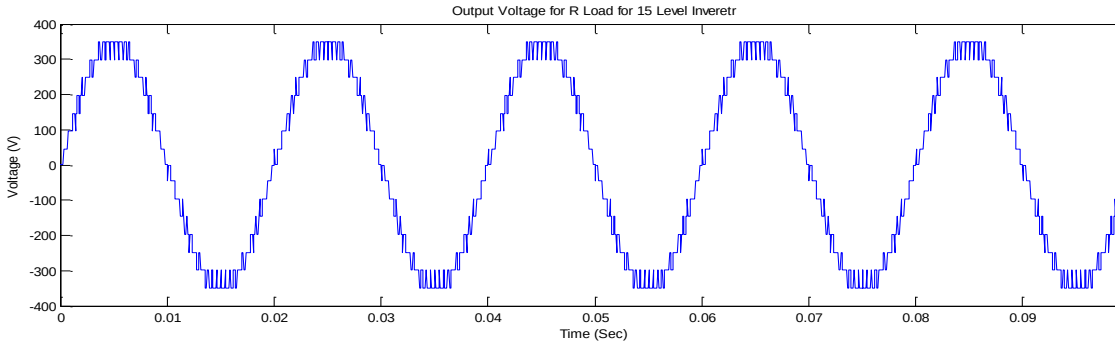

Figure 9. Output voltage waveform of reverse voltage generation part for R-Load without filter

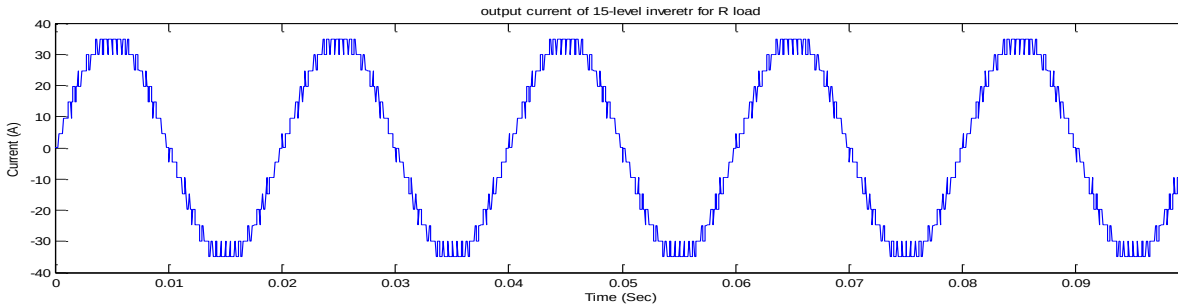

Figure 10. Output current waveform of reverse voltage generation part for R-Load without filter

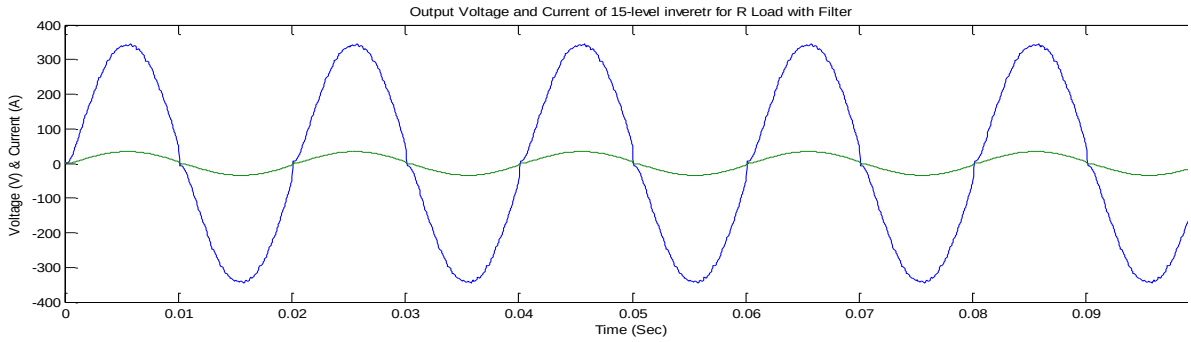

Figure 11. Output voltage and current of 15-Level Inverter for R load with filter

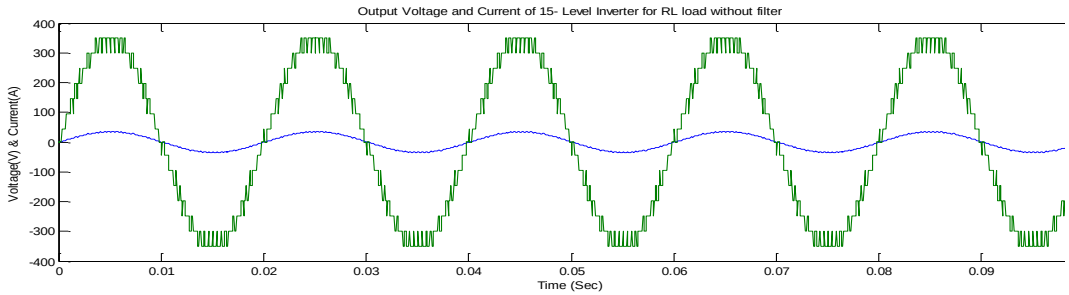

Figure 12. Output voltage and current of 15-level inverter for RL load without filter

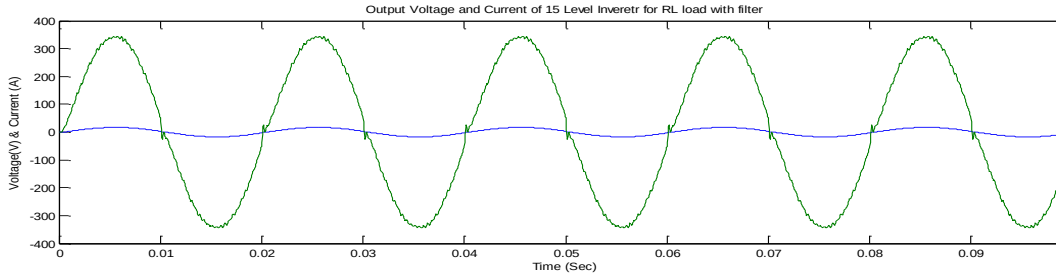

Figure 13. Output Voltage and Current of 15-Level Inverter for RL load with Filter

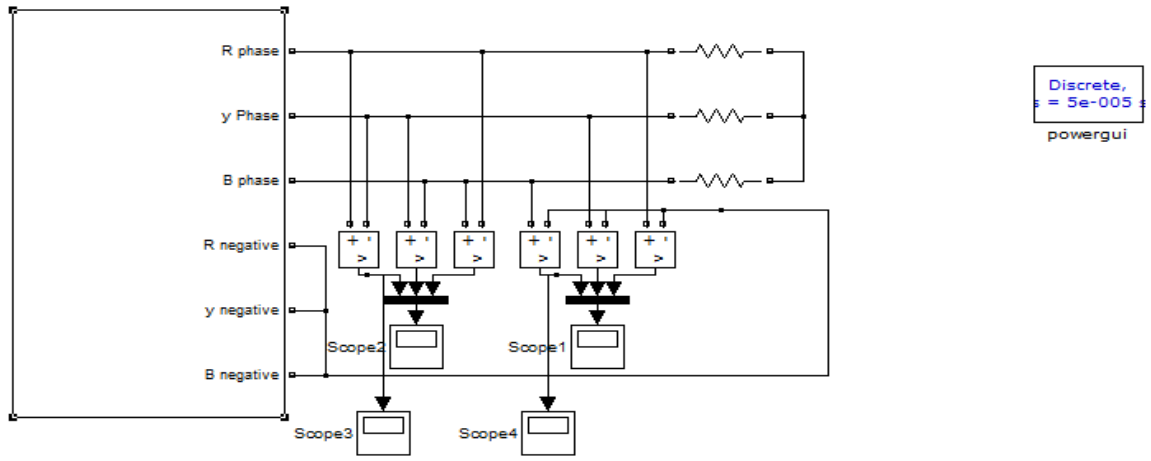

Figure 14. Subsystem of three phase Matlab/Simulink circuit for 15-level

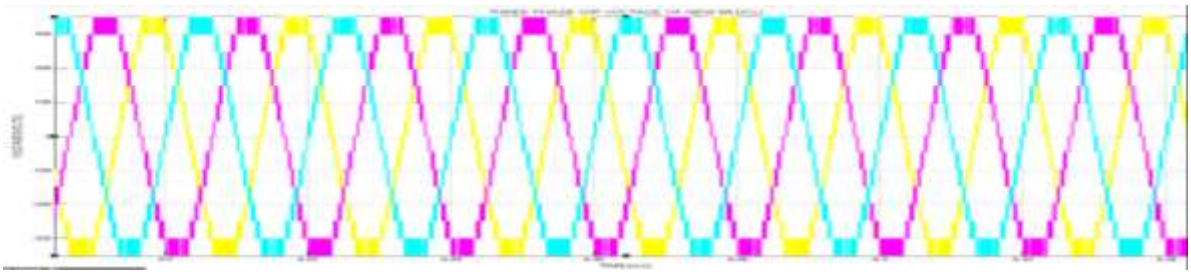

Figure 15. Three phase output voltage waveform

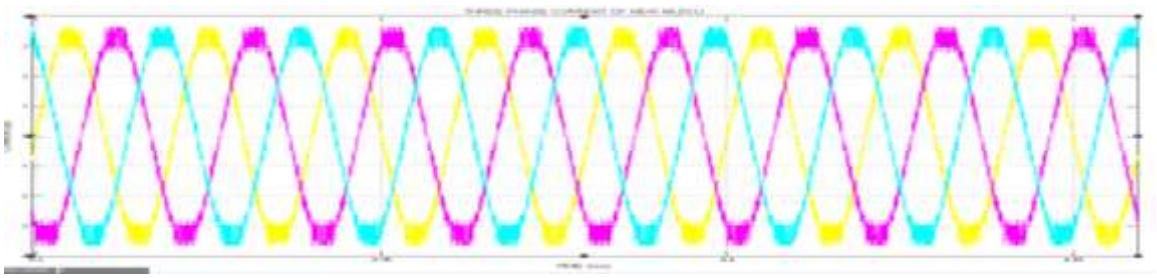

Figure 16. Current wave form of three phase circuit

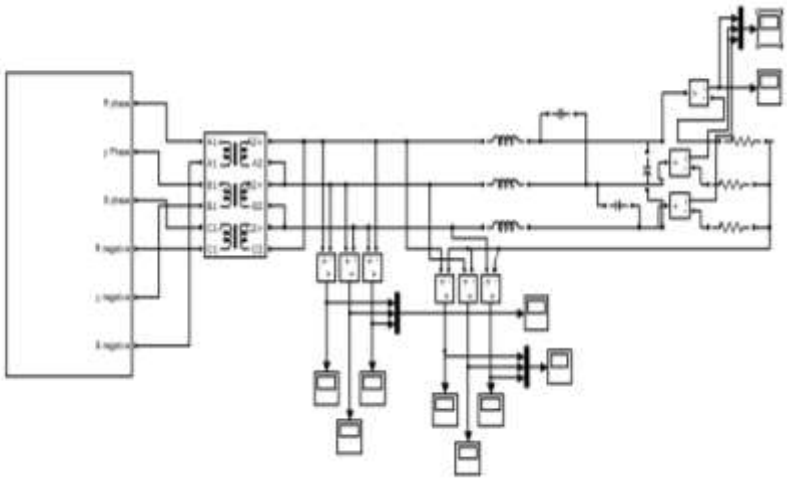

Figure 17. Three phase 15-Level Inverter for R Load with Filter

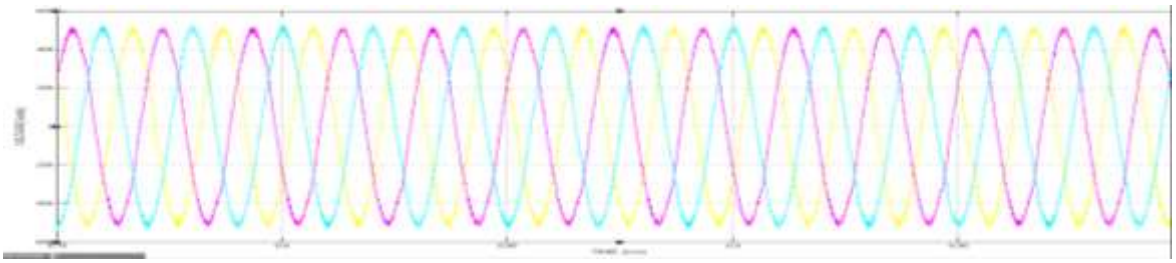

Figure 18. Three phase o/p voltage waveform for R-Load with LC filter

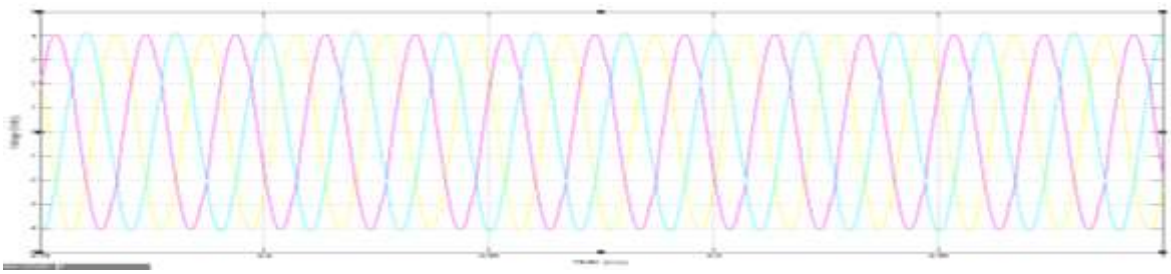

Figure 19. Three phase current waveform for R-load with filter

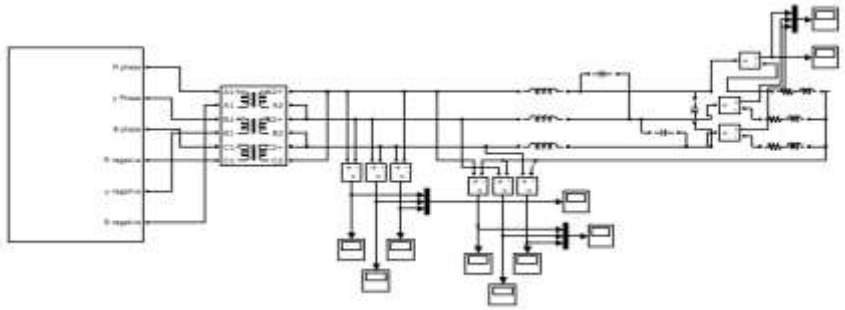

Figure 20. Simulation diagram of three phase prefeered MLDCLI for RL Load with filter

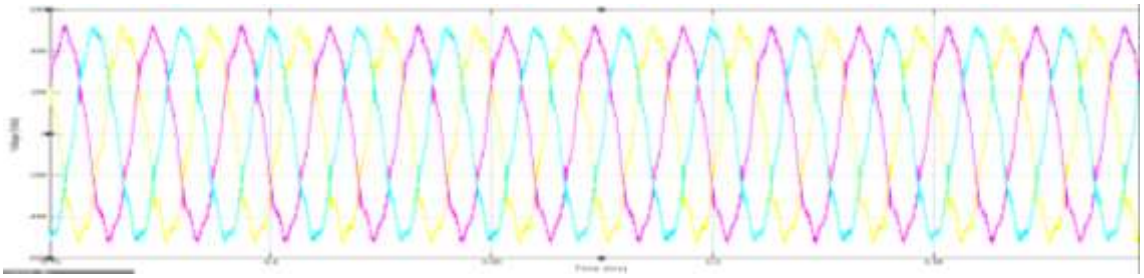

Figure 21. Three phase output phase voltage for RL-Load with filter

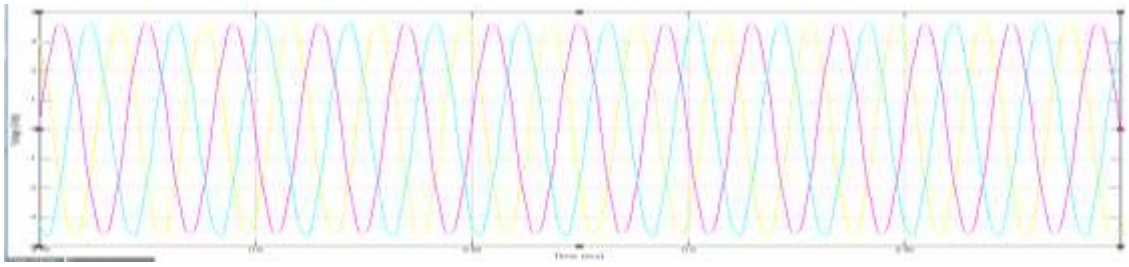

Figure 22. Output current waveform for RL-Load

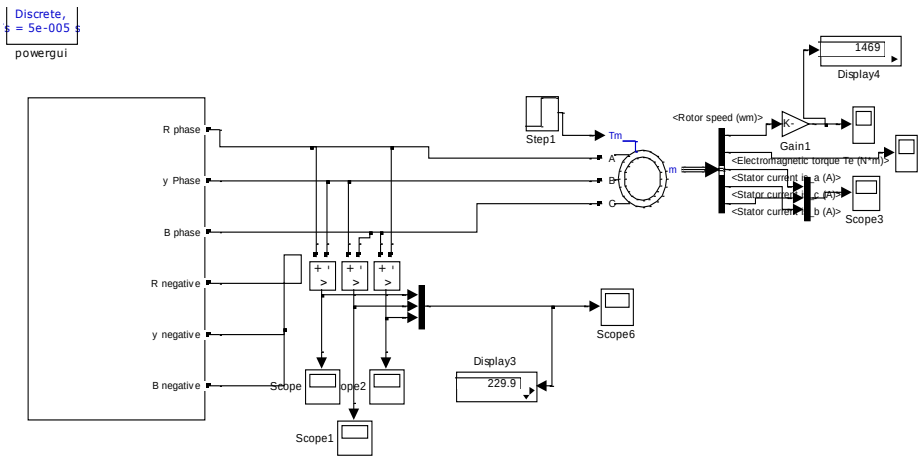

Figure 23. Simulation diagram of the preferred topolgy with Induction motor using Step torque

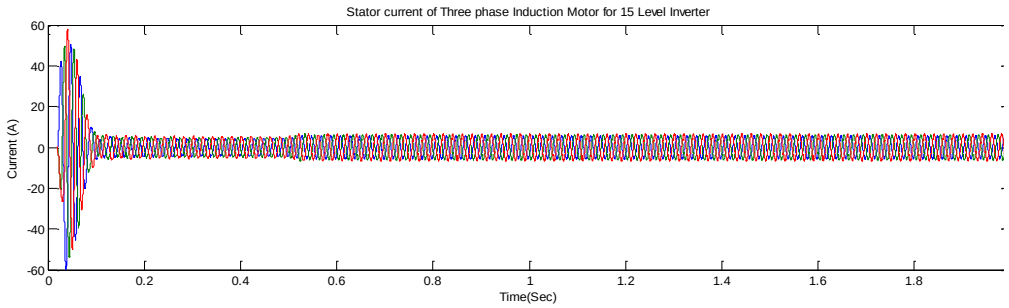

Figure 24. Stator current of three phase IM for 15-level inverter

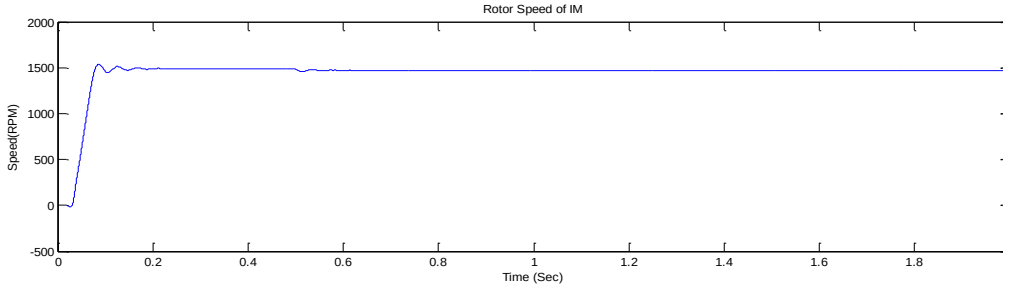

Figure 25. Rotor Speed of IM for 15-level inverter

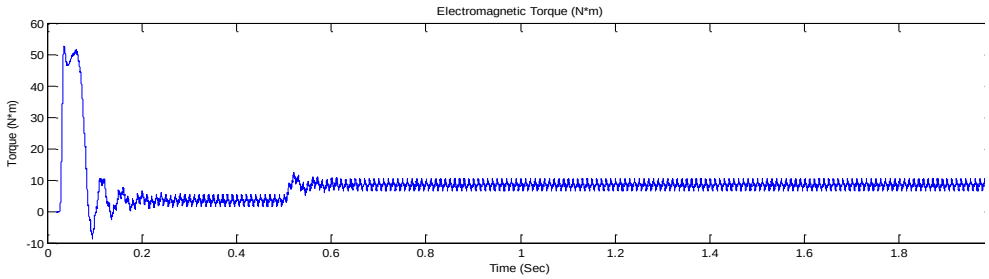

Figure 26. Electromagnetic torque of IM for 15-level inverter

Table 3. Result Analysis of Preferred MLDCLI with Filter

Switching Frequency	Phase Voltage			Load Current		
	V _peak	V_rms	THD%	I_peak	I_rms	THD%
2500	500.7	354.1	2.62	4.061	2.871	1.48
3000	501.7	354.8	2.79	4.069	2.877	2.33
3500	499.3	353.1	2.78	4.049	2.863	2.05
4000	502.6	355.4	2.63	4.076	2.882	2.02
4500	501.3	354.5	2.66	4.065	2.875	1.99
5000	498	352.2	3.07	4.039	2.856	1.90

Table 4. Result Analysis of Preferred MLDCLI without Filter

Switching Frequency	Phase Voltage			Load Current		
	V _peak	V_rms	THD%	I_peak	I_rms	THD%
2500	344.9	243.9	4.62	3.458	2.445	4.45
3000	345.7	244.5	4.27	3.439	2.432	4.31
3500	346.5	245	4.45	3.452	2.441	4.47
4000	348.4	246.4	4.69	3.471	2.454	4.72
4500	344.3	243.4	5.09	3.449	2.439	5.01
5000	344.3	243.4	5.12	3.432	2.427	5.33

Table 5. THD% Varying MI

MI	THD% of V_phase	THD% of Current
1	4.01	4.11
0.8	4.35	4.37
0.6	4.84	4.80
0.4	5.10	5.75

Table 6. %THD Varying MI Using Filter

MI	THD% of V_phase	THD% O/P Current
1	2.62	1.48
0.8	3.70	2.22
0.6	5.31	2.67
0.4	8.03	2.98

The performance of the preferred topology is compared with the traditional Cascaded H-Bridge (CHB) Inverter by varying the Modulation Index and it is observed that the % THD value is less in preferred topology than traditional CHB same is shown in Table 7.

Table 7. THD% Comparision of Prefered Topology with Traditional CHB inverter by Varying MI

MI	THD% of preferred topology	THD% of traditional CHB Inverter
1	4.01	9.03
0.8	4.35	10.41
0.6	4.84	10.83
0.4	5.10	12.57

Table 8 shows the comparision of % THD between preferred topology and the topology discussed in [16] and the % THD level is better than topology in [16].

Table 8. THD% Comparision of Prefered Topology with Topology in [16] Using Various PWM Techniques

PWM Technique	THD% of preferred topology	THD% of topology [16]
PD or IPD PWM	4.01	5.67
PODPWM	4.39	5.93
APODPWM	5.17	6.15

5. EXPERIMENTAL RESULTS

The simulation circuit discussed in section 4 is carried for hardware implementation and single phase fifteen level inverter of the preferred topology is tested for R Load and validated. SPARTAN-3A DSP from the FPGA family is considered as pulse generation module and the driving pulses as required patterns are developed using VHDL. Further, the generated pulses are diagnosed using ModelSim software. The experimental procedures are executed and the measurements are carried out with a scale division of 5A/div & 15 Volt/div. Figure 27 shows the hardware implementation of the topology and Figure 28show the flowchart for gate pulse generation in LG part, Figure 29 represents the output waveform of level generation unit having only positive polarity that is obtain experimentally with modulation index (MI) =1 and switching frequency=2KHz and Figure 30 and 31 shows the output voltage and current without and with filter respectively. Table 9, shows the % THD variation by varying MI and switching frequency

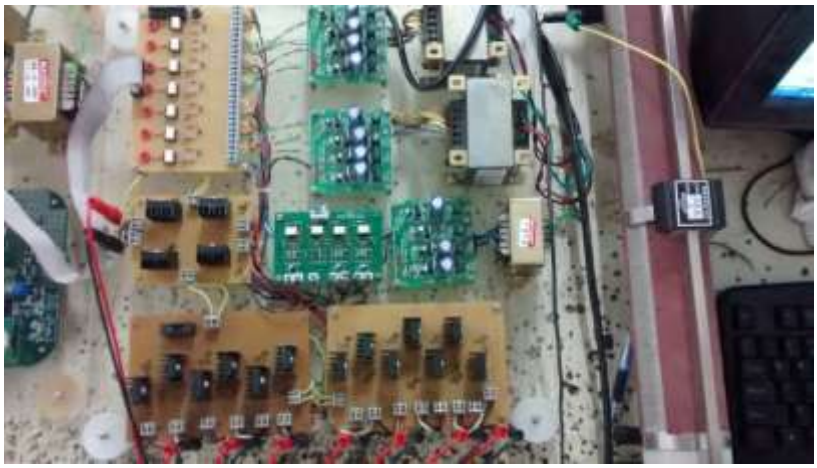

Figure 27. Experimental circuit of 15 level inverter

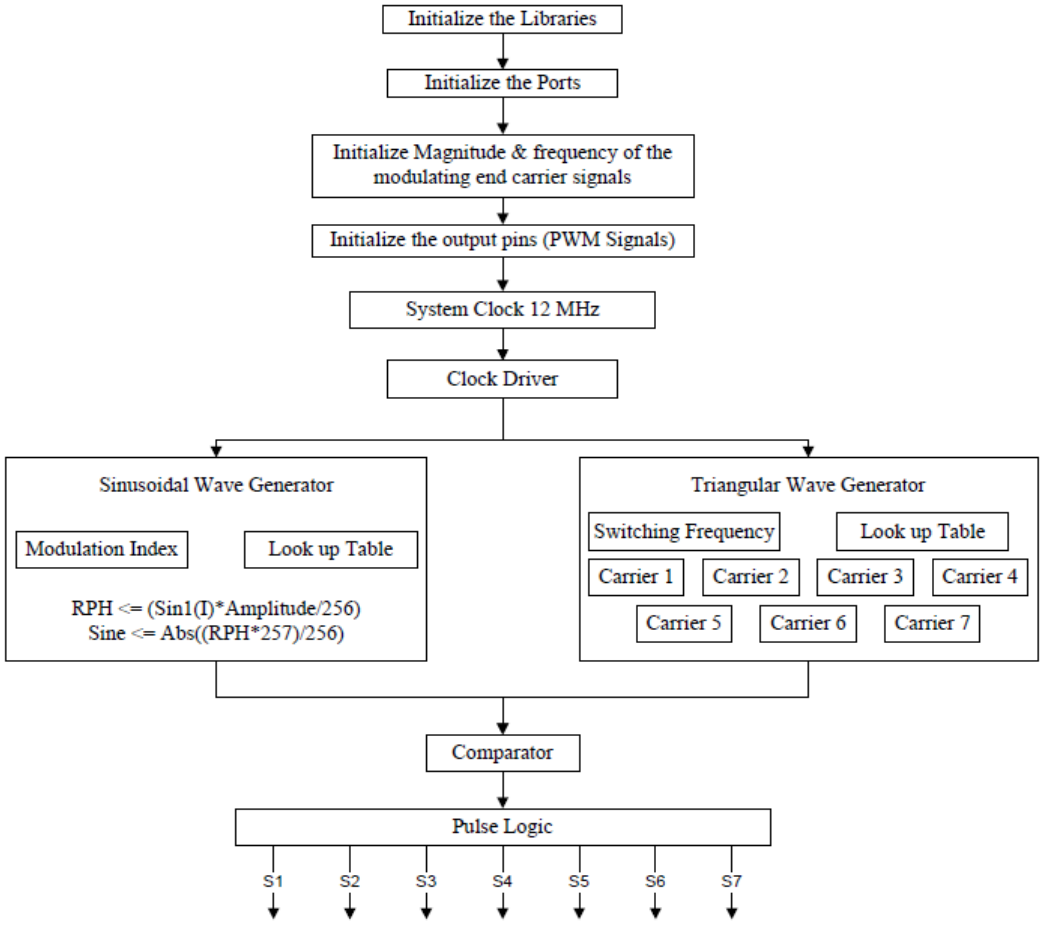

Figure 28. Flow chart for generating switching pulses for LG part using FPGA

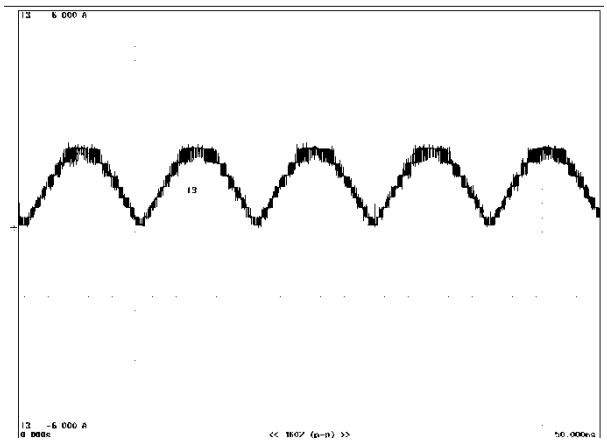

Figure 29. Out of level generation unit

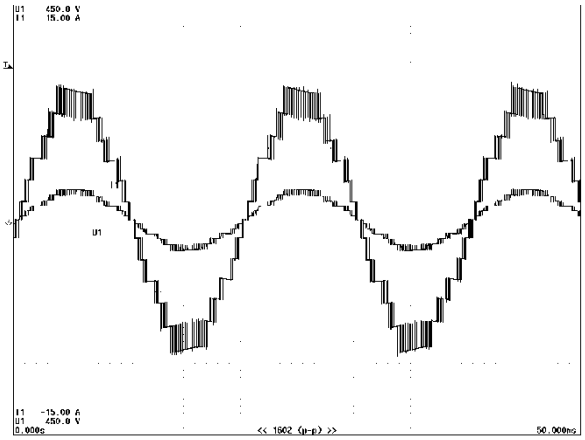

Figure 30. Output voltage and current for R load without filter

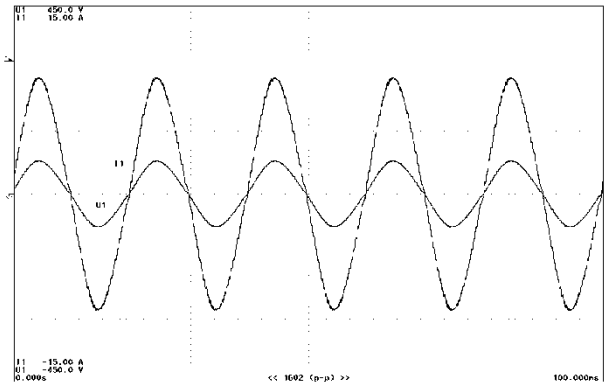

Figure 31. Output voltage and current for R Load with filter

Table 9. Comparison of % THD for R Load

MI	Switching frequency=2kHz				Switching frequency =5kHz				Switching frequency =10kHz			
	Voltage THD		Current THD		Voltage THD		Current THD		Voltage THD		Current THD	
	With out filter	With filter	With out filter	With filter	With out filter	With filter	With out filter	With filter	With out filter	With filter	Without filter	With filter
1	4.58	2.02	4.67	2.06	3.05	1.15	3.01	1.63	5.02	4.05	5.04	4.05
0.8	5.02	2.25	5.04	2.29	3.13	2.03	3.07	2.07	5.12	4.22	5.21	4.20
0.6	5.80	2.65	5.90	2.67	3.79	2.22	3.79	2.27	5.98	4.54	5.97	4.52

6. CONCLUSION

In this paper, a new inverter topology has been proposed which has superior features over conventional topologies in terms of the required power switches, control requirements, cost, and reliability. It is shown that this topology can be a good candidate for converters used in power applications such as FACTS, HVDC, PV systems, UPS, etc. In the discussed topology, the switching operation is separated into high- and low-frequency parts. This will add up to the efficiency of the converter as well as reducing the size and cost of the final prototype. The IPD-SPWM control method is used to drive the inverter. The simulation and experimental results of the topology for a fifteen-level inverter are shown in this paper. The results clearly show that the topology discussed can effectively work as a multilevel inverter with a reduced number of carriers for PWM and can be easily extendable to any required number of levels.

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