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An Ultra Low Power CMOS Sigma Delta ADC Modulator for System-on-chip (SoC) Temperature Sensor for Aerospace Applications

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ABSTRACT

In the current paper, an accurate with low power consumed sigma delta (ΣΔ) analog to digital converter has been designed for the aerospace applications. The sigma delta ADC has been designed in such a way that it works fine with consumption of low power and high accuracy in the system on chip (SoC) temperature sensor where the analog output from the temperature sensor unit will be the fed to the analog to digital converter. To check the robustness, different parameters with variation has been analyzed. The high gain operational amplifier plays a vital role in the circuits design. Hence, a 30 MHz operational amplifier has also been proposed whose unity gain bandwidth (UGB) has been observed of about 30 MHz, 51.1dB dc gain and slew rate (SR) of about 27.9 V/ µsec. For the proper operation of the circuit, a power supply of +1.3V to -1.3V is used. The proposed sigma delta ADC modulator is showing better results over previously designed modulator in terms of power consumption, error and performance. The design and simulation have been tested with the help of cadence analog design environment with UMC 90nm CMOS process technology.

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1. INTRODUCTION

The continuous innovation of technology has demanded an entire circuit system to be embedded on a single chip. System-on-chip temperature sensor requires a high performance, least inaccurate, more efficient, reliable and robust analog to digital converter which can be used to convert the analog signal receiving from the temperature sensor into digital domain. The data in digital domain is much safer, can be transferred, copied easily compared to analog domain. In terms of accuracy and high signal to noise ratio (SNR), sigma delta (ΣΔ) ADC is the best choice in compared to available ADC as they cannot gain very high accuracy. The sigma delta (ΣΔ) ADC comprises of two part i.e. sigma delta modulator and digital filter. The modulator part combines sampling at the rate equal and above to Nyquist rate with negative feedback while the preceding digital filter exchanges the amplitude for the resolution in time. Furthermore, sigma delta (ΣΔ) ADC has a capability to tolerate the imperfection of analog circuit up to great extend. Sigma delta (ΣΔ) provides the implementation of high density and complex analog circuit.

Therefore it becomes the first priority to realize in system-on-chip (SoC). The block diagram of sigma delta modulator is sjowun in Figure 1. The designed sigma delta (ΣΔ) ADC modulator consists of an integrator. The forward path of high order sigma delta (ΣΔ) ADC modulator contains more than one integrator which no doubt offers great resolution but unfortunately it suffers from potential instability [1], [2]. However, single order sigma delta (ΣΔ) ADC modulator may be cascaded to get precise gain. The order of

sigma delta (ΣΔ) ADC modulator varies with its applications. The input signal to sigma delta (ΣΔ) ADC modulator is sampled at high frequency and thus the conversion of analog signal into digital pulse takes place. The bad filtering process result into generation of digital pulse engulfed of unwanted noise [3], [4].

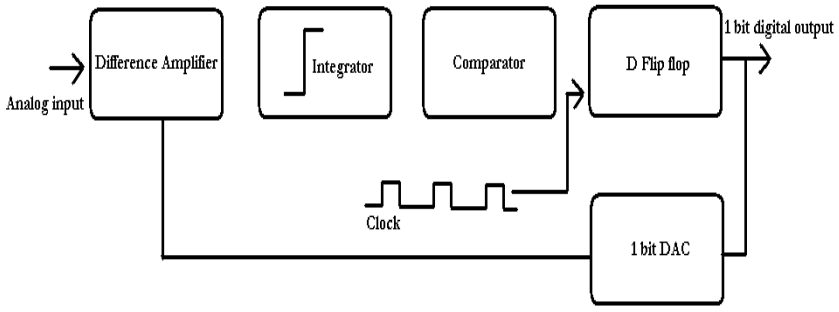

Figure 1. Block diagram of sigma delta modulator

The resolution of obtained output is directly dependent on the order of modulator and the sampling ratio which is decided at the modulator stage. Eariler the anti-aliasing filter was being considered but the principle of oversampling ratio ends the requirement of it, since now the analog input signal can be sampled directly using oversampling clock [6], [7]. Hence, an improved and accurate ultra low power sigma delta (ΣΔ) ADC modulator has been designed and argued in this paper. The rest of the article is patterned as follows. Section II enlightens the proposed circuit's configuration with the detailed depiction of each unit. Section III is dedicated to the results and discussion. Finally, section IV wraps up the work and the article ends with conclusions and acknowledges to the funding agency Indian Space Research Organization (ISRO) (India). The sigma delta (ΣΔ) ADC modulator shown in Figure.1 consists of a difference amplifier, an integrator, a comparator, a D flip flop and a DAC in the feedback loop of the modulator. The input analog signal has been passed through several processes like oversampling, quatization and noise shaping before it comes into pulse train at output. Both the conversion processess i.e. analog to digital (ADC) and digital to analog (DAC) conserves a vital space in modern technology [8], [9].

2. PROPOSED CIRCUIT CONFIGURATION

2.1. Operational Amplifier

The wide applications of operational amplifier make it a key ingredient to many analog systems. Basically it consists of a differential amplifier which amplifies the difference between two input signals. The differential amplifier also provides a required gain. To further improvise the gain of an operational amplifier, a second stage of common source stage is attached. Miller compensation technique has been implemented here for the stability of system. On the other hand, coupling capacitor found it place inbetween the common source amplifier's input and final stage of differential amplifier. Figure 2 shows the schematic of proposed operational amplifier. Mostly the feedback in operational amplifier is imposed to make the transfer function of system independednt of gain. But in high frequency applications, as the frequency increases, gain slightly decreases and making transfer function unstable. To avoid this unstablilty, op-amps must be chosen of broad band for high frequency applications. The sizes of different transistors used in Fiigure 2 are tabulated in Table 1.

The two stage architecture has the disadvantage of having two impedance nodes which are indicated by A and B due to which two pole will be dominant which will deteriorate the phase margin of the op amp. Hence, a Miller capacitance (C_C) has been introduced between A and B to resolve it. The chosen value must satisfy the following equation [10].

$$C_C = (2.2/10)C_L \quad (1)$$

Where, coupling capacitor is denoted by C_c while load capacitorn is expressed as C_L. Similarly, the unity gain bandwidth product (GB) is termed as,

$$B = {g_{m1}}/{C_C} \quad (2)$$

Where, g_{m1} is the input transconductance. For the gain-bandwidth product to be high the input transconductance should be high, by making the channels of MN1 and MN2 wide. Similarly the output capacitance should be low.

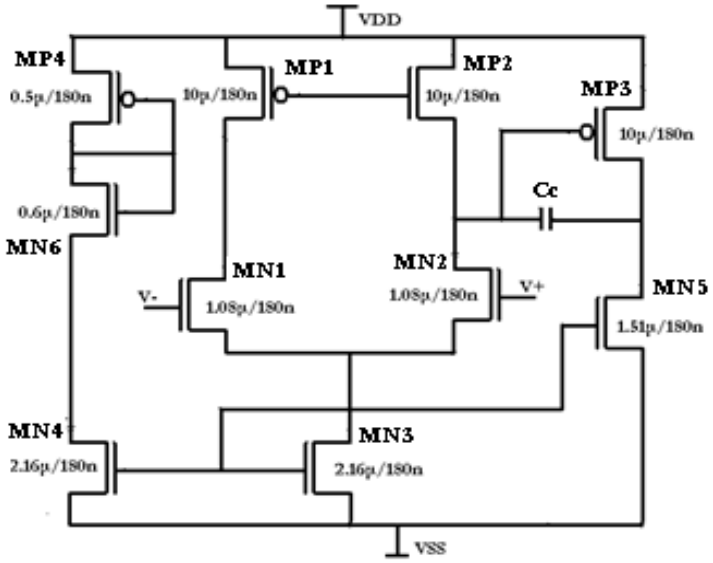

Figure 2. Proposed schematic of Op-amp

Variation in W and L can be made by using following Equation (3).

$$g_m = \sqrt{2\mu_p C_{ox} {W}/{L} I_d} \quad (3)$$

Slew rate decides the current flowing in the transistor MN5, and is determined by how fast can be charged and discharged. This is given by Equation (4)

$$Slew\ Rate = {I_s}/{C_C} \quad (4)$$

The aspect ratio of transistor MP3 is decided by the positive input common mode range. Output pole should be assumed at the location which is approx 2.2 times for phase margin of 60°. Hence, g_{m6} is determined by the following Equation (5)

$$g_{m6} = 2.2 g_{m2} \left({C_L}/{C_C}\right) \quad (5)$$

Table 1. Sizes of Transistor Utilized in Circuit 2

Transistor	Width (W)	Length (L)	Used in
MP1	10µm	0.18 µm	Fig.2
MP2	10µm	0.18 µm	Fig.2
MP3	10µm	0.18 µm	Fig.2
MP4	0.5µm	0.18 µm	Fig.2
MN1	1.08 µm	0.18 µm	Fig.2
MN2	1.08 µm	0.18 µm	Fig.2
MN3	2.16 µm	0.18 µm	Fig.2
MN4	2.16 µm	0.18 µm	Fig.2
MN5	1.51 µm	0.18 µm	Fig.2
MN6	0.6 µm	0.18 µm	Fig.2

2.2. Difference apmlifier and integrator

Difference amplifier comes under the list of applications of operational amplifier. The design of difference amplifier uses two stage operational amplifier. Since it shows good voltage gain, CMRR, slew rate, it is adopted here. The difference amplifier is basically having two input terminals i.e. V_2 and V_1 and one output terminal (V_{out}). The output is the difference of the two inputs. On the other hand, The CMOS integrator performs mathematical operation on input and produces an output which is proportion to the integral of the input voltage. Figures 3 and 4 show the schematic of difference amplifier and integrator. Integrator is the important building block used in the design of continuous time filters [11]. The change in the combination of resistance and capacitor values changes the value of RC time constant which further affects the rate of change of output voltage.

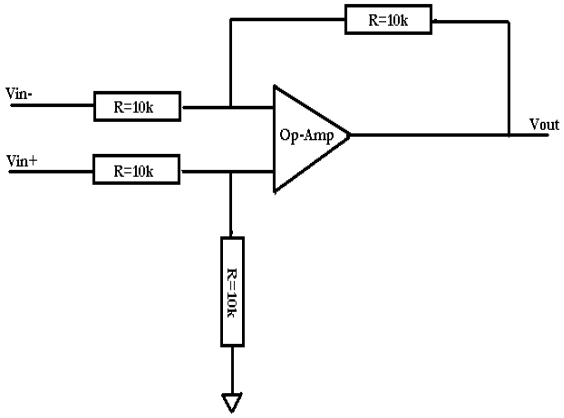

Figure 3. Schematic of difference amplifier

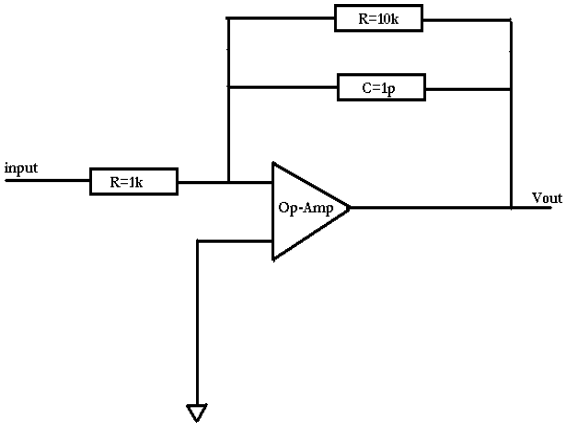

Figure 4. Schematic of integrator

Ideally the summation of previous output $v(kT-T)$ and previous input $u(kT-T)$ gives the output of the integrator.

$$v(kT) = g_0 u(kT-T) + v(kT-T) \quad (6)$$

The constant g_0 represents the gain preceding the input to integrator. Equation (6) is corresponding to the transfer function of an ideal integrator shown in Equation (7).

$$H(z) = \frac{g_0 z^{-1}}{1-z^{-1}} \quad (7)$$

2.3. Comparator

In compare to other units of sigma delta (ΣΔ) ADC modulator, comparator is the most fundamental component as the comparison of two different analog inputs signal and make out of single digital output signal have been done in this unit. It has a vital impact on the performance and reliability of the designed circuit. The schematioc of proposed comparator is shown in Figure 5. The input offset voltage, delay and the range of the input signal decides the speed and resolution of analog to digital converter [12].The basic property of the comparator is to take the analog input and gives a binary or digital output. Clocked comparators are often called dynamic comparator. Regenerative feedback is often used in dynamic comparator and occasionally in non clocked comparator. Dynamic comparator is used in the design of high speed ADCs.

2.4. D flip flop

The used D flip flop has three interconnected RS latch circuits. In designing, any of NAND or NOR can be used. When clock gets logic 1, the output latch gets isolated from any input changes as the output of the two middle input gates is forced to get logic 0. On the other hand, the input latych with an illegal state will automatic resume its latching action, when logic 0 is triggered by clock. Figure 6 depicts the schematic of proposed D flip-flop.

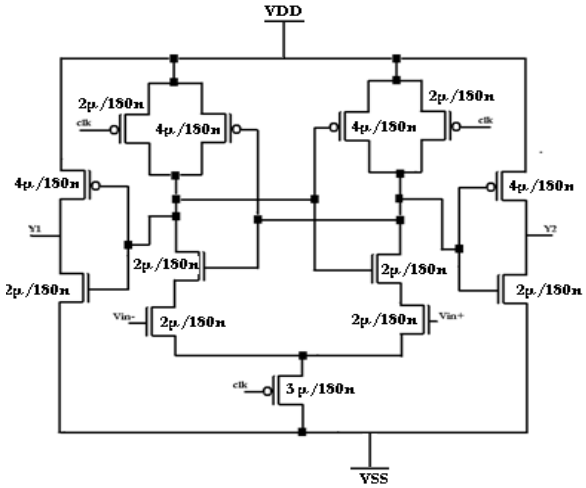

Figure 5. Proposed schematic of comparator

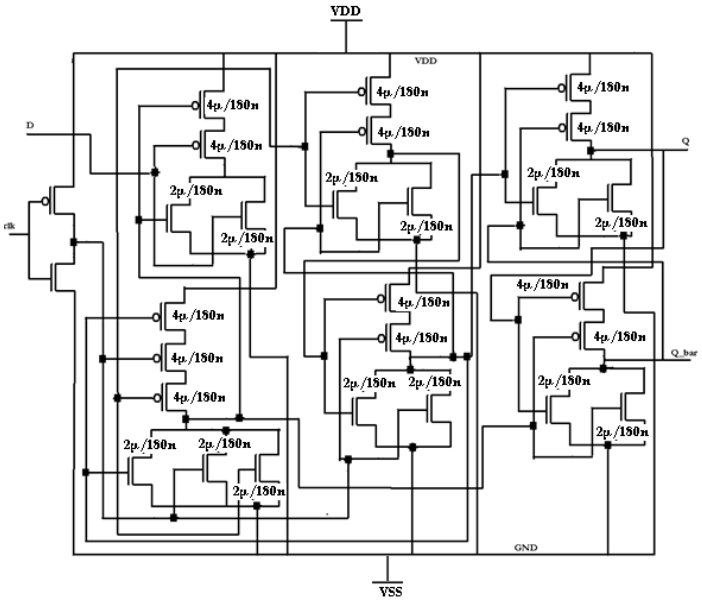

Figure 6. Proposed schematic of D flip-flop

2.5. 1 bit DAC

Basically digital signal or code is converted into analog voltage or current by using digital to analog converter (DAC). The DAC is comprised of reference voltage (V_{ref}), supply voltage (V_{dd}) and analog output. True analog quantity has not been observed at the output of the digital to analog converter (DAC). The schematic of proposed 1 bit DAC is shown in Figure 7. The output is found in pseudo analog quantity. The number of input bits should be increased, since the obtained analog output is propotional to its digitalpulse input. Therefore the step size gets reduced and due to higher number of bits, the output seems to b analog signal.

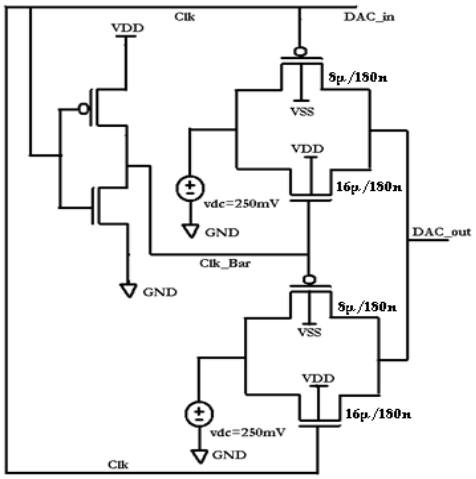

Figure 7. Proposed schematic of 1 bit DAC

3. RESULTS AND ANALYSIS

The components and the final designed sigma delta modulator are simulated using UMC 90nm. The output gain of operational amplifier is depicted in Figure 8. While the simulated results of difference amplifier as shown in Figure 9, integrator as shown in Figure 10, Comparator as shown in Figure 11, D flip-flop as shown in Figure 12, 1bit DAC as shown in Figure 13 and sigma delta modulator as shown in Figure 14. Comparison of work done in this paper has been compared in Table 2.

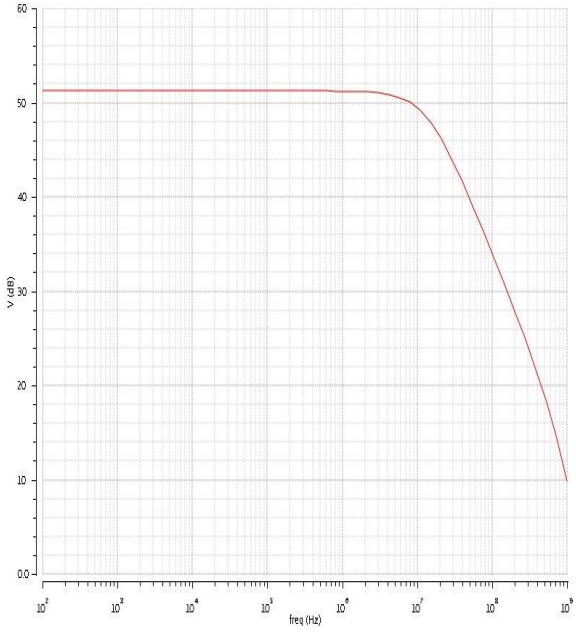

Figure 8. Output gain of operational amplifier

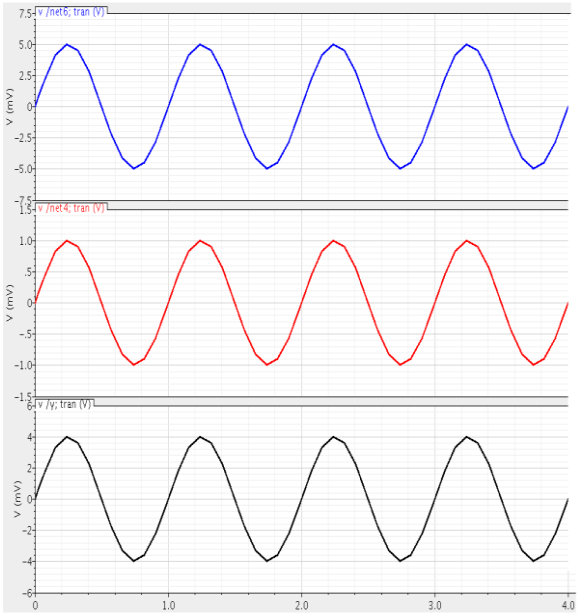

Figure 9. Output result of difference amplifier

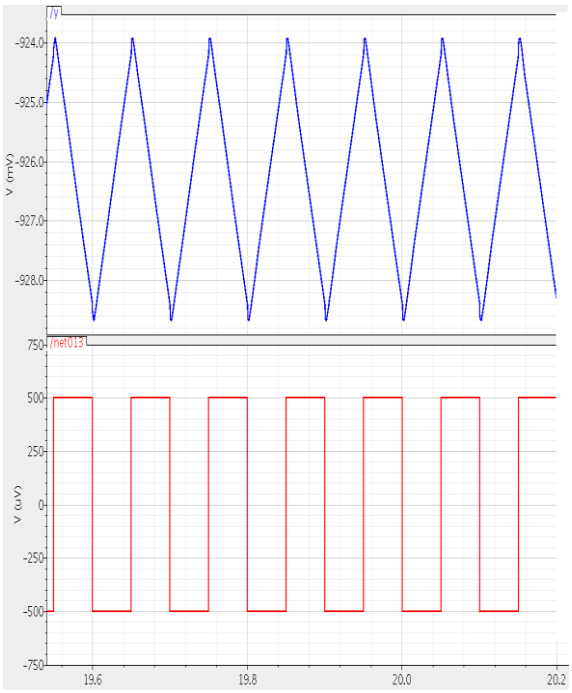

Figure 10. Output result of integrator

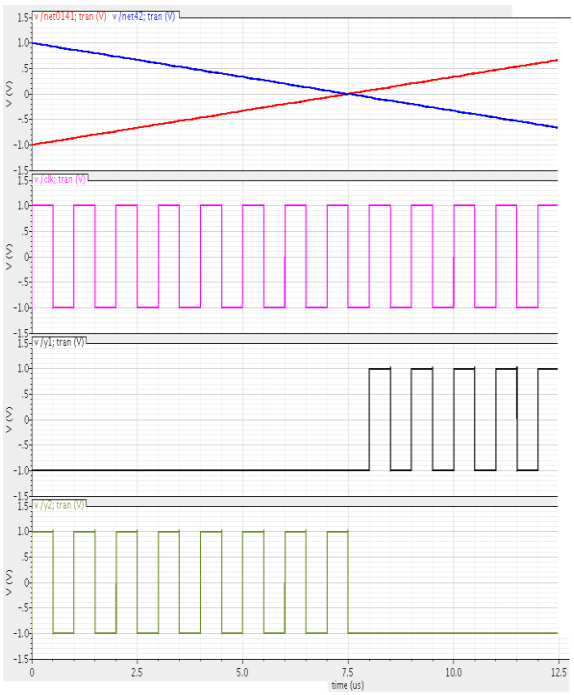

Figure 11. Output result of clocked comparator

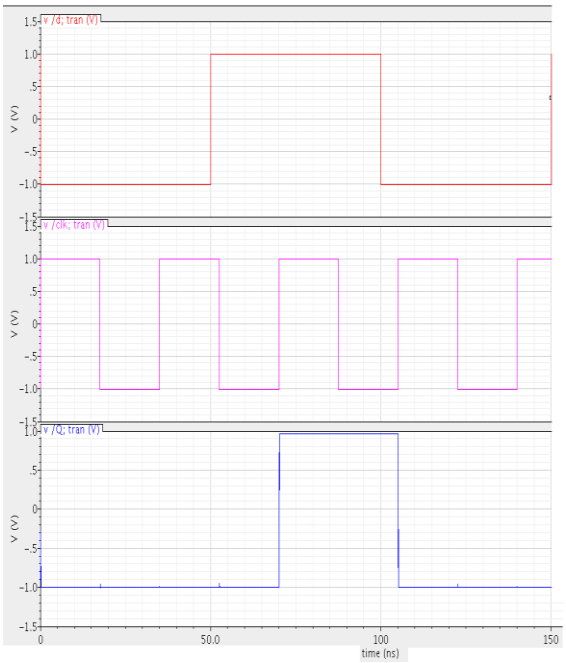

Figure 12. Output result of D flip flop

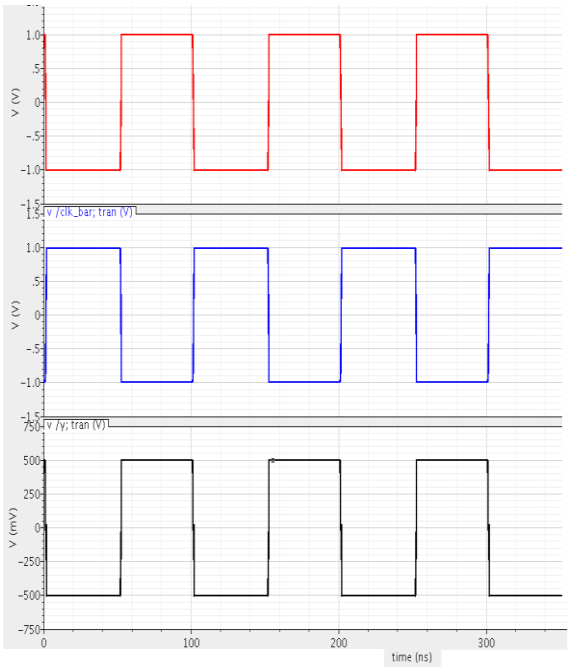

Figure 13. Output result of 1 bit DAC

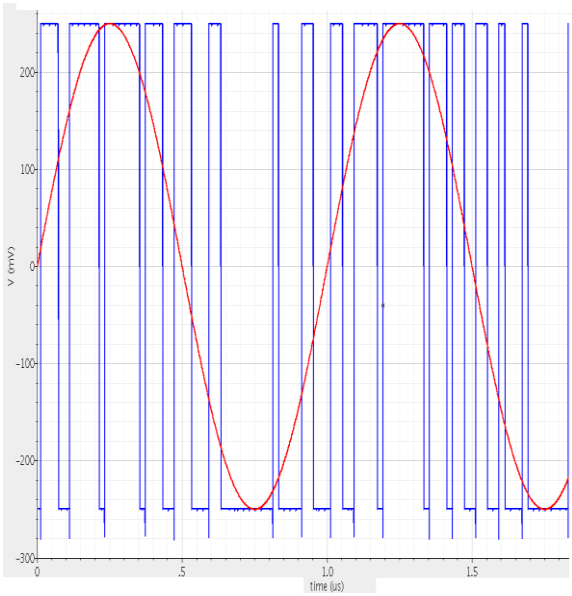

Figure 14. Output result of Sigma Delta (ΣΔ)

Table 2. Comparison with Some Other Recent Work

Factor	[5]	[13]	[14]	[16]	[17]	[18]	[15]	[19]	This Work
Process Technology	0.18µm CMOS	130nm CMOS	180nm CMOS	MATLAB	0.18µm CMOS	0.35mm CMOS	0.35 µm CMOS	0.13nm CMOS	90nm CMOS
Architecture	Flash	Sigma Delta	Sigma Delta	Sigma Delta	Sigma Delta	Sigma Delta	Flash	Flash	Sigma Delta
Input Voltage	0 to 1.8V	1V	2V		1V	3.3V	3V	1.5V	1.3V
SNR	---	78dB	---	82dB	85.2dB	85dB	73 dB	--	62dB
Power dissipated	36.23mW	68µW	6.45µW	--	1.96mW	200mW	341mW	160mW	54µW

4. CONCLUSION

In the present paper, an ultra low power sigma delta (ΣΔ) ADC modulator which is highly useful in system on chip (SOC) temperature sensor for aerospace applications has been described. Comparison of work done in this paper has been compared in Table 2. The each unit of sigma delta delta (ΣΔ) ADC modulator is examined and modeled here. The proposed sigma delta delta (ΣΔ) ADC modulator works utilizing minimal power supply of +1.3V to -1.3V. The average power of 54 µW is dissipated with the smapling frequency of 50MHz.

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