

Implementation of High Speed Vedic Multiplier Using Vertical and Crosswise Algorithm

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ABSTRACT

Multiplication is an important fundamental function in arithmetic operations. Multiplication-based operations such as Multiply and Accumulate (MAC) and inner product are some of the frequently used operations in many Digital Signal Processing (DSP) applications such as convolution, Fast Fourier Transform(FFT), filtering and in microprocessors in its arithmetic and logic unit. Since multiplication dominates the execution time of most DSP algorithms, so there is a need of high speed multiplier. Higher throughput arithmetic operations are important to achieve the desired performance in many real-time signal and image processing applications. In this project, the comparative study of Vedic multiplier and Sequential multiplier is done for low power requirement and high speed. The proposed architecture is based on the Vertical and Crosswise algorithm of ancient Indian Vedic Mathematics, which increases the speed of multiplier by reducing the number of clock cycles thus achieving the greater speed of the processor or system.

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1. INTRODUCTION

In computers, considerable amount of processing time is spent by the CPU on implementing arithmetic operations, particularly multiplication operations and it requires substantially more hardware resources and processing time than addition and subtraction. In fact, 8.72% of all the instruction in typical processing units is multipliers [1].

Thus multiplication time becomes one of the dominant factor in determining the instruction cycle time of a processor. The need for high speed processing is increasing as computer and signal processing applications are expanding and the development of fast multiplier circuit has been a subject of interest over decades[2]. In the binary multiplier, multiplication is implemented generally with a sequence of addition, and shift operations. Multiplier based on Vedic Mathematics is one of the fast and low power multiplier. This optimization includes the circuit style and topology, the architecture for implementing the circuits. Employing this technique in the computation algorithms will reduce the complexity, execution time, power. The method can also be used to compute NxN multiplication, by reducing the NxN structure into an efficient 8x8 multiplier structures [3].

2. RESEARCH METHOD (URDHVA TIRYAKBHYAM)

The proposed multiplier algorithm is based on Urdhva Tiryakbhyam Sutra of ancient Indian Vedic Mathematics. Urdhva Tiryakbhyam Sutra is a general multiplication formula applicable to all cases of

multiplication. It literally means “Vertically and crosswise”. It is based on a concept of generating of all partial products in parallel (at once) and the final result is obtained by adding these partial products concurrently as shown in Figure 1. It should be clearly noted that carry may be a multi-bit number [4]. This algorithm traditionally used for the multiplication of two numbers in the decimal number system. In this work, the same logic is used for the binary number system to make the proposed algorithm compatible with the digital hardware.

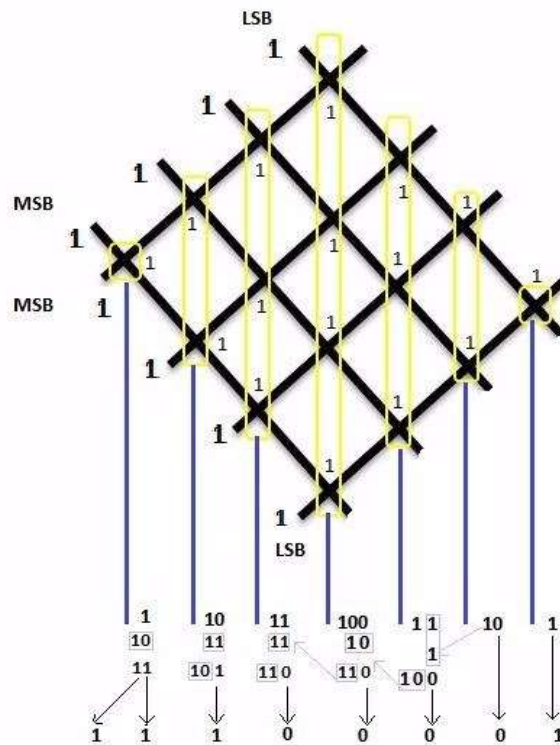


Figure 1. Vertically and crosswise multiplication

To illustrate the multiplication algorithm, we have considered the multiplication of two binary numbers $a_3a_2a_1a_0$ and $b_3b_2b_1b_0$. As the result of this multiplication would be more than 4 bits, we express it as $r_7r_6r_5r_4r_3r_2r_1r_0$. The circuit is designed making use of the proposed method and carry look ahead adder concept. The circuit makes use of 72 logic gates and the design is implemented using Circuit Maker software. The expressions used to calculate final product is shown in Figure 2 and the circuit diagram is shown in Figure 3 respectively. In the Vedic Multiplier each multiplicand bit is multiplied with all the bits of the multiplier, starting from MSB. The products are arranged (crosswise) as shown in Figure 4.

Then the bits are added vertically, the carry generated from the lower bit addition is added to the next stage sum, by using the carry look ahead method. Note that the carry generated may be multi bit. Thus sum obtained by the crosswise and vertical multiplication and addition of bits of the two numbers. The example of decimal number multiplication is illustrated in the Figure 4. The general sequential multiplier makes use of shifter and adder. Thus to generate the result of 4×4 multiplication requires 4 shift operations to generate the 16 product terms plus addition of these partial product terms. The flowchart of the sequential multiplier is given in Figure 5. Figure 6 and Figure 7 illustrates the binary multiplication by sequential and Vedic method respectively. Absence of the shift operation in the Vedic multiplier not only increases the speed of the operation but also helps in reducing the area and power required for the design [5], [6].

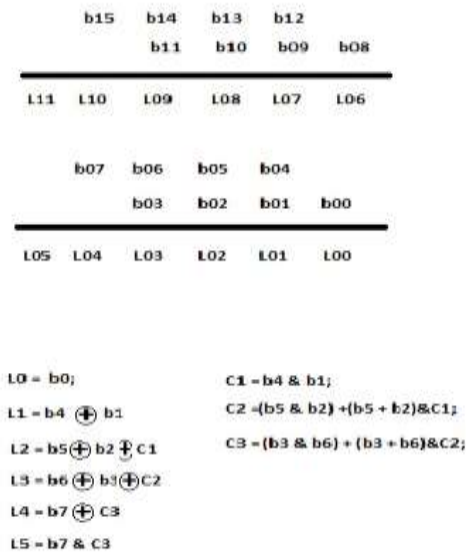


Figure 2. Carry look ahead equations

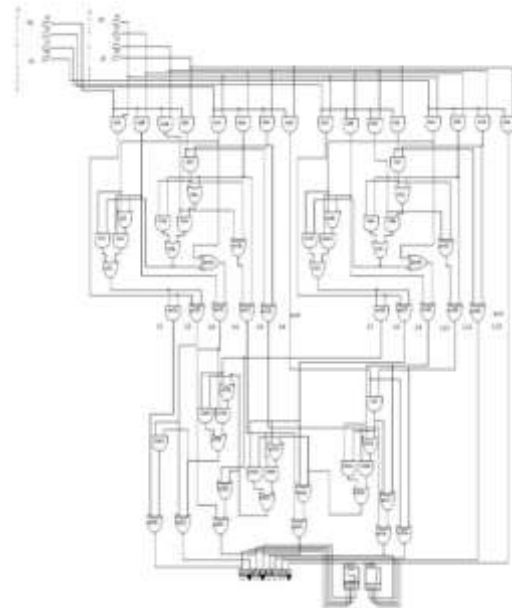


Figure 3. Architecture of Vedic multiplier

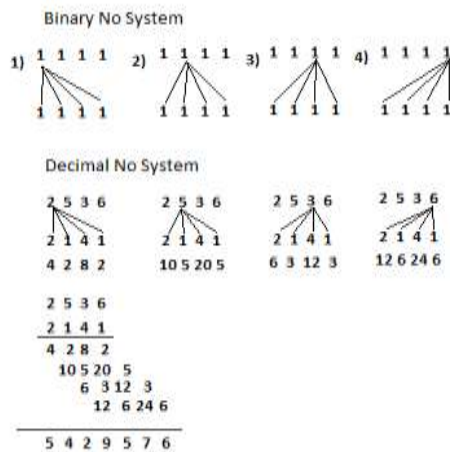


Figure 4. Multiplication of two 4-bit numbers

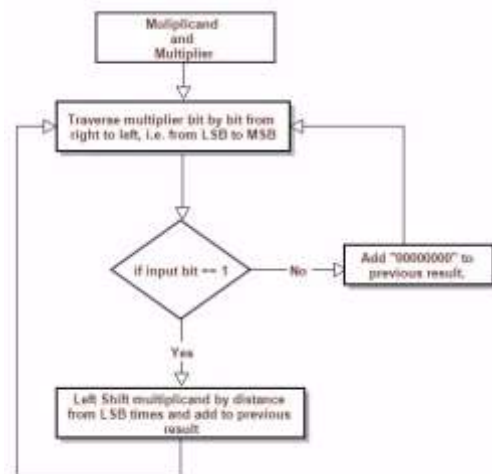


Figure 5. Flow chart sequential multiplier algorithm

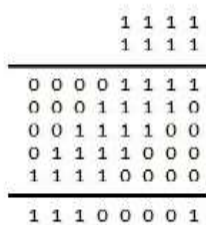


Figure 6. Binary multiplication by sequential method

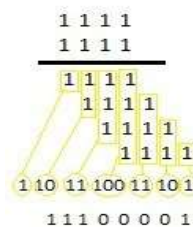


Figure 7. Binary multiplication by Vedic

3. RESULTS

The multiplier has been implemented using Verilog HDL. Timing dig and Synthesis result is obtained for both the multipliers. Delay in Vedic multiplier for 4 x 4 bit number is around 10ns while the

delay in Sequential multiplier is around 50 ns. The simulation results of Vedic multiplier and Sequential multiplier are shown in Figure 8 and Figure 9 respectively.

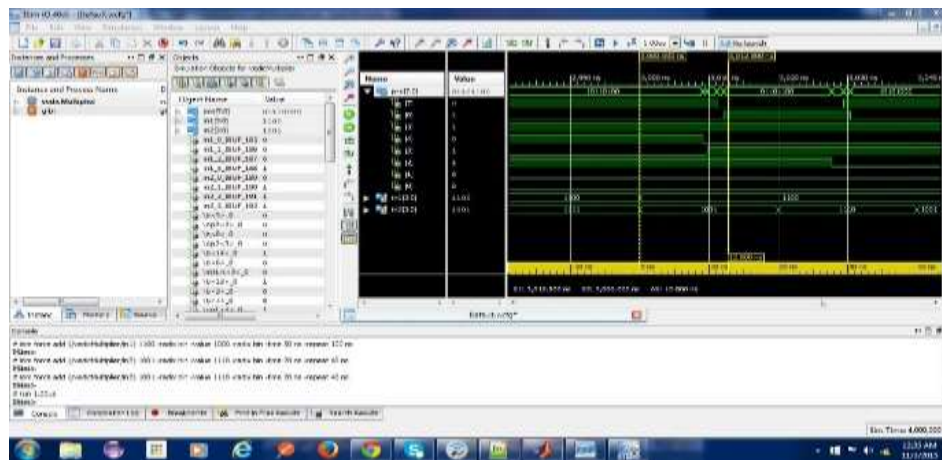


Figure 8. Simulation result of Vedic multiplier

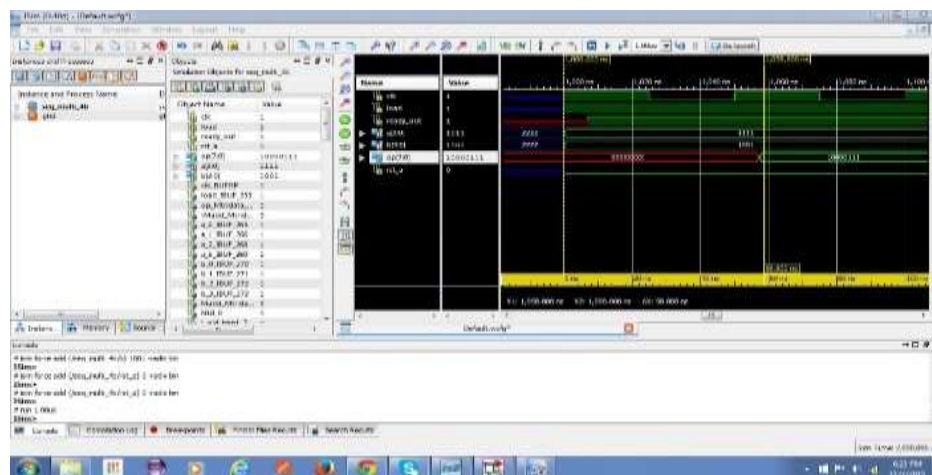


Figure 9. Simulation result of sequential multiplier

4. CONCLUSION

This hardware design of Vedic can be looked as similar to the array multiplier. All the partial products are calculated in parallel and the delay associated is mainly the time taken by the carry to propagate through the adders plus the partial products generation from the logic gates. As the number of bits increases for 8x8 bits, 16x16 bits the timing delay is greatly reduced for Vedic multiplier as compared to other multipliers. Vedic multiplier has the greatest advantage as compared to other multipliers over gate delays and regularity of structures.

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