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BIST Architecture using Area Efficient Low Current LFSR for Embedded Memory Testing Applications

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ABSTRACT

One of the important block of BIST controller is LFSR and the speed with which BIST operates depends on LFSR systems design. There are methods in implementing LFSR using field programmable gate arrays (FPGAs) or digital signal processors (DSPs). BIST controller system speed is then limited to FPGAs and DSPs, which may influence other parameters such as overall area, maximum current, limit and power dissipation. This paper proposes a technique to achieve an efficient BIST controller by redesigning LFSR using GDI based D flip-flops that resulted with low area and low current capabilities. This paper presents three different techniques for implementing flip-flops for an efficient LFSR so that the layout area will be minimized as well as the maximum current drawn will be lower.

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1. INTRODUCTION

Similar to a shift register, a Linear Feedback Shift Register (LFSR) shifts the signal from one bit to next bit when applied with the clock. Based on seed input bits, some of the outputs from the register are combined through the Ex-OR gate configuration and further a feedback mechanism will be formed to provide that as input to LFSR. Although much work has already carried out by different techniques, it is still a challenging work for circuit designer to design an optimized and reliable circuit. Many of the techniques are focussed on minimizing the power dissipation at different levels and are circuit, architecture, layout, and process technology level. Some researchers are claimed that reasonable amount of power saving can be attained at the circuit design level by properly choosing a logic style for implementing combinational circuits [1]. The same was observed while implementing various flip-flop circuits using CMOS transistors with voltage and gate size scaling technique that reduces power dissipation without distorting the normal function of the basic flip-flops [2].

LFSR uses flip-flops, which are to be connected in series along with a feedback circuit constructed according to generator polynomial. Initially the primary seed is to be loaded in the outputs of the flip-flops, and then using an external clock a random sequence will be generated. Each clock pulse can produce a unique pattern at the output of the flip-flops against to the test input. The number of flip-flops in general will be chosen according to the number of inputs required by the circuit under test. Each input combination becomes a test pattern that can run on the circuit under test for desired fault coverage. If each input vector is unique and no correlation between the successive vectors then the applied stimuli for a circuit under test can result in much higher power consumption by the device than the budgeted power.

It is observed that, there are many innovative ideas and solutions are put forth for the power optimization by many researchers such as reverse body bias, transistor stacking, and LFSR design with parallel architecture, pipelining and retiming algorithms and reversible logic. The BIST controller consists of a test pattern generator, which can be a standard linear feedback register, counter, or cellular automata.

Aiming at power and hardware reduction a test pattern generator FC-LFSR [3,4] is designed that generates intermediate patterns between the random patterns.

A new pattern generation technique is implemented for low power using a modified conventional LFSR, in which shift registers may be implemented by using pulsed latches and flip-flops. However, shift register implemented by pulsed latches have power and area problems .So, flip flops are preferred over pulsed latches [5].

As an inherent behaviour of flip-flops, their output at any instant of time depends on the present input as well as on past output, hence they are known as memory elements. NOT, OR, AND, NOR, NAND, CMOS latches are used to build these memory elements. Variety of applications can be seen by flip-flops, for example, a JK flip-flop is used in sequential circuits as data processor. Since majority of the applications operate on the battery power dissipation becomes the major constraints [6,7].

Recently reported logic style based on flip-flops [8] claimed that the complementary pass-transistor logic (CPL) to be much more power-efficient than complementary CMOS. However, the performance in terms of speed, area, power dissipation, and power-delay products of efficient CMOS circuit realizations using variety of different logic cells [9-17] demonstrate that the CMOS is superior to CPL. However, there is always demand for new techniques with respect to low power or low area considerations, in this paper JK flip-flop is redesigned using various logic styles such as pass transistors, and transmission gates which is discussed in section II. Observed that the implementation of JK flip-flop using complementary CMOS has a power-delay product less than half that of the CPL version. Further JK flip-flop is implemented using GDI logic and observed much greater improvement in the performance. Low voltage, low area, and small delay are of concern, this paper shows that GDI based JK is the logic style of choice for further implementations of D FF and LFSR as discussed in section III. Results and comparisons are discussed in section IV. Conclusions are in section V.

2. RESEARCH METHOD: REDESIGN OF JK FLIPFLOP USING CMOS LOGIC

Similar to R-S flip-flop, JK outputs follow the inputs when the Clk is on. If J and K are different then the output Q takes the value of J at the next clock edge. If J and K are both low then no change occurs. Toggle state occurs when J and K are both given a high state. This eliminates the ambiguous states resulted in RS flip-flop. Further, this toggle condition finds many applications in binary counters and in frequency division that found in prescalars. One can observe a problem with the basic J-K Flip-flop is that spikes can appear on the output and due to these unstable state results when both J & K inputs are tied to logic '0'. A 'latch' circuit of can be used to avoid this spike hence outputs Q and Q' are isolated from the inputs J & K as shown in Figure 3. Circuit and corresponding truth table of J-K flip-flop are shown in Figure 1 and Table 1.

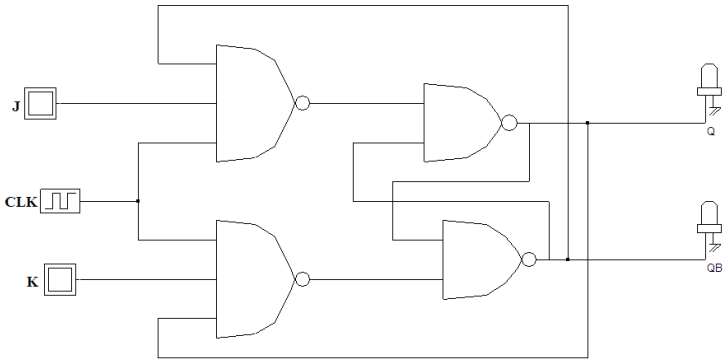

Figure 1. Schematic of JK flip-flop

Table 1. Truth Table of JK Flip-flop

J	K	CLK	Q
0	0	↑	Q(No Change)
1	0	↑	1
0	1	↑	0
1	1	↑	QB(Toggles)

The propounded CMOS based JK schematic circuit is shown in Figure 2 is designed by using strong 1 (pull up) and strong 0 (pull down) transistors namely pMOS and nMOS transistors. It uses 20 transistors, out of them 10 are nMOS transistors and 10 are pMOS transistors. The efforts are done to give the common VDD supply to reduce the power. Corresponding timing diagram, is shown in Figures 3-5 respectively

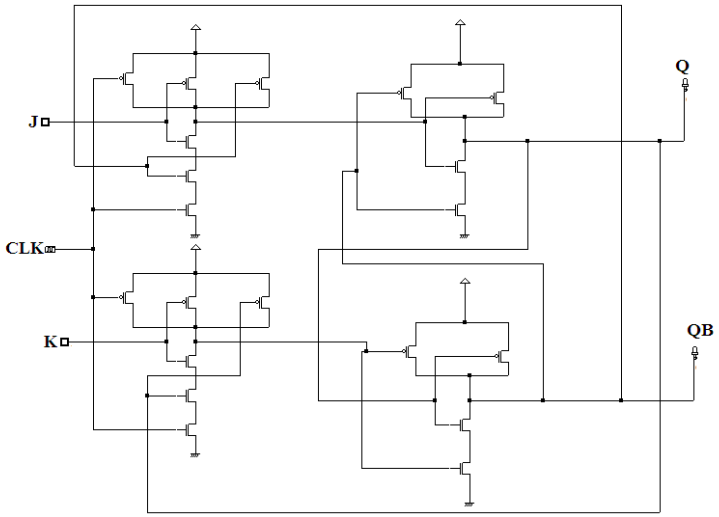

Figure 2. Schematic of CMOS based JK flip-flop

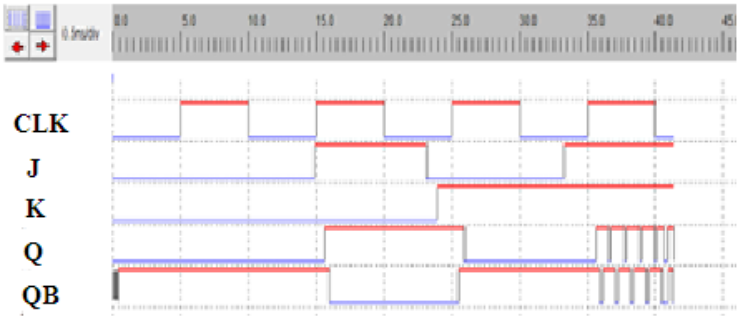

Figure 3. Transient waveform of CMOS based JK

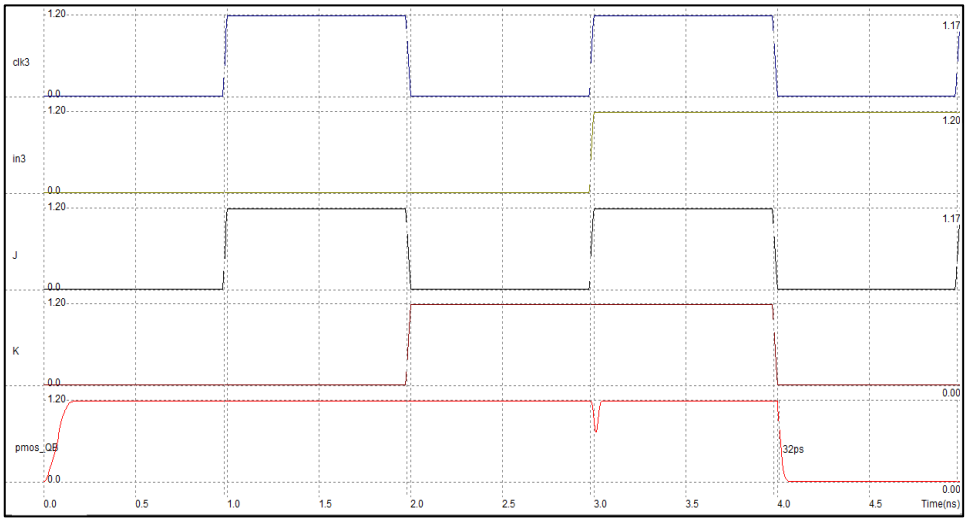

Figure 4. Microwind based simulated waveform for JK flip-flop using CMOS logic

2.1. JK flipflop using GDI (Gate diffusion input) logic

GDI methodology allows implementation of a wide range of complex logic functions using only two transistors. Compared to traditional CMOS logic, and existing PTL the combinatorial and sequential logic designed by GDI resulted in significant reduction in area and power dissipation.

The main drawbacks associated with GDI include: The bulk terminals are not properly biased thereby the circuit exhibits threshold drop and variation in Vt. Because of floating bulk, the cells can be implemented in SOI process, which would increase the cost of the fabrication. These demerits can be overcome by permanently connecting the bulk terminals PMOS to VDD and NMOS to GND which resolves the threshold variation. This configuration provides suitability for fabricating the logic cells in CMOS p-well and n-well process. Even today some IC fabricators uses CMOS as their choice due to its easiness in achieving required transistor sizing usinf necessary voltage scaling in order to improve the reliability at low voltages. One of the drawbacks of CMOS is use of large PMOS transistors that results in high input loads at high operating frequency which in turn increases the circuit power dissipation. The propagation delay is slightly higher when compared to other logic family due to its larger node capacitances. Schematic of GDI based JK FF, corresponding timing diagram, and simulation on layout are shown in Figures 6-8.

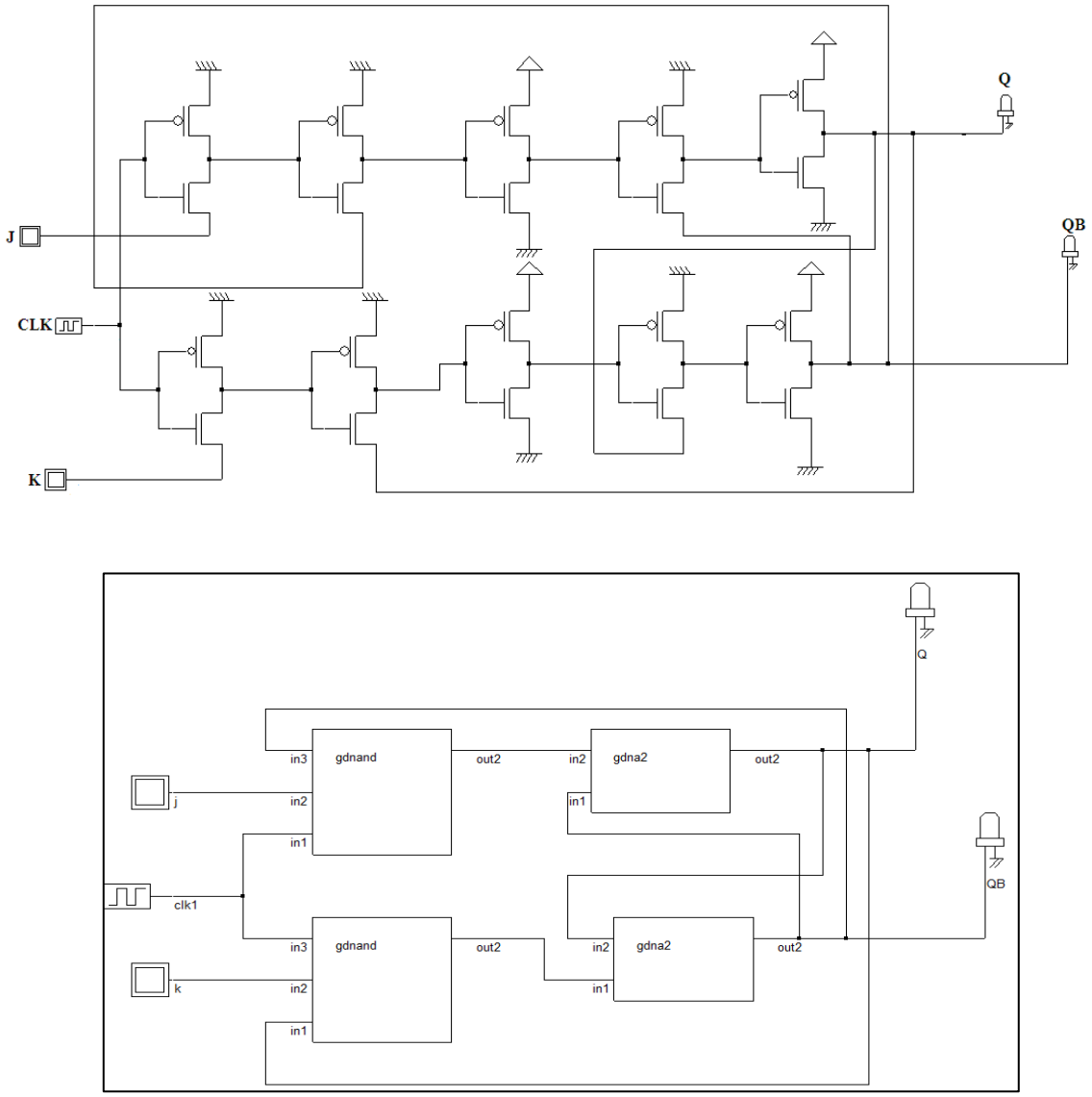

Figure 6. Schematic of GDI based JK FF

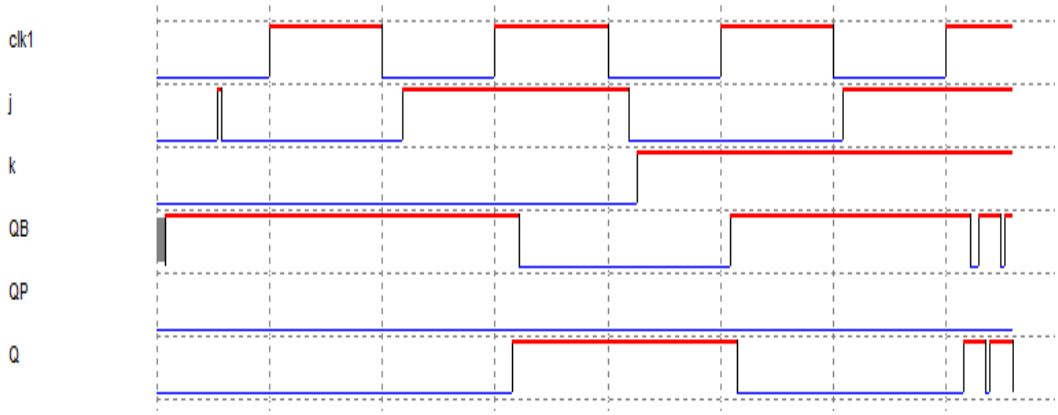

Figure 7. Transient waveform for GDI based JK

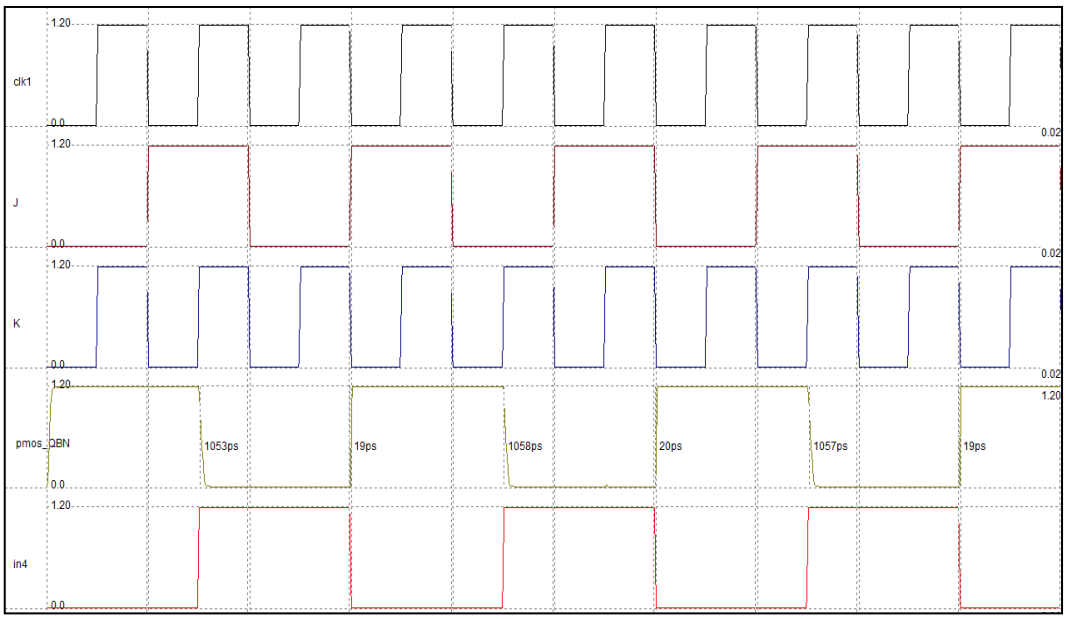

Figure 8. Simulation results for GDI based JK

2.2. JK flipflop using pass transistor logic (PTL)

In CMOS logic the transistors are connected directly to power supply hence the active devices are more that causes the continuous leakage current flow within the circuit. In contrast to this, in PTL the transistors are used as switches to pass lagoic levels between nodes of a circuit such that number of active devices are reduced. Since the logic comprises with transistors as switches PTL needs lesser number of transistors compare to the design using CMOS, which results in low power dissipation, less area, less delay and also less interconnect effects. The drawback seen in PTL is the difference of the voltage between high and low logic levels decreases at each stage. This is because the transistor in series is less saturated at its output than at its input, this effect is more pronounced when several devices are chained in series in a logic path. Hence a conventional gate may be required to restore the signal voltage to the full value. Inspite of this, PTL (Pass Transistor Logic) is most popular for low power digital circuits. Some of the main advantages of PTL over standard CMOS design are high speed, due to the small node capacitances and low power dissipation because of the reduced number of transistors. An added advantage is lower interconnection effects due to a small area.

The Pass Transistor Logic (PTL) circuit offers better characteristics than static CMOS. PTL can implement most functions with fewer transistor counts, thus reducing the overall capacitance, which results in faster switching times and low power dissipation. The general issue pertaining to this PTL logic is voltage variation due to threshold drop owing to series resistance between input and output. These demerits were surmounted using Complementary Pass-Transistor Logic (CPL) and Swing Restored Pass-Transistor Logic

(SRPL). However this logic produced larger short circuit currents, high transistor count to realize a simple gate and high wiring overhead due to the dual-rail signals. Two input and three input NAND in PTL logic are shown in Figures 9 and 10 respectively. JK FLipflop using PTL logic is shown in Figure 11.

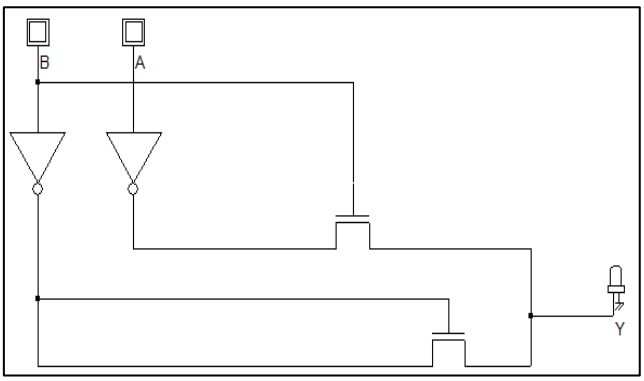

Figure 9. Critical path for PTL using two input nand gate

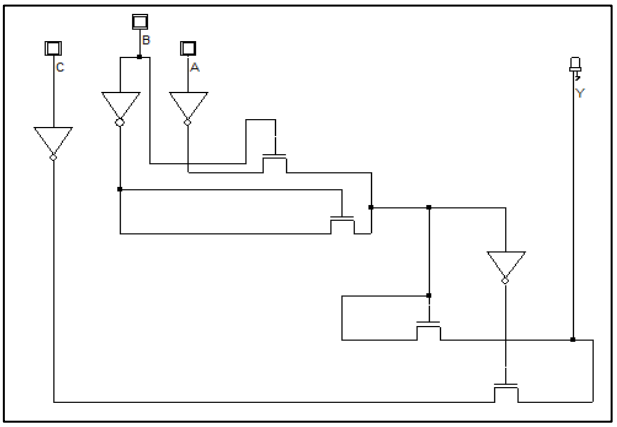

Figure 10. Schematic of PTL using three input nand gate

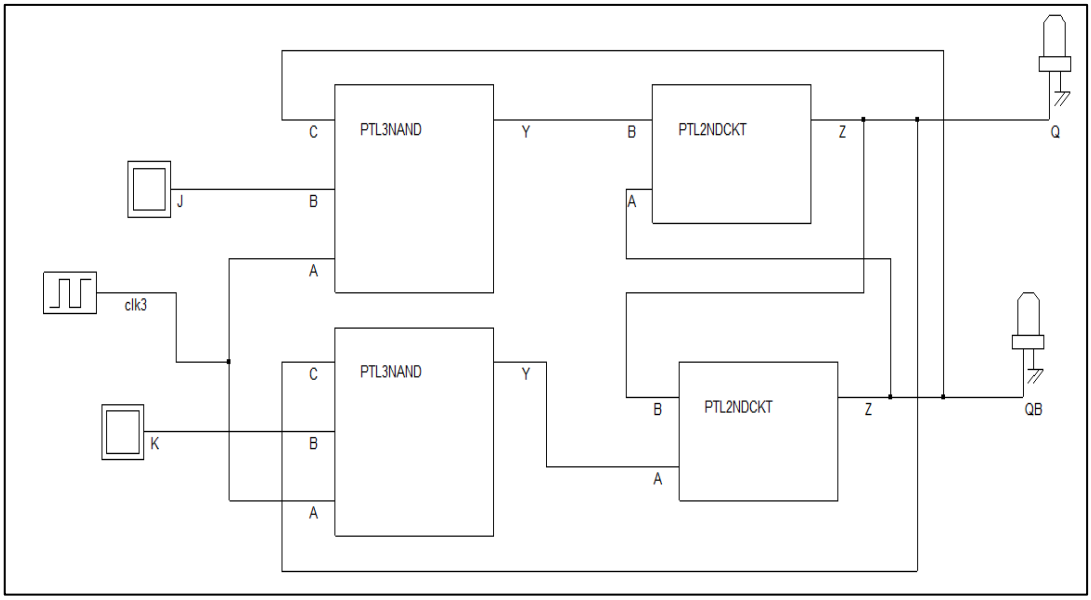

Figure 11. Schematic of JK flip-flop using PTL

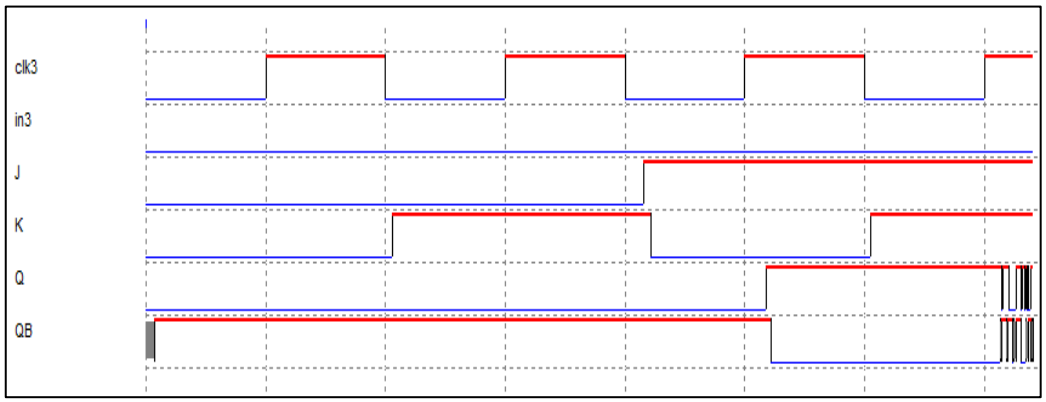

Figure 12. DSCH based simulated waveform for JK flip-flop using PTL

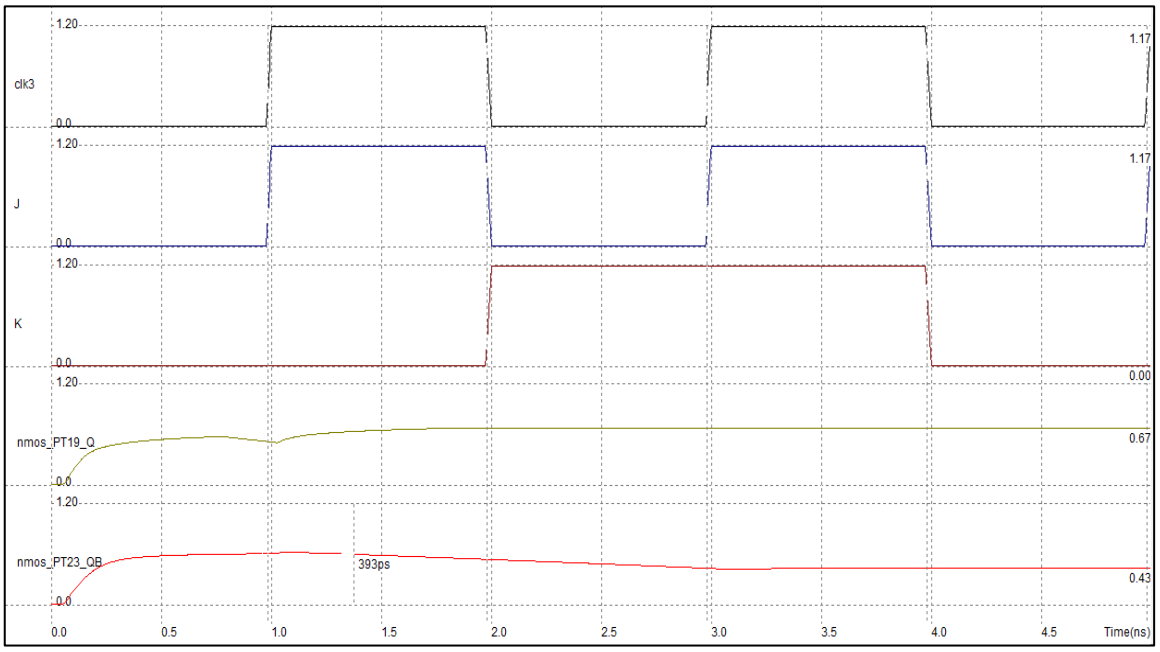

Figure 13. MICROWIND based simulated waveform for JK flip-flop using PTL

The disadvantages of PTL logic design are Output charges only up to VDD - VTH as seen in Figure 13, therefore cascade designs further degrades the performance. The threshold voltage drop across the single channel pass transistor produces low drive current that causes slow operation at reduced power supply. Hence, the high logic level at the regenerative inverter is not a full VDD, which causes pMOS device in the inverter to switch partially OFF which inturn leads to significant static power dissipation due to direct path between supply rails.

Table 2. Comparison for JK flip flop design performance

Logic used for JK FF	CPD,ns	PD,dyn,µW	PD,stat, µW	PD,tot, µW	IDmax,mA	Area,um^2
CMOS	6.08	21.128	9.778	30.906	2.660	428.4
GDI	4.570	14.53	13.006	27.536	0.061	414.5
PTL	1.385	72.602	73.279	145.881	0.957	360.1

From Table 2 one can observe that CMOS has lower Critical Path Delay compared to other two followed by PTL then GDI. This is because, the output to input delay path has inverter in the case of GDI, one MOS transistor in the case of PTL. However, in the case of CMOS design no device appears in the critical delay path, hence less delay results. CMOS exhibits medium Power dissipation, PTL exhibits more power dissipation than other two, whereas GDI results in less power dissipation. PTL has few transistors compare to CMOS and GDI hence exhibits less area occupation. Compare to PTL and CMOS less current requirement results in GDI. Hence, for less power dissipation and less current requirements one can choose GDI logic. For less area requirement, one can choose PTL.

3. EFFICIENT LOW CURRENT LFSR

A conventional LFSR shown in Figure 14 consists of D Flipflop (data or delay flipflop) where D is a single data input in addition to the clock input. It's a modified circuit of clocked RS flipflop using NOR gates. The D input goes directly to S input and its complement through NOT gate, is applied to the R input. The input value D reaches the output only when input clock changes. Initially both AND gates are disabled for clock low signal, hence D can change values but Q will not effect. When the clock is high, both AND gates are enabled then Q is forced equal to D. But when the clock again goes low, Q retains or stores the previous value of D. Corresponding truth table is shown in Table 3.

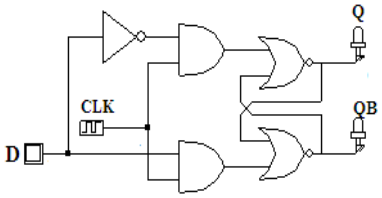

Figure 14. Circuit for D flip-flop using basic gates

Table 3. Truth Table of D Flip-flop

D	CLK	Q
0	0	0
0	1	0
1	0	0
1	1	1

There is a special type of shift register called linear feedback shift register (LFSR). The name indicates that such shift register has a feedback, which is a linear function (usually XOR) of its input and current state. LFSRs are mostly used for generation of pseudo-random sequences that find application in cryptography, circuit testing and digital communication among others. The feedback function of LFSR is usually represented with characteristic polynomial. When the polynomial is known, there are two ways to implement LFSR: as Fibonacci type LFSR or as Galois type LFSR. A 4-bit Fibonacci type LFSR is shown in Figure 15. The value of the highest degree in the polynomial indicates the size of LFSR (four bits in this particular case). To construct a Fibonacci type LFSR from a given characteristic polynomial the flip-flops in the shift register are numbered sequentially starting from a flip-flop that is closest to the input. The output of each numbered flip-flop can then be mapped to terms of the polynomial with the corresponding power (as it is shown in Figure 1). The term 1 (essentially X0) in the polynomial is mapped to the data input of the LFSR. The outputs of the flip-flops that correspond to the terms which are present in the characteristic polynomial are then XOR-ed together to form the feedback of LFSR.

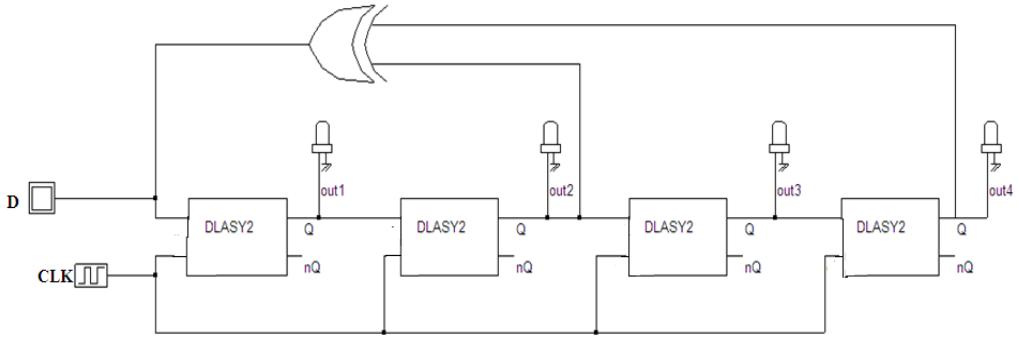

Figure 15. Circuit for 4-bit conventional LFSR

Quite often LFSRs are designed as pure generators without data input. In this case input D (X0) is omitted from the feedback equation (even though it is always present in the characteristic polynomial). For such configuration of the LFSR the feedback is completely determined by its current state. Since the total number of possible states is finite (e.g. a 4-bit LFSR has 2 4 -1=15 possible states excluding the one with all zeros) and the operation of the LFSR is deterministic, at some point LFSR will get into its initial state (the seed) and will start to repeat the same sequence of states all over again. The length of this cycle depends on the selected characteristic polynomial. For example, characteristic polynomial X4 + X3 + 1 produces a maximum sequence of all 15 states (excluding the all zeros state) before entering a repeat cycle. Corresponding simulation diagram for LFSR is shown in Figure 16. An area efficient low current LFSR is shown in Figure 17, in which D flipflops are designed using GDI logic. Corrsponding simulation results are shown in Figure 18.

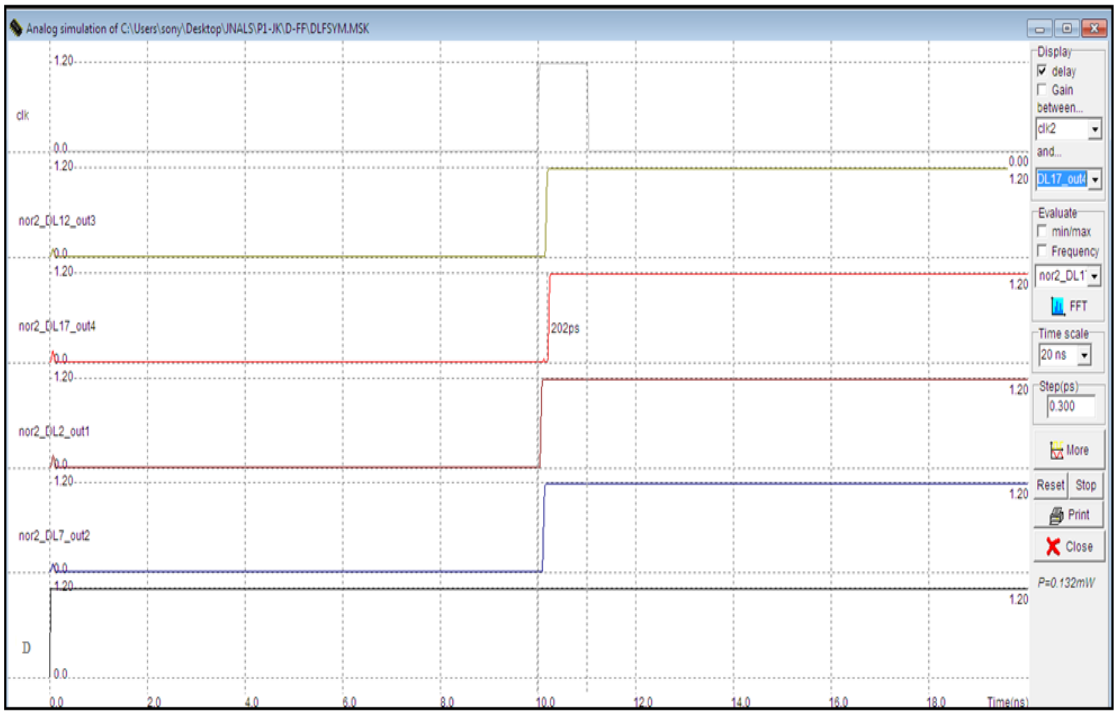

Figure 16. Simulation results for 4-bit conventional LFSR

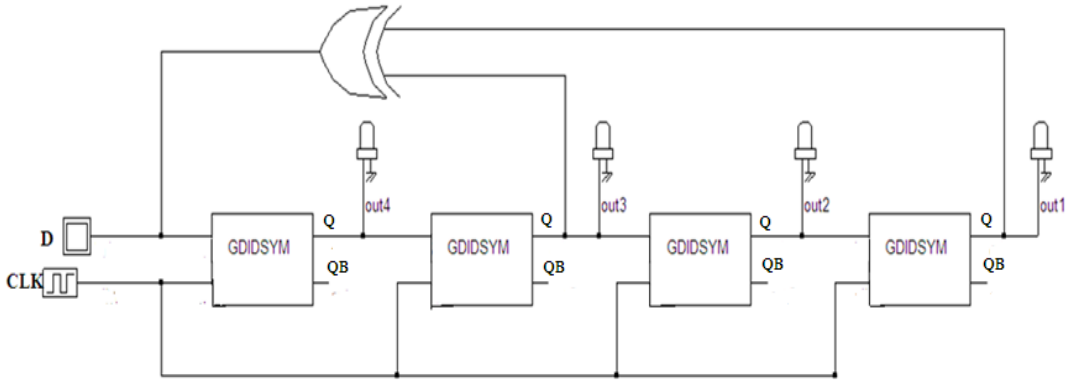

Figure17. Circuit for 4-bit area efficient low current LFSR

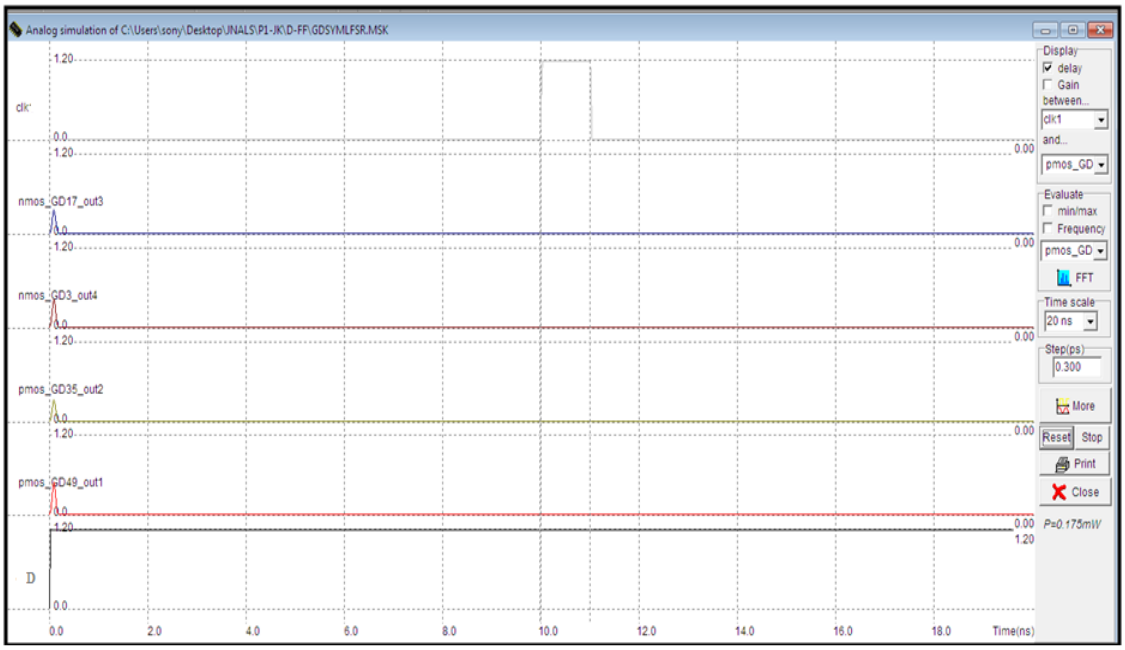

Figure 18. Simulation results for area efficient low current LFSR

Table 4. Results and Comparisons for LFSR

Logic used	CPD, ns	PD, w	IDD, mA	Area,um^2
CMOS- LFSR	5.49	0.132m	1.324	416
GDI - LFSR	11.430	0.175m	0.15	79.19
%of Improvement	51.9	24.57	88.67	80.96

4. RESULTS AND ANALYSIS

Thogh PTL is faster compare to other two logic designs from Table 3, it is inefficient for low power applications. Since the ovedrall power dissipation, current and area required observed are less in GDI logic, it is chosen for the design of proposed LFSR. Despite to the small increment in power dissipation, the resulting GDI based LFSR is observed with consistent behavior in the performance intems of low current of 88.67% and less area of 80.96% compared with traditional CMOS design.

5. CONCLUSION

Three logic designs such as CMOS, GDI and PLT are considered for the design of JK flipflop. However, PTL proven with its less delay capability but it is out of the selction due to large variations in other parameters. On the otherhand, traditional CMOS logic design resulted with more power dissipation and current compared with GDI, hence GDI logic is chosen for the design of LFSR. Due to profound improvement of 80.96% in area reduction and 88.67% in current reduction, the design of BIST using proposed LFSR deffinetly an advantageous for low power applications

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