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Simulation and Real Time Implementation of Various PWM Strategies for 3 Φ Multilevel Inverter Using FPGA

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ABSTRACT

For high power applications Multilevel Inverter (MLI) is extensively used. The major advantages of MLI are good power quality, low switching losses and maintenance of the desired voltage. In this work, the three phase cascaded multi level inverter is analyzed under various modulation techniques that include Sub-Harmonic Pulse Width Modulation (SHPWM) i.e. Phase Disposition (PD) strategy, Phase Opposition Disposition (POD) strategy, Alternate Phase Opposition Disposition (APOD) strategy, hybrid strategy (PD and PS) and Phase Shift (PS) strategy. The study will help to choose those techniques with reduced harmonics for the chosen three phase cascaded MLI with R-L load. The Total Harmonic Distortion (THD), VRMS (fundamental), crest factor and form factor are evaluated for various modulation indices at two different switching frequencies (3.15KHz and 6 KHz). Simulation is performed using MATLAB-SIMULINK. It is observed that HYBRID PWM and PSPWM methods provide output with relatively low distortion for low and high switching frequencies. PODPWM and PSPWM are found to perform better since they provide relatively higher fundamental RMS output voltage for 6 KHz and 3.15 KHz switching frequencies. The experimental result shows PSPWM provide output with low distortion and HYBRID PWM provide output with higher fundamental RMS voltage for fc=3.15KHz. The experimental results were obtained only for fc=3.15KHz.

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1. INTRODUCTION

Multilevel inverters offer a number of advantages when compared to its conventional two-level inverter counterpart. The stepped approximation of the sinusoidal output using higher levels reduces the harmonic distortion of the output and the stresses across the semiconductor devices and also allows higher voltage/current and power ratings. Rajesh Gupta et al [1] proposed switching characterization of cascaded multilevel inverter controlled systems. Palanivel and Dash [2] evaluated THD and output voltage of three phase cascaded MLI using multicarrier PWM techniques. Rajesh Gupta et al [3] developed multiband hysteresis modulation and switching characterization for sliding-mode-controlled cascaded MLI. Ghoreishy et al [4] proposed methods for reducing common-mode voltage and power dissipation in cascaded multilevel inverters with flexible DC sources. Malinowski et al [5] carried out a detailed survey on cascaded multilevel inverters. Zhong et al [6] discussed fundamental frequency switching strategies of a seven level hybrid cascaded H-bridge multilevel inverter. Teodorescu et al [7] developed a multilevel inverter using cascaded industrial voltage source inverter. Corzine et al [8] proposed control for cascaded multilevel inverter. Deepa

et al [9] undertook harmonic analysis of a modified cascaded multilevel inverter. Zambra et al [10] Compared neutral point clamped, symmetrical and hybrid asymmetrical multilevel inverters. Youheihinago and Hirotaka Koizumi [11] proposed a single phase multilevel inverter using switched series/parallel DC voltage sources. Risnidar et al [12] discusses the influence of harmonics in laboratory due to Nonlinear Loads. Mohammad Jamil in [13] made a comparison on multilevel inverters with reduction of common mode voltage. Manjunatha and Anand [14] suggested a multilevel DC link inverter with reduced switches and batteries. Balamurugan et al [15] introduced a new bipolar hybrid carrier PWM strategies for symmetrical multi level inverter. Balamurugan et al [16] made a comparison between simulation and dSPACE based implementation of various PWM strategies for a new H-type FCMLI topology. This literature survey reveals few papers only on various PWM techniques and hence this work presents a novel approach for controlling the harmonics of output voltage of chosen MLI employing sinusoidal PWM switching strategies with triangular carriers. Simulations are performed using MATLAB-SIMULINK. Harmonics analysis and evaluation of performance measures for various modulation indices have been carried out and presented.

2. MULTILEVEL INVERTER

The multilevel inverters have drawn tremendous interest in the power industry. Multilevel inverters are also well suited for use in reactive power compensation. Power electronics technologies have also provided an important improvement of renewable energy applications. Many renewable energy applications will require high power inverters (>50 kW); for instance, a grid connected inverter. Therefore, multilevel inverters are suitable for this application because a multilevel inverter can possibly provide the high volt ampere ratings; multilevel inverters will significantly reduce the magnitude of harmonics and increases the output voltage and power without the use of step-up transformer. A cascaded multilevel inverter consists of a series of H- bridge inverter units connected to three phase R-L load. The general function of this multilevel inverter is to synthesize a desired voltage from several DC sources. The AC terminal voltages of each bridge are connected in series. Unlike the diode clamped or flying-capacitors inverter, the cascaded inverter does not require any voltage clamping diodes. This configuration is useful for constant frequency applications such as active front- end rectifiers, active power filters, and reactive power compensation. In this case, one of the very efficiently used control strategies is the space vector based control, which can be implemented using digital signal processor. Fig.1 shows the three phase cascaded multilevel inverter with induction motor load. The general function of this multilevel inverter is to produce a preferred voltage from several separate DC sources, which may be obtained from batteries, fuel cells or solar cells. Each DC source is connected to an H-bridge inverter. The operation of cascaded multilevel inverter is based on the separate DC sources. Each inverter level can generate three different voltage outputs, $+V_{dc}$, 0 and $-V_{dc}$ using various combinations of four switches. The number of output phase voltage levels m in a cascaded inverter is defined by m=2s+1, where s is the number of separate DC sources. Using the example, turning on T_{a1} and T_{a4} yields $+V_{dc}$ output voltage, turning on T_{a2} and T_{a3} yields $-V_{dc}$ output voltage, turning off all switches yields no output. Fig. 1 show the power circuit of three phase cascaded multilevel inverter. The AC output voltage at other bridges can be obtained in the same manner. Controlling the conducting periods of switches of different inverter bridges can minimize the harmonic distortion of the output voltage. Several forms of renewable zero pollution energy resources including wind, solar, bio, geothermal can be used by cascaded multilevel inverter.

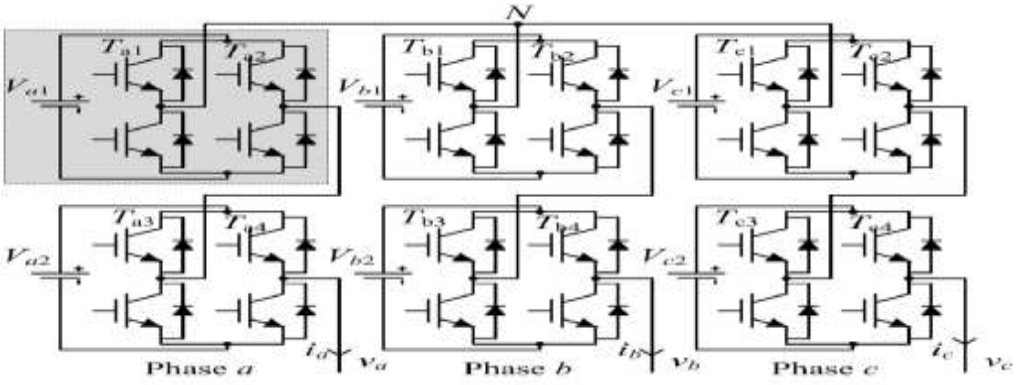

Figure 1. A three phase cascaded multilevel inverter

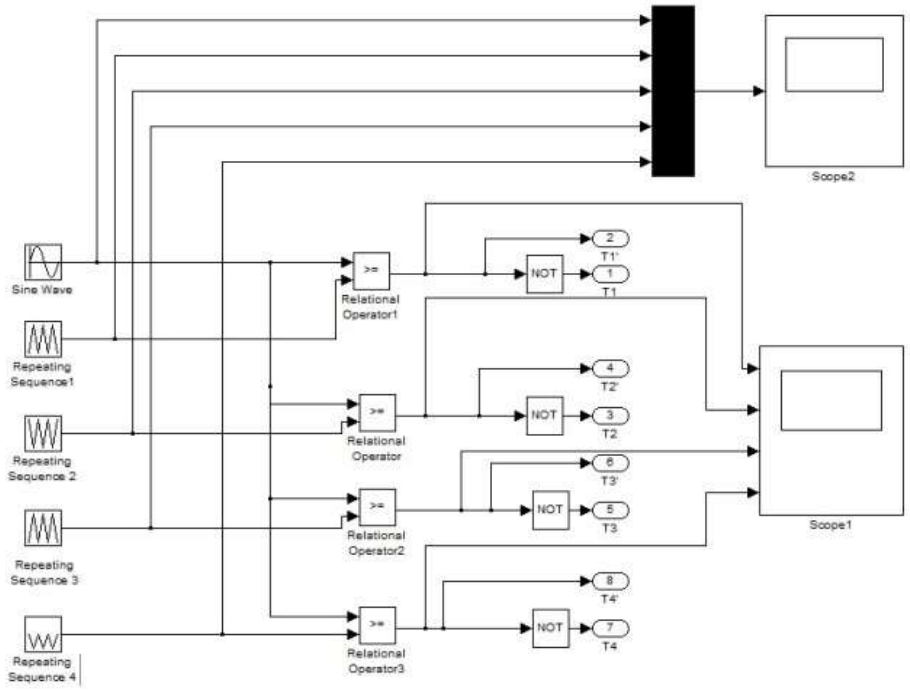

Figure 2. Sample PWM generation logic using SIMULINK developed for APOD TECHNIQUE

3. MULTICARRIER PWM METHODS

This work used the intersection of a sine wave reference signal with triangular carrier waves to generate firing pulses. There are five alternative strategies to implement this objective and Figure 2 shows a sample PWM generation logic.

3.1. Phase Disposition PWM Strategy

The rules for phase disposition method Figures (3 and 4) for a multilevel inverter are

a. 4 carrier waveforms in phase are arranged.
b. The converter is switched to + 2Vdc when the sine wave is greater than both upper carrier waveform.
c. The converter is switched to + Vdc when the sine wave is greater than first upper carrier waveform.
d. The converter is switched to zero when sine wave is lower than upper carrier but higher than the lower carrier.
e. The converter is switched to - Vdc when the sine wave is less than first lower carrier waveform.
f. The converter is switched to - 2Vdc when the sine wave is less than both lower carrier waveforms.

The following formula is applicable to sub harmonic PWM strategy i.e PD, POD and APOD PWMs.

The frequency modulation index is $m_f=f_c/f_m$
The amplitude modulation index is $m_a=2A_m/(m-1)A_c$
where

f_c - Frequency of the carrier signal
f_m - Frequency of the reference signal
A_m - Amplitude of the reference signal
A_c - Amplitude of the carrier signal
m - Number of levels.

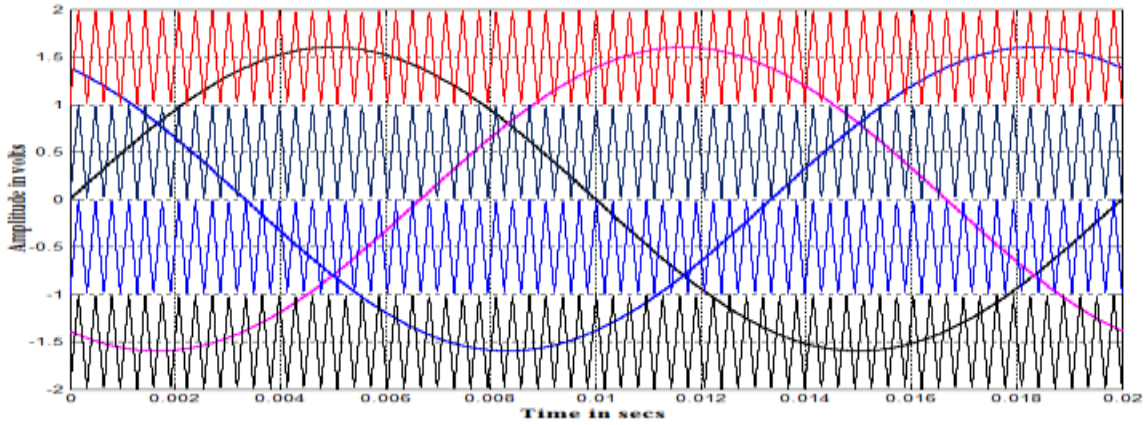

Figure 3. Carrier Arrangement for PDPWM Strategy (m_a=0.8 and m_f =63)

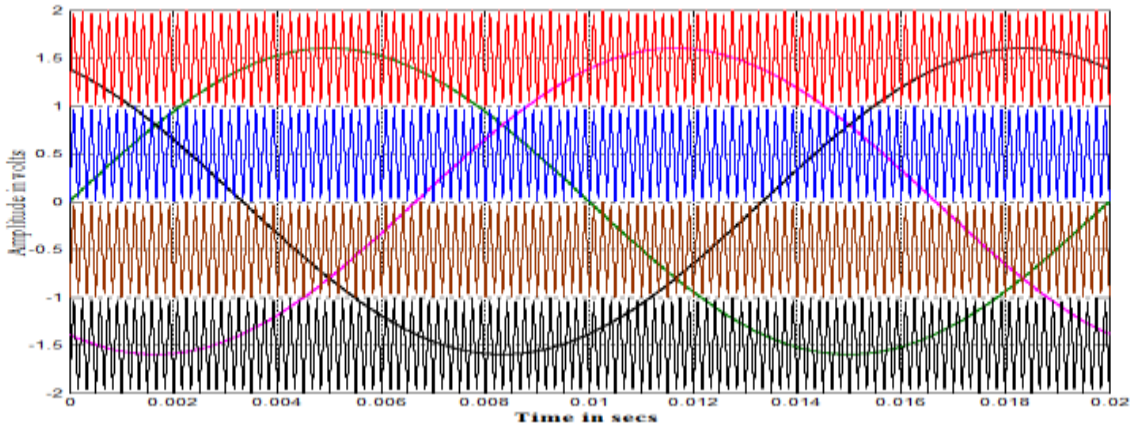

Figure 4. Carrier arrangement for PDPWM strategy (m_a=0.8 and m_f=120)

3.2. Phase Opposition and Disposition PWM Strategy

Four carrier waveforms are arranged so that all carrier waveforms above zero are in phase and they are 180 degrees out of phase with those below zero see Figures 5 and 6.

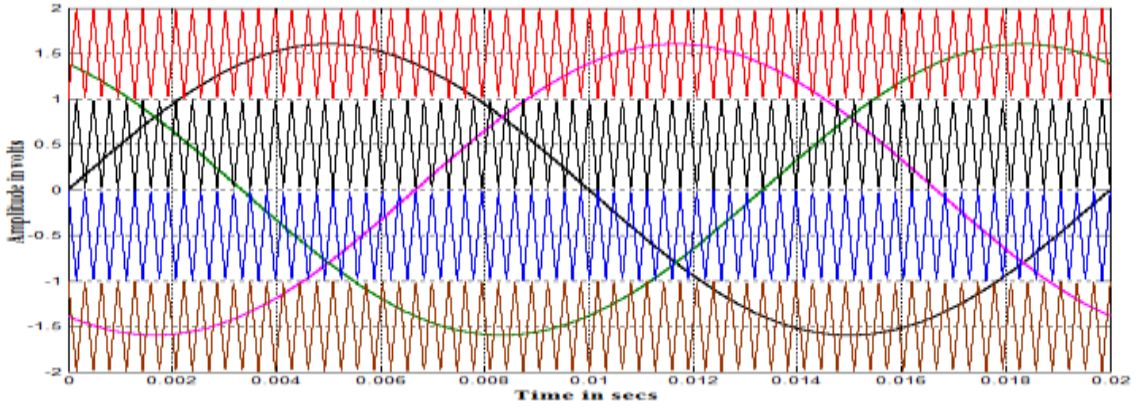

Figure 5. Carrier arrangement for PODPWM strategy (m_a=0.8 m_f=63)

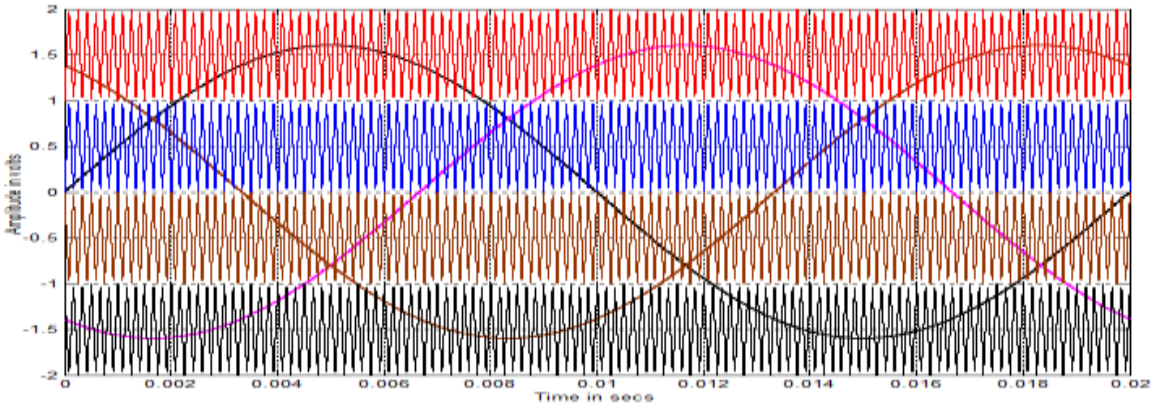

Figure 6. Carrier arrangement for PODPWM strategy (m_a=0.8 and m_f=120)

3.3. Alternative Phase Opposition and Disposition PWM strategy

Carriers are arranged in such a manner that each carrier is out of phase with its neighbor by 180 degrees see Figure 7 and 8.

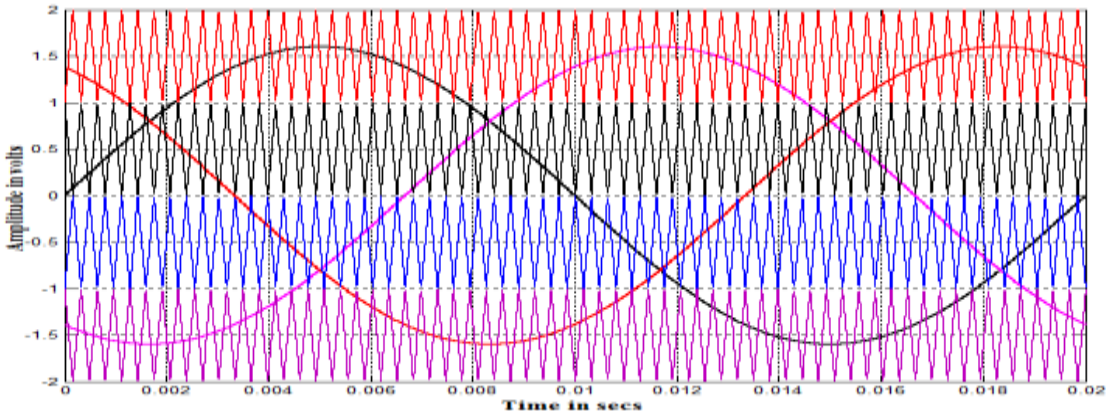

Figure 7. Carrier arrangement for APODPWM strategy (m_a=0.8 and m_f=63)

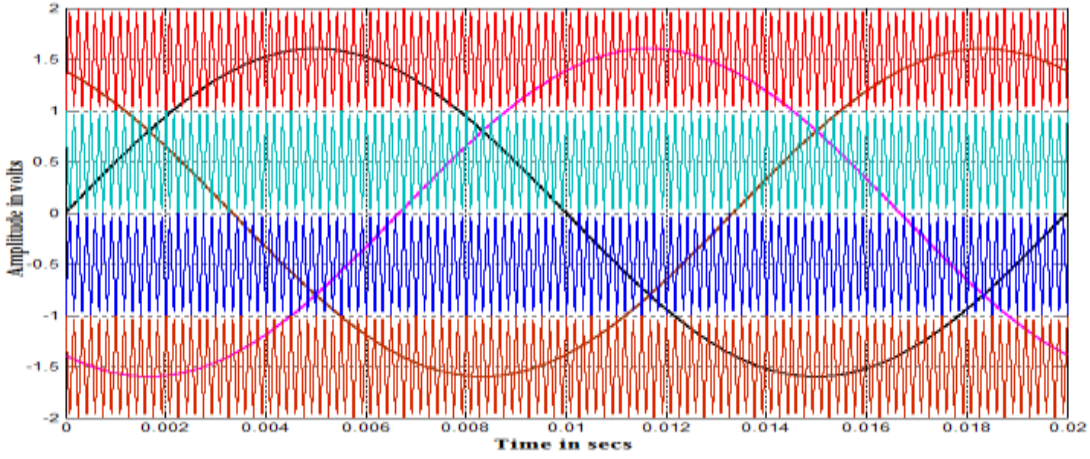

Figure 8. Carrier arrangement for APODPWM strategy (m_a=0.8 and m_f=120)

3.4. Phase Shift PWM Strategy

The phase shift multicarrier PWM technique uses four carrier signals of the same amplitude and frequency which are shifted by 90 degrees to one another to generate the five level inverter output voltages see Figure 9 and 10. The gate signals for the cascaded inverter can be derived directly from the PWM signals (comparison of the carrier with the sinusoidal reference). There is a certain degree of freedom in the allocation of the carriers to the inverter switches.

The amplitude modulation index

$m_a = A_m / (A_c/2)$

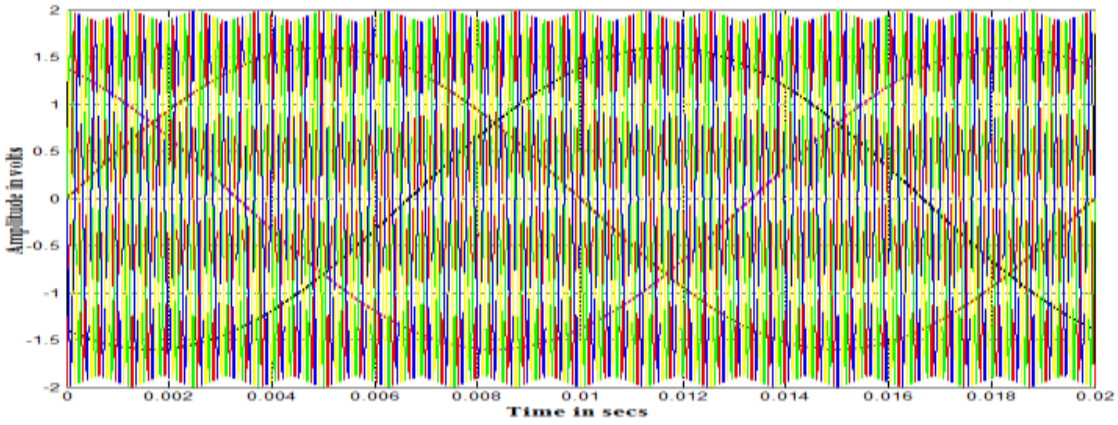

Figure 9. Carrier arrangement for PSPWM strategy (m_a=0.8 and m_f=63)

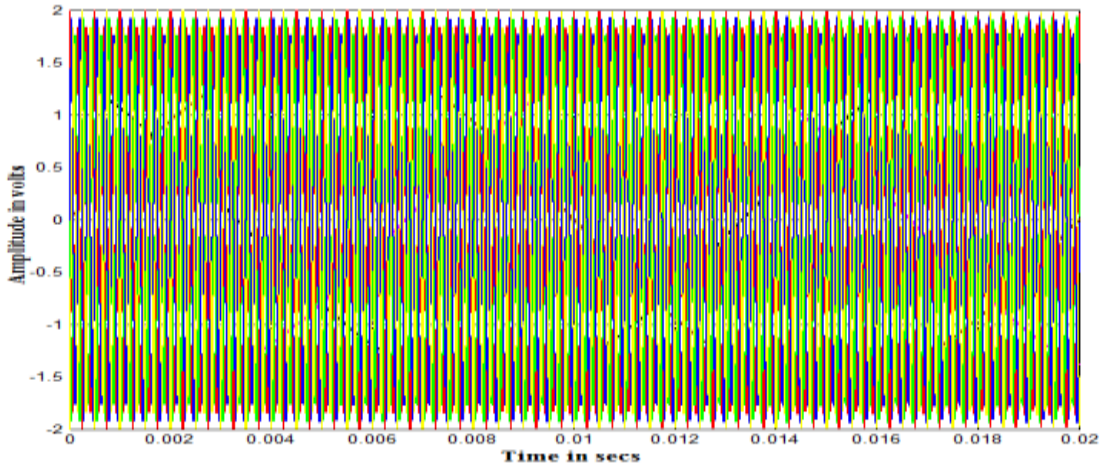

Figure 10. Carrier arrangement for PSPWM strategy (m_a=0.8 and m_f=120)

3.5. Hybrid PWM Strategy

The hybrid PWM strategy is the combination of phase disposition and phase shift strategy. Hybrid PWM strategy is illustrated see Figure 11 and 12.

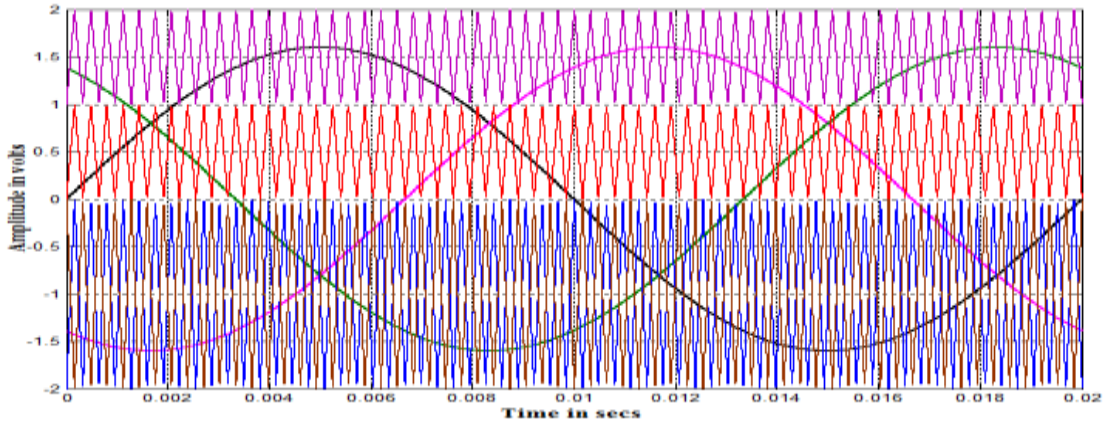

Figure 11. Carrier arrangement for HYBRID PWM strategy (m_a=0.8 and m_f=63)

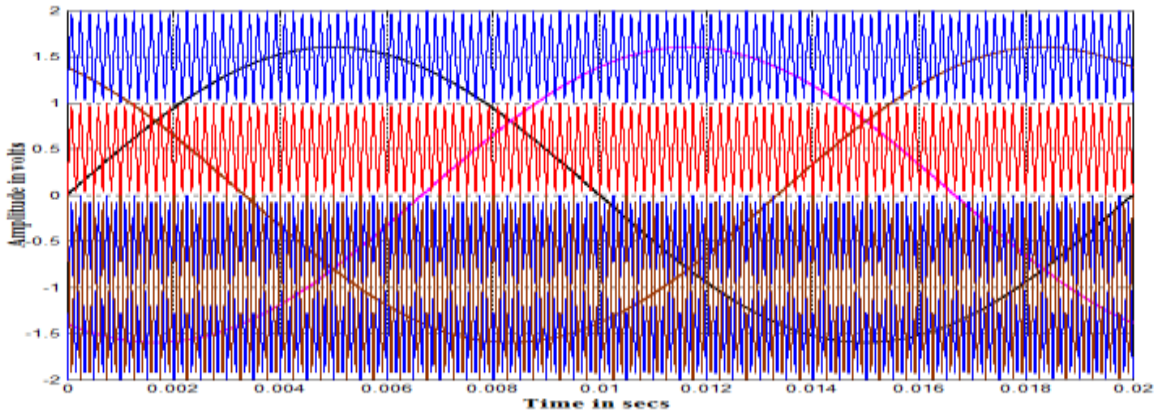

Figure 12. Carrier arrangement for HYBRID PWM strategy (m_a=0.8 and m_f=120)

4. SIMULATION RESULTS

To verify the proposed schemes, a simulation model for a three phase five level cascaded H-bridge inverter is implemented using MATLAB as in Figure 2. Simulations are performed for different values of m_a ranging from 0.5 to 0.9 and the corresponding %THD is measured using the FFT block and their values are shown in Table 1. Figures 13 – 32 show the simulated output voltages of CMLI and their harmonic spectrum with different PWM strategies but for only one sample value of m_a=0.8 for R-L load. Figure 13 shows the five level output voltage generated by PDPWM strategy (m_f=63 with f_c=3.15KHz and f_m=50Hz) and its FFT plot is shown in Figure 14. From Figure 14 it is observed that the PDPWM strategy produces significant 53rd, 55th, 59th and 61st harmonic energy. Figure 15 shows the five level output voltage generated by PDPWM strategy (m_f=120 with f_c=6KHz and f_m=50Hz) and its FFT plot is shown in Figure 16. From Figure 16 it is observed that the PDPWM strategy produces significant 110th, 112th, 116th and 118th harmonic energy. Figure 17 shows the five level output voltage generated by PODPWM strategy (f_c=3.15KHz) and its FFT plot is shown in Figure 18. From Figure 18 it is observed that the PODPWM strategy produces significant 56th, 58th and 62nd harmonic energy. Figure 19 shows the five level output voltage generated by PODPWM strategy (f_c=6KHz) and its FFT plot is shown in Figure 20. From Figure 20 it is observed that the PODPWM strategy produces significant 114th, 116th and 120th harmonic energy. Figure 21 shows the five level output voltage generated by APODPWM strategy (f_c=3.15KHz) and its FFT plot is shown in Figure 22. From Figure 22 it is observed that the APODPWM strategy produces significant 58th, 60th and 62nd harmonic energy. Figure 23 shows the five level output voltage generated by APODPWM strategy (f_c=6KHz) and its FFT plot is shown in Figure 24. From Figure 24 it is observed that the APODPWM strategy produces significant 116th, 118th and 120th harmonic energy. Figure 25 shows the five level output voltage generated by HYBRIDPWM strategy (f_c=3.15KHz) and its FFT plot is shown in Figure 26. From Figure 26 it is observed that the HYBRIDPWM strategy produces significant 53rd, 55th, 56th, 58th and 62nd harmonic energy. Figure 27 shows the five level output voltage generated by HYBRIDPWM strategy (f_c=6KHz) and its FFT plot is shown in

Figure 28. From Figure 28 it is observed that the HYBRIDPWM strategy produces significant 113th, 114th, 116th and 120th harmonic energy. Figure 29 shows the five level output voltage generated by PSPWM strategy (f_c=3.15KHz) and its FFT plot is shown in Figure 30. From Figure 30 it is observed that the PSPWM strategy does not produce significant harmonic energy. Figure 31 shows the five level output voltage generated by PSPWM strategy (f_c=6KHz) and its FFT plot is shown in Figure 32. From Figure 32 it is observed that the PSPWM strategy does not produce significant harmonic energy. The following parameters were chosen for the simulation V_{dc}=20V, f_c=3.15KHz and 6KHz, R=100 ohms and L= 0.5 mH.

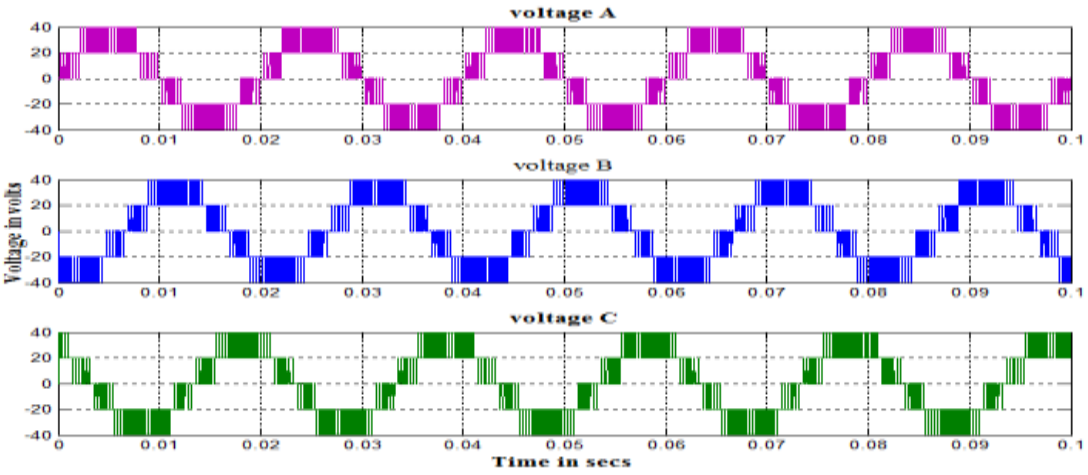

Figure 13. Output voltage generated by PDPWM strategy for R-L load. (m_a=0.8 and m_f=63)

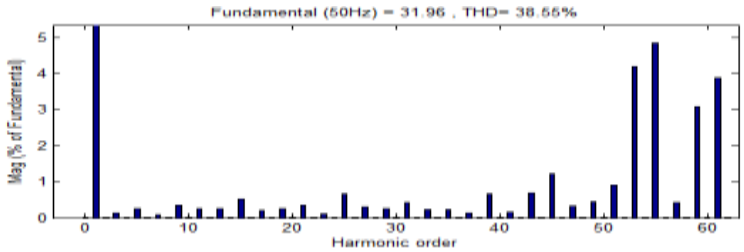

Figure 14. FFT plot for output voltage of PDPWM strategy for R-L load (m_f=63)

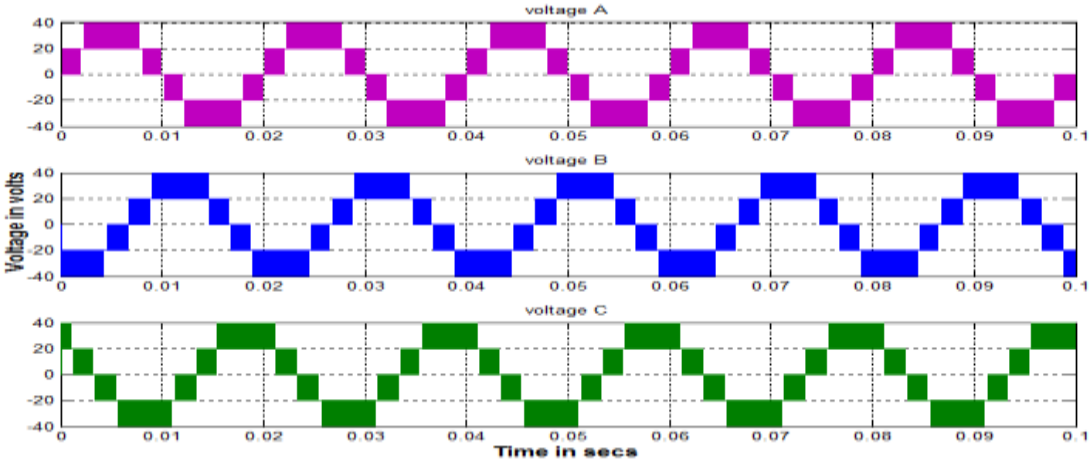

Figure 15 Output voltage generated by PDPWM strategy for R-L load (m_a=0.8 and m_f=120)

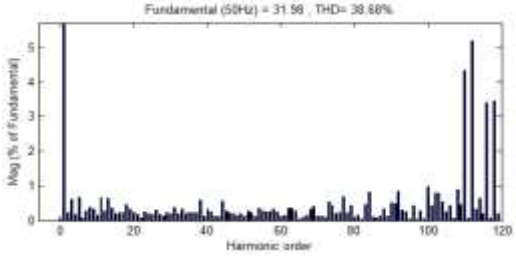

Figure 16. Output voltage generated by PDPWM strategy for R-L load (m_f=120)

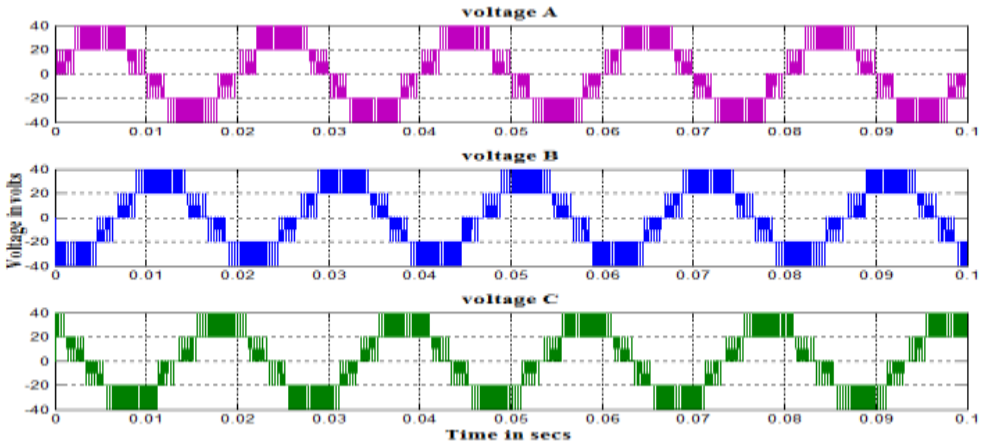

Figure 17 Output voltage generated by PODPWM Strategy for R-L load (m_a=0.8 and m_f=63)

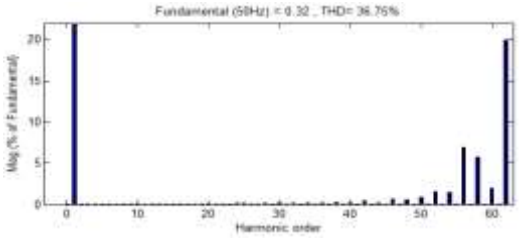

Figure 18. FFT Plot for output voltage of PODPWM strategy for R-L Load (m_f=63)

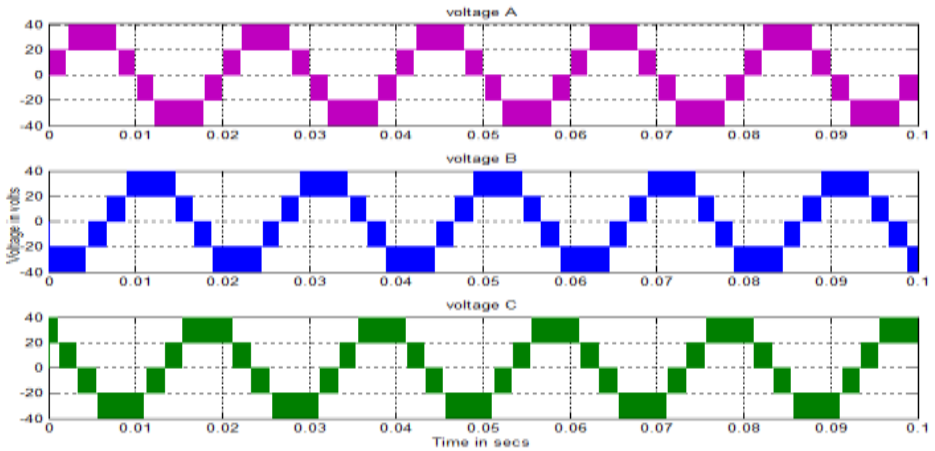

Figure 19. Output voltage generated by PODPWM Strategy for R-L Load (m_a=0.8 and m_f=120)

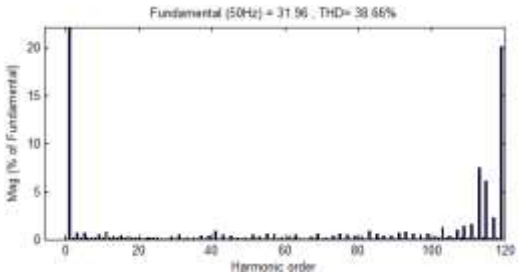

Figure 20. FFT plot for output voltage of PODPWM strategy for R-L load (m_f=120)

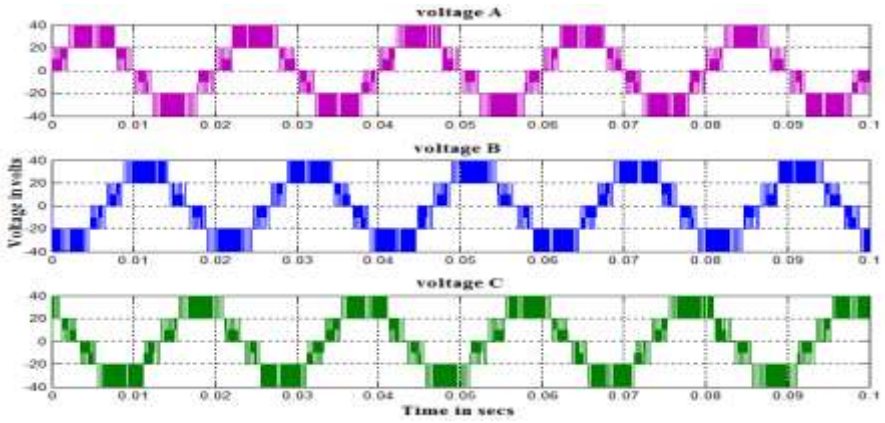

Figure 21. Output voltage generated by APODPWM strategy for R-L load (m_a=0.8 and m_f=63)

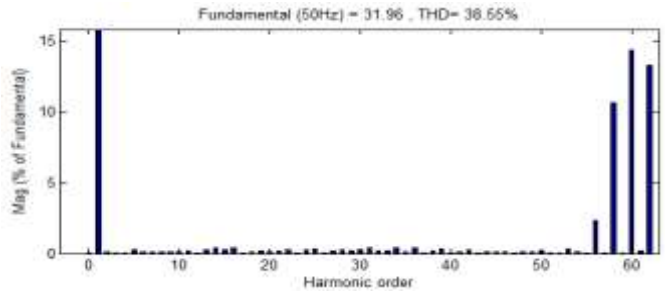

Figure 22. FFT plot for output voltage of APODPWM strategy for R-L load (m_f=63)

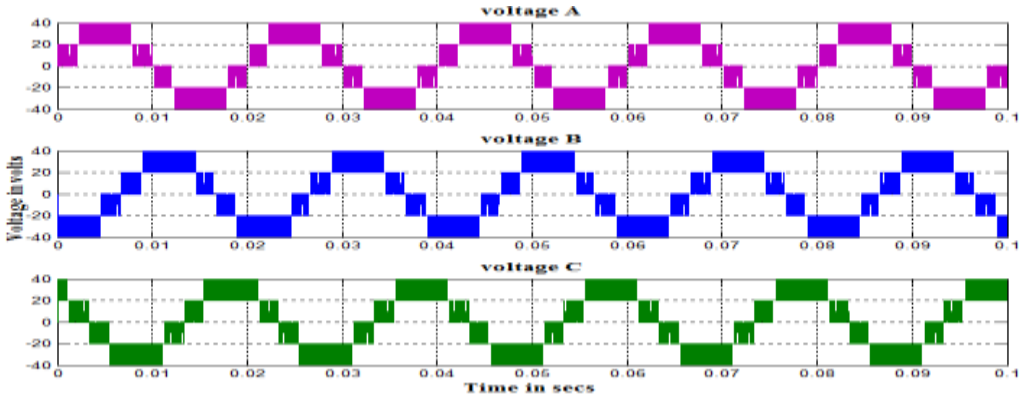

Figure 23. Output voltage generated by APODPWM strategy for R-L load (m_a=0.8 and m_f=120)

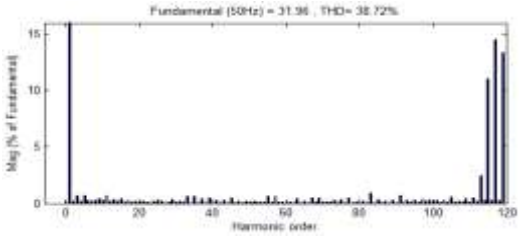

Figure 24. FFT plot for output voltage of APODPWM strategy for R-L load (m_f=120)

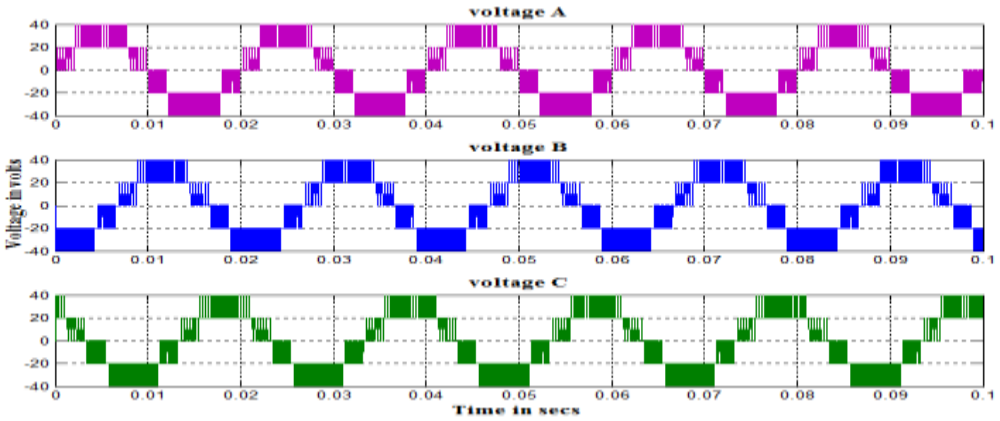

Figure 25. Output voltage generated by HYBRIDPWM strategy for R-L load (m_a=0.8 and m_f=63)

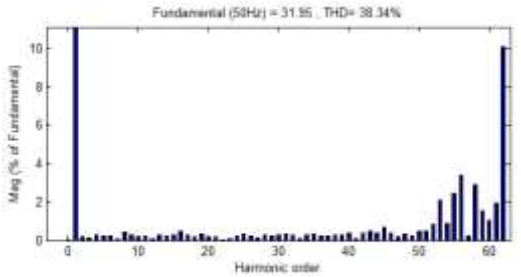

Figure 26. FFT plot for output voltage of HYBRIDPWM strategy for R-L load (m_f=63)

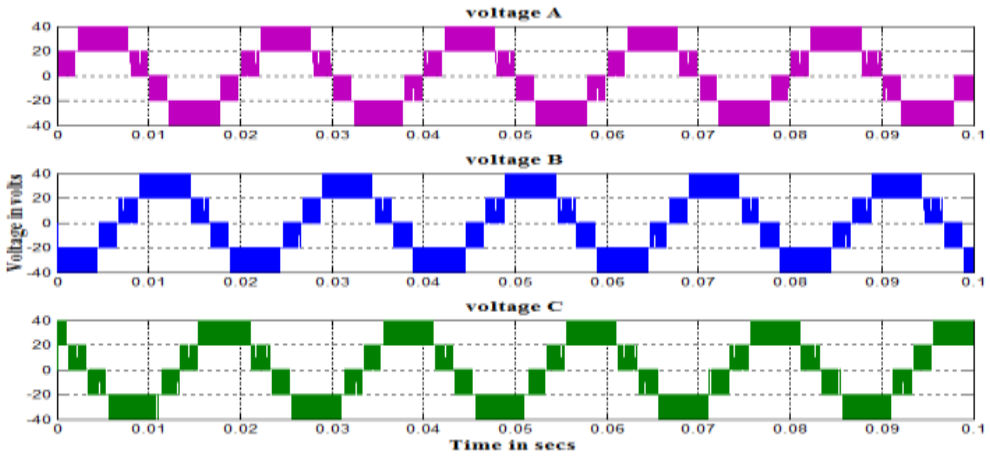

Figure 27. Output voltage generated by HYBRID PWM strategy for R-L load (m_a=0.8 and m_f=120)

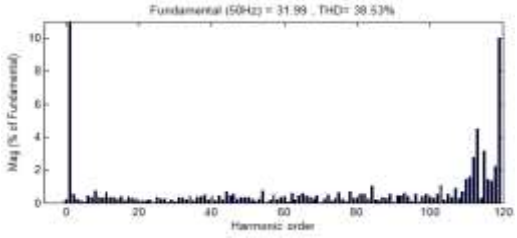

Figure 28. FFTPlot for output voltage of HYBRID PWM Strategy for R-L load (m_f=120)

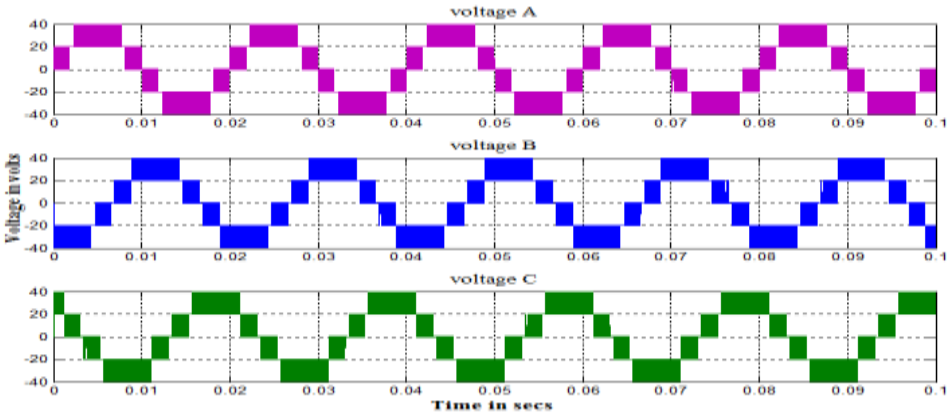

Figure 29. Output voltage generated by PSPWM strategy for R-L load (m_a=0.8 and m_f=63)

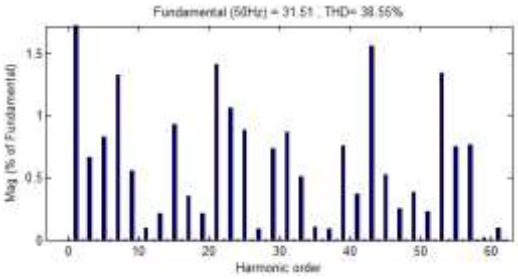

Figure 30. FFT plot for output voltage of PSPWM strategy for R-L load (m_f=63)

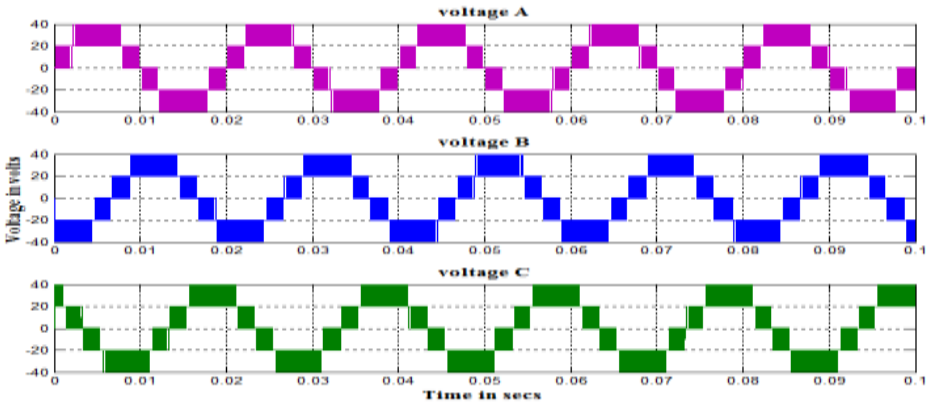

Figure 31. Output voltage generated by PSPWM strategy for R-L load (m_a=0.8 and m_f=120)

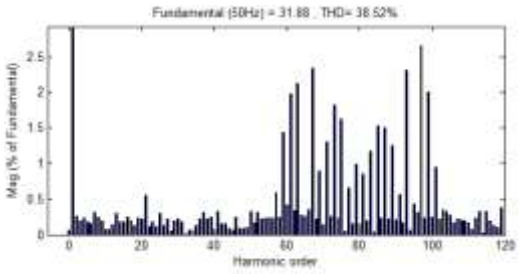

Figure 32. FFT plot for output voltage of PSPWM strategy for R-L load (m_f=120)

Table 1. % THD Comparison for Different Modulation Indices with R-L Load (by Simulation)

m_a	PD		POD		APOD		PS		HYBRID	
	3.15KHz	6KHz	3.15KHz	6KHz	3.15KHz	6KHz	3.15KHz	6KHz	3.15KHz	6KHz
1	26.93	26.93	28.3	27.13	26.93	28.34	26.10	27.13	26.72	26.97
0.9	33.41	33.51	33.38	33.58	33.38	33.68	33.24	33.43	33.37	33.52
0.8	38.55	38.68	38.56	38.66	38.55	38.72	38.55	38.52	38.34	38.53
0.7	41.73	41.61	41.73	41.51	41.73	41.93	43.18	41.86	41.78	41.55
0.6	44.43	44.41	44.43	44.24	44.43	44.55	44.37	44.06	44.19	44.17
0.5	51.76	52.70	51.17	53.39	51.77	51.56	55.12	52.02	51.48	52.79

Table 2. V_{RMS} (Fundamental) for Different Modulation Indices for R-L Load (by Simulation)

m_a	PD		POD		APOD		PS		HYBRID	
	3.15KHz	6KHz	3.15KHz	6KHz	3.15KHz	6KHz	3.15KHz	6KHz	3.15KHz	6KHz
1	28.3	28.33	28.3	28.29	28.3	28.34	28.5	28.21	28.34	28.26
0.9	25.41	25.52	25.42	25.48	25.41	25.49	25.45	25.54	25.42	25.47
0.8	22.6	22.61	22.6	22.6	22.6	22.6	22.28	22.54	22.59	22.62
0.7	19.87	19.81	19.87	19.92	19.87	19.86	20	19.85	19.86	19.85
0.6	17.03	16.96	17.03	17	17.03	16.95	17.13	16.94	16.93	16.95
0.5	14.19	14.09	14.19	14.03	14.19	14.19	13.84	14.15	14.24	14.08

Table 3. Crest Factor for Different Modulation Indices with R-L Load (by Simulation)

m_a	PD		POD		APOD		PS		HYBRID	
	3.15KHz	6KHz	3.15KHz	6KHz	3.15KHz	6KHz	3.15KHz	6KHz	3.15KHz	6KHz
1	1.4144	1.4144	1.4144	1.4142	1.4144	1.4142	1.4143	1.4706	1.4142	1.4143
0.9	1.4140	1.4141	1.4145	1.4139	1.4142	1.4141	1.4144	1.4139	1.4145	1.4144
0.8	1.4141	1.4144	1.4138	1.4136	1.4141	1.4140	1.4140	1.4145	1.4140	1.4112
0.7	1.4139	1.4140	1.4142	1.4140	1.4141	1.4140	1.4141	1.4144	1.4145	1.4143
0.6	1.4139	1.4139	1.4142	1.4144	1.4139	1.4144	1.4142	1.4155	1.4142	1.4139
0.5	1.4136	1.4141	1.4144	1.4141	1.4136	1.4145	1.4144	1.4142	1.4144	1.4141

m_a	PD		POD		APOD		PS		HYBRID	
	3.15KHz	6KHz	3.15KHz	6KHz	3.15KHz	6KHz	3.15KHz	6KHz	3.15KHz	6KHz
1	INF	236.0	INF	INF	INF	1417	INF	122.6	566.8	282.6
0.9	847	318.8	INF	849.3	INF	424.8	INF	182.4	INF	181.9
0.8	INF	753.6	INF	251.11	INF	376.6	INF	375.6	53	119
0.7	INF	61.90	INF	498	INF	INF	INF	180.45	110.33	79.4
0.6	INF	130.46	INF	425	INF	423.7	428.25	211.7	51.30	99.70
0.5	INF	46.96	INF	140.3	INF	INF	INF	283	40.68	46.93

Table 4. Form Factor for Different Modulation Indices with R-L Load (by Simulation)

Table 5. Distortion Factor for Different Modulation Indices with R-L Load (by Simulation)

m_a	PD		POD		APOD		PS		HYBRID	
	3.15KHz	6KHz	3.15KHz	6KHz	3.15KHz	6KHz	3.15KHz	6KHz	3.15KHz	6KHz
1	0.0515	0.0729	0.0678	0.0179	0.0691	0.0233	0.0324	0.0435	0.0120	0.176
0.9	0.0688	0.0731	0.0136	0.0154	0.0143	0.0149	2.404	0.0187	0.0193	0.0324
0.8	0.0804	0.0644	0.0157	0.134	0.0164	0.0151	0.0796	0.0799	0.0169	0.0157
0.7	0.0803	0.0789	0.0164	0.265	0.0172	0.0188	0.0917	0.0923	0.0164	0.0175
0.6	0.0958	0.0653	0.0165	0.0162	0.0167	0.0145	0.0714	0.734	0.0674	0.0165
0.5	0.0121	0.0234	0.0197	0.0153	0.0196	0.0123	0.0622	0.543	0.423	0.0194

5. EXPERIMENTAL RESULTS

This section presents the results of experimental work carried out on chosen CMLI using SPARTAN 3E development board (Model No: VPTB-05) SPARTAN–3EXC3S100E FPGA. This kit provides a low cost, easy to use development and evaluation platform for Spartan – 3E FPGA designs. Real time implementation of these strategies using FPGA requires less time for development. The Spartan-3E includes the following components and features, 100000 gates, 2160 logic cell equipment, Four 18 K–bit block RAMs (72 K bits), Four 18×18 pipelined hardware multipliers, two digital clock managers (DCMs), 32 Mbit Intel strata flash, 3 numbers of 20 pin header to interface VLSI based experimental modules, 8 input dip switches, 8 output LEDs, on board programmable oscillator (3 to 200 MHz), 16×2 alphanumeric LCD, RS232 UART, 4 channel 8 bit 12c based ADC and single channel DAC, PS/2 keyboard/mouse, prototype area for user applications, on board configuration flash PROM XCFOIS. The gate signal generation using different PWM strategies listed above is designed and developed using VLSI software. The result of the experimental study are shown in the form of the output voltage and FFT spectrum of chosen CMLI. Optocoupler circuit provides isolator between the control circuit and the power converter circuit. The optocoupler used is 6n137 which is an optically coupled gate that combines a GaAsp light emitting diode and an integrated high gain photo detector. An enable input allows the detector to be strobed, The output of the detector `IC is inversion of the applied input. The PWM signal from the FPGA are not capable of driving the MOSFETs. On order to strengthen the pulses a driver circuit is provided. The result of the experimental study are shown in the form of the oscillograms of PWM outputs and harmonic spectrum of chosen CMLI. Figs. 35–44 Show the experimental output voltage and corresponding harmonic spectrum of chosen CMLI obtained using SPARTAN-3E with PD, POD, APOD, PS and Hybrid PWM strategy respectively. The input voltage of each H-bridge is 20V. Figure 34 shows the entire hardware setup. Table. 6 and 7 Show the comparison of %THD of output voltage with different PWM strategies for various values of modulation index.

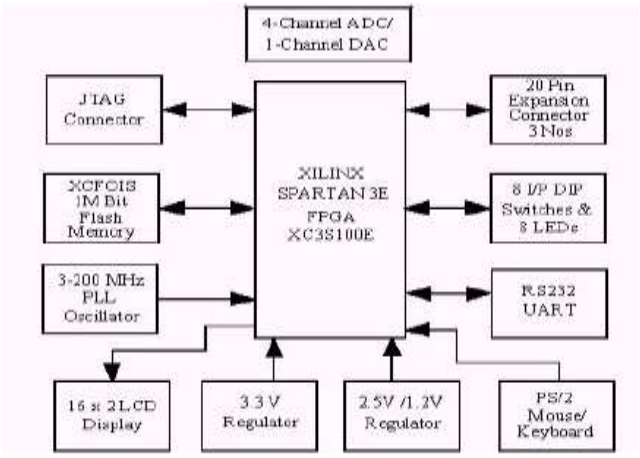

Figure 33. Spartan 3E development board block diagram

Figure 34. Entire hardware setup

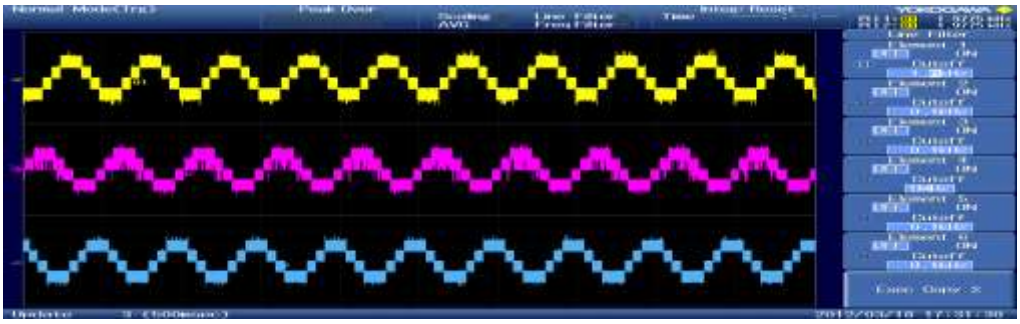

Figure 35. Output voltage generated by PDPWM strategy for R-L load. (m_a=0.8 and m_f=63)

Figure 36. FFT plot for output voltage of PDPWM strategy for R-L load (m_a=0.8 and m_f=63)

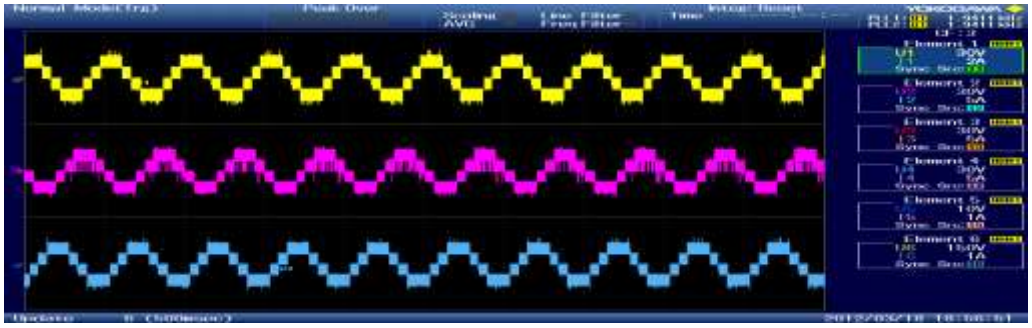

Figure 37. Output voltage generated by PODPWM strategy for R-L load. (m_a=0.8 and m_f=63)

Figure 38. FFT plot for output voltage of PODPWM strategy for R-L load (m_a=0.8 and m_f=63)

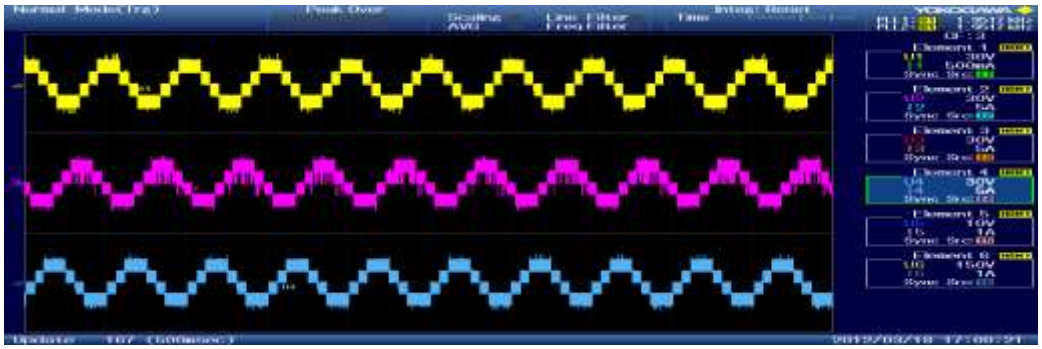

Figure 39. Output voltage generated by APODPWM strategy for R-L load. (m_a=0.8 and m_f=63)

Figure 40. FFT plot for output voltage of APODPWM strategy for R-L load (m_a=0.8 and m_f=63)

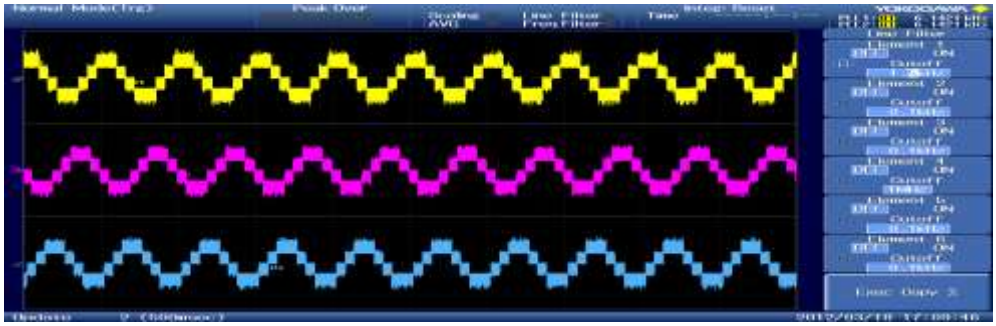

Figure 41. Output voltage generated by PSPWM strategy for R-L load. (m_a=0.8 and m_f=63)

Figure 42. FFT plot for output voltage of PSPWM strategy for R-L load (m_a=0.8 and m_f=63)

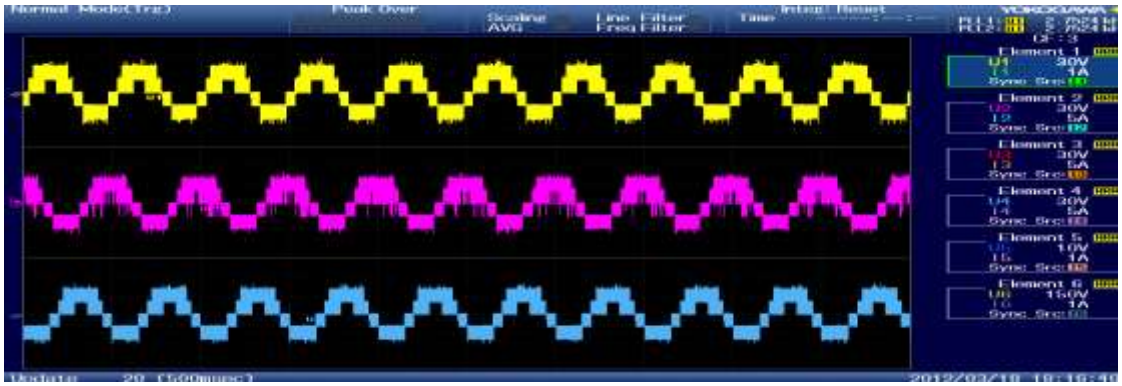

Figure 43. Output voltage generated by HYBRIDPWM strategy for R-L load. (m_a=0.8 and m_f=63)

Figure 44. FFT plot of output voltage generated by HYBRIDPWM strategy for R-L load. (m_a=0.8 and m_f=63)

Table 6. %THD for Different Modulation Indices for R-L Load (by Experiment)

m_a	PD 3.15KHz	POD 3.15KHz	APOD 3.15KHz	PS 3.15KHz	HYBRID 3.15KHz
0.9	2.070	2.083	1.645	3.504	2.466
0.85	2.568	2.337	2.219	1.802	2.508
0.8	2.597	2.089	2.447	1.881	2.250
0.75	1.781	1.908	2.425	2.070	2.445
0.7	3.246	2.094	2.150	2.151	2.438
0.65	2.603	2.306	2.329	2.143	2.772
0.6	3.324	2.172	2.124	2.355	3.256

Table 7. V_{rms} (Fundamental) % THD for Different Modulation Indices for R-L Load (by Experiment)

m_a	PD 3.15KHz	POD 3.15KHz	APOD 3.15KHz	PS 3.15KHz	HYBRID 3.15KHz
0.9	26.33	26.49	26.42	27.17	26.32
0.85	25.02	25.37	25.64	24.38	26.39
0.8	23.69	23.96	23.95	22.94	25.21
0.75	22.53	22.77	22.76	21.87	24.87
0.7	21.36	21.26	21.27	20.41	23.62
0.65	19.92	19.61	20.06	19.08	22.15
0.6	18.31	18.33	18.58	17.60	19.28

6. CONCLUSION

Three phase multilevel inverter fed R-L load is simulated using the blocks of Simulink in this work. The simulation results are compared for two different switching frequencies. It is observed that HYBRID and PSPWM methods provide output with relative low distortion for low and high f_c respectively and PODPWM and PSPWM are found to perform better since they provide relatively higher fundamental RMS output voltage for R-L load with f_c=6 and 3.15KHz respectively. If the switching frequencies are increased there is a slight decrease in the THD and slight increase in the Vrms. Table 1 displays the THD

values for different PWM strategies for both m_a. Table 2 shows the Vrms values for various modulation indices. Table 3 shows the crest factor for both m_a. Table 4 display the form factor for different modulation indices. Table 5 provides the distortion factor. The experimental results shows PSPWM provide output with low distortion and HYBRID provide output with high fundamental RMS voltage for f_c=3.15KHz. The experimental results were obtained only for f_c=3.15KHz.

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