**International Journal of Reconfigurable and Embedded Systems (IJRES)**
Vol. 4, No. 3, November 2015, pp. 213~218
ISSN: 2089-4864


# Design and Implementation of Four Bit Binary Shifter Circuit Using Reversible Logic Approach

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**Article Info**

***Article history:***

Received Mar 2, 2015
Revised Jun 19, 2015
Accepted Jul 12, 2015

***Keyword:***

Four bit combinational shifter
Low power design
Reversible Circuit Design
Reversible Logic Gates

**ABSTRACT**

Shifter circuits are the key component of arithmetic logic unit as well as storage unit of any digital computing device. Designing these shifter circuits using reversible logic approach leads to create low power loss digital systems. Reversible circuit design approach is nowadays widely applicable in various disciplines such as Nanotechnology, Low power CMOS design, Optical computing etc. This paper presents two design approaches for four bit binary combinational shifter circuit with the help of different types of reversible logic gates. The proposed optimized design is simulated using Modelsim tool and synthesised for Xilinx Spartan 3E with Device XC3S500E with 200 MHz frequency.



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## 1. INTRODUCTION

Minimization of generated heat from electronic devices due to the information loss is the key motivation for researchers to work in the area of reversible circuit design. R. Landauer (1961) and C. H. Benette (1973) has concluded that redesigning digital circuits using reversible logic gates ideally leads to the lossless digital devices [1-3].

Till now remarkable work has been done in the low power loss combinational circuit designs using reversible logic approach. Among these combinational circuits, shifter is one of the significant circuit. These shifter circuits are key components of any processing or storage unit.

This paper presents two design approaches for four bit binary combinational shifter circuit using reversible logic gates. Depending upon the minimization of performance parameters the optimized design is simulated and synthesized for further low loss design considerations.

This paper is organized in six sections. Section I and II provides the introduction of the work and basic concepts of reversible logic respectively. Section III and IV elaborate conventional approach and proposed designs for four bit binary shifter circuit respectively. Section V gives the result and analysis of the proposed work. The paper is concluded in section VI at the end.

## 2. BASIC CONCEPTS OF REVERSIBLE LOGIC DESIGN

Conventional logic gates are considered irreversible due to the information loss from the device. Reversible logic approach targets to redesign the aimed digital circuit using reversible design entities [4-7]. These design entities are various available reversible logic gates. Following subsections describe some basic terms of reversible circuit design:

### A. Reversible Logic Gates

These are defined as (N, N) digital logic gates with one to one mapping between input and output bits [8-13]. Information of output bits at any instance provides the knowledge of applied input bits. Apart from these some other characteristics of reversible logic gates are equal number of input and output signals, low fan-out and any output bit is high for half the number of total input combinations possible. Figure 1 shows the block diagram of a typical (N, N) reversible logic gate.

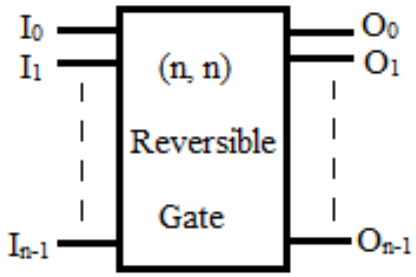
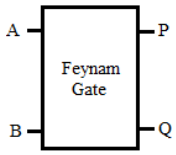
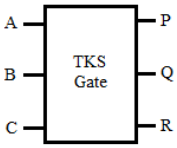
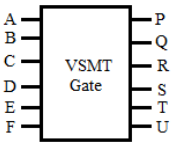



Figure 1. Block diagram of a (N, N) reversible logic gates

### B. Examples of Some Reversible Logic Gates

Till now researchers have already proposed various reversible logic gates such as feynman, toffoli, TKS, VSMT gate etc [14-20]. Any reversible digital circuit can be designed using the combination of these reversible logic gates. Table 1 details some reversible logic gates with their size, block deigaram and output equations.

Table 1. Examples of some reversible logic gates

| No. | Name | Size | Block Diagram | Output Equations |
|---|---|---|---|---|
| 1 | Feynman Gate | 2×2 |   | $P = A;$ $Q = A \oplus B;$ |
| 2 | TKS Gate | 3×3 |   | $P = A.C' + B.C;$ $Q = A \oplus B \oplus C;$ $R = A.C + B.C';$ |
| 3 | VSMT Gate | 6×6 |   | A = E'.(A.F'+B.F)+E.(C.F'+D.F) $Q = A \oplus B \oplus C;$ $R = E \oplus F;$ $S = C \oplus D;$ $T = D \oplus E \oplus F;$ $U = E;$ |

### C. Reversible Circuit Design

Any digital circuit is redesigned using reversible logic gates with an aim for ideal reversible circuit with no power loss [21-25]. Designed reversible circuit is characterized with zero garbage output, zero constant input, no feedback and minimum number of reversible gates used in the design etc. But in practical aspects these performance parameters are optimized to produce most suitable design solution for the aimed digital circuit.

### D. Garbage Output Signals

These are described as the undesired output signals generated from the designed reversible circuit. These signals contribute to the information loss which leads to the power loss from the designed device. Thus garbage output signals are required to be minimized from reversible circuit designs.

## 3. CONVENTIONAL FOUR BIT BINARY COMBINATIONAL SHIFTER CIRCUIT DESIGN

A shifter circuit performs shifting of applied bits in both directions i.e. left and right [26-28]. Here we require four 4:1 multiplexer circuits to perform the desired shift operations as shown in table 2 below.

Table 2. Function table of shifter

| S. No. | $S_1$ | $S_0$ | Functions performed |
|---|---|---|---|
| 1 | 0 | 0 | O ← F |
| 2 | 0 | 1 | O ← Shr F |
| 3 | 1 | 0 | O ← Shl F |
| 4 | 1 | 1 | O ← 0 |

To design this four bit shifter conventional logic gates are used for the design and implementation in conventional approach of digital circuit design.

This shifter circuit is very useful in arithmetical, logical and storage applications. Utility of this shifter circuit in these fields demands the reversible design of shifter for the generation of low loss processing systems.

## 4. PROPOSED DESIGNS FOR FOUR BIT BINARY COMBINATIONAL SHIFTER CIRCUIT USING REVERSIBLE LOGIC APPROACH

Here we have designed the aimed four bit binary combinational shifter circuit through two different approaches as discussed in the subsequent subsections.

### A. Design 1

Initially TKS gate was considered as the most suitable reversible logic gate to design multiplexer circuits using reversible logic approach. So this design approach for four bit binary shifter circuit utilizes only TKS gates as shown in figure 2 below.

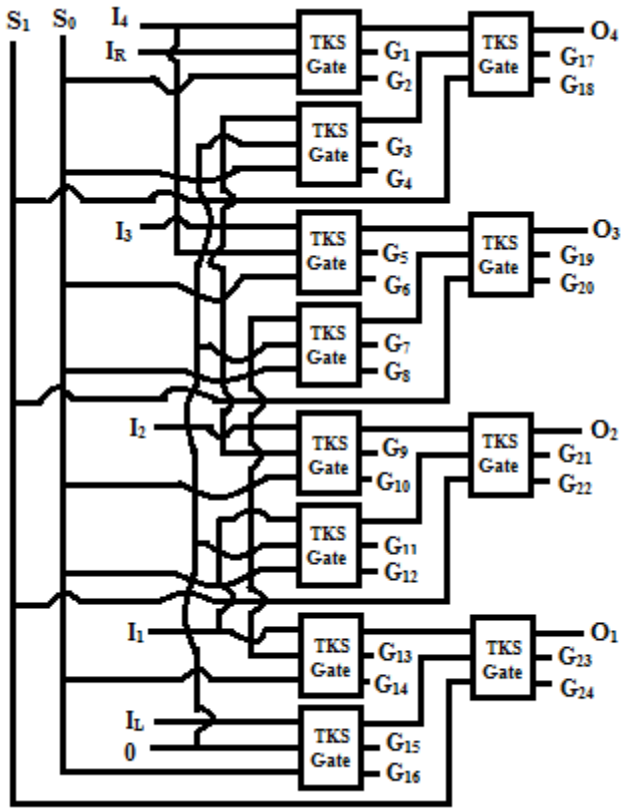



Figure 2. Proposed design 1 for four bit binary combinational shifter circuit using reversible logic gates

This design requires a total of 12 TKS gates which generate 24 garbage output signals.

### B. Design 2

This design employs only four VSMT gates to design the aimed shifter circuit using reversible approach. Total garbage generation from this design approach is 17 as shown in figure 3 below.

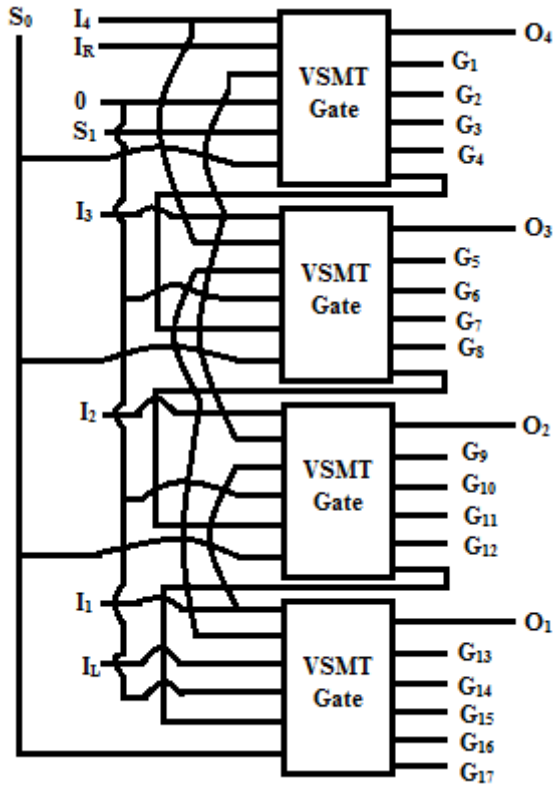



Figure 3. Proposed design 2 for four bit binary combinational shifter circuit using reversible logic gates

## 5. RESULT AND ANALYSIS

As discussed earlier the two proposed designs for four bit binary combinational shifter circuit using reversible logic are compared on some selected performance parameters such as total number of reversible gates used in the design and total garbage output signals generated. The comparison table for these designs are shown in table 3 and after that figure 4 shows the comparison chart of the same.

Table 3. Comparison Table

| S. NO. | Design | Total reversible gates | Garbage output |
|---|---|---|---|
| 1 | Design 1 | 12 | 24 |
| 2 | Design 2 | 4 | 17 |

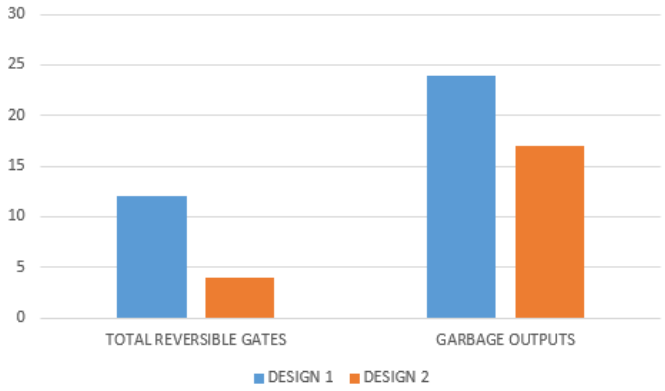



Figure 4. Comparison chart

From above comparison we can conclude that design 2 is more optimized design for four bit binary combinational shifter circuit using reversible logic approach depending upon the considered performance parameters. This design is simulated using Modelsim tool and synthesised for Xilinx Spartan 3E with Device XC3S500E with 200 MHz frequency. Figure 5 gives the simulated waveform of the proposed design 2 using VSMT gates as shown in figure 5. The designed reversible circuit conforms to the function table of aimed shifter circuit as shown in table 2.

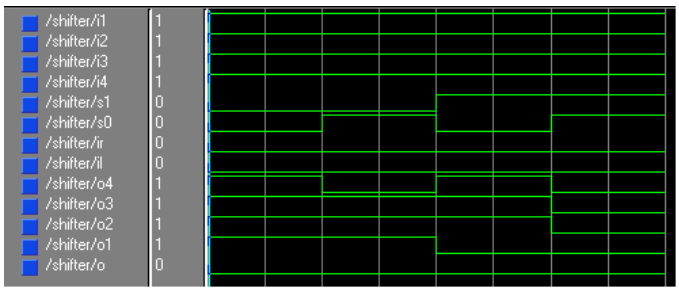



Figure 5. Simulated waveform of the proposed four bit shifter ciruit using reversible logic approach

## 6. CONCLUSION

This paper presents two design approaches for four bit combinational shifter circuit using reversible logic approach. These designs are optimized on some selected performance parameters such as total reversible gates and garbage output signals. The optimized design uses only four VSMT gates and generates 17 garbage outputs. This design is simulated using ModelSim simulator and synthesized for Xilinx software. Future scope for this work may be considered as the optimization of various performance parameters to improve the efficiency of digital systems with the design of other low power loss processing and storage digital systems.

## ACKNOWLEDGEMENTS

Authors are thankful to Mr. Aseem Chauhan (Additional President RBEF, Chancellor AUR), Maj. General K. K. Ohri, AVSM (Retd.), Pro Vice Chancellor, AUUP, Lucknow Campus, Wing Cd (Dr) Anil Kumar Tiwari (Director, ASET) and Brig. Umesh K. Chopra (Director, AIIT, & Co-ordinator, ASET) for their cooperation, motivation and suggestive guidance.

## REFERENCES

[1] R. Landauer, "Irreversibility and Heat Generation in the Computational Process", *IBM Journal of Research and Development*, 5, pp. 183- 191, 1961.
[2] G.E. Moore, "Cramming more compounds onto integrated circuits", *Elecronics*, Vol. 38, No. 8, April 19, 1965.

[3] C.H. Bennett, "Logical Reversibililty of Computation", *IBM J. Research and Development*, pp. 525-532, November 1973.
[4] Majid Haghparast, Keivan Navi, "A Novel Fault Tolerant Reversible Gate for Nanotechnology Based Systems", *American Journal of Applied Sciences*, Vol. 5, (5), pp. 519-523, 2008.
[5] M. Morrison, N. Ranganathan, "A novel optimization method for reversible logic circuit minimization", *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, pp. 182-187, 2013.
[6] Himanshu Thapliyal and Nagarajan Ranganathan, "Design of Efficient Reversible Binary Subtractors Based on A New Reversible Gate", *IEEE Computer Society Annual Symposium on VLSI*, pp. 229-234, 2009.
[7] Lihui Ni, Zhijin Guan, Xiaoyu Dai and Wenjuan Li, "Using New Designed NLG Gate for the Realization of Four-Bit Reversible Numerical Comparator", *International Conference on Educational and Network Technology (ICENT-2010), IEEE*, pp. 254-258, 2010.
[8] Himanshu Thapliyal and M.B Srinivas, "A New Reversible TSG Gate and Its Application For Designing Efficient Adder Circuits", 7th *International Symposium on Representations and Methodology of Future Computing Technologies (RM 2005)*, Tokyo, Japan, September 5-6, 2005.
[9] T. Toffoli, "Reversible Computing", Tech memo MIT/LCS/ TM-151, MIT Lab for Computer Science, 1980.
[10] E. Fredkin and T. Toffoli, "Conservative Logic", *Int'l J. Theoretical Physics*, Vol. 21, pp. 219- 253, 1982.
[11] R. Feynman, "Quantum Mechanical Computers," *Optics News*, Vol. 11, pp. 11–20, 1985.
[12] Peres, "Reversible Logic and Quantum Computers", *Physical review A*, 32: 3266- 3276, 1985.
[13] Diganta Sengupta, Mahamuda Sultana, Atal Chaudhuri, "Realization of a Novel Reversible SCG Gate and its Application for Designing Parallel Adder/Subtractor and Match Logic", *International Journal of Computer Applications*, Vol 31, No. 9, pp. 30-35, October 2011.
[14] Vandana Shukla, O.P. Singh, G.R. Mishra, R.K. Tiwari, "Design of a 4-bit 2's Complement Reversible Circuit for Arithmetic Logic Unit Applications", *The International Conference on Communication, Computing and Information Technology (ICCCMIT), Special Issue of International Journal of Computer Applications*, pp. 1-5, 2012.
[15] Lavanya Thunuguntla, Bindu Madhavi K, Pullaiah T, "Designing of Efficient Online Testable Reversible Multiplexers and DeMultiplexers with New Reversible Gate", *International Journal of Engineering Research and Applications (IJERA)*, Vol. 2, Issue 2, pp. 183-191, Mar-Apr 2012.
[16] Md. Mahfuzzreza, Rakibul Islam, Md. Belayet Ali, "Optimized Design of High Performance Reversible Multiplier Using BME and MHNG Reversible Gate", *American International Journal of Research in Science, Technology, Engineering & Mathematics*, IASIR USA, Vol. 2(2), pp. 227-232, March-May 2013.
[17] M.P Frank, "*Introduction to Reversible Computing: Motivation, Progress and Challenges*", Proceedings of the 2nd Conference on Computing Frontiers, pp. 385–390, 2005.
[18] Nagamani AN, Jayashree HV, HR Bhagyalakshmi, "Novel Low Power Comparator Design using Reversible Logic Gates", *Indian Journal of Computer Science and Engineering (IJCSE)*, Vol. 2, No. 4, pp. 566-574, Aug -Sep 2011.
[19] Majid Haghparast, Maryam Hajizadeh, Rogayye, Rozhin Bashiri, "On the Synthesis of Different Nanometric Reversible Converters", *Middle-East Journal of Scientific Research*, vol. 7, issue 5, pp. 715-720, 2011.
[20] Vandana Shukla, O.P. Singh, G.R. Mishra, R.K. Tiwari, "A novel approach to design decimal to BCD encoder with reversible logic", *International Conference on Power, Control and Embedded Systems (ICPCES), IEEE*, pp. 1-5, 2014.
[21] Y.Syamala, A.V.N Tilak, "Reversible Arithmetic Logic Unit", 3rd *International Conference on Electronics Computer Technology (ICECT)*, Vol. 5, pp. 207-211, 2011.
[22] J.W. Bruce, M.A. Thornton, L. Shivakumaraiah, P.S. Kokate, and X. Li, "Efficient Adder Circuits Based on a Conservative Reversible Logic Gate", *IEEE Computer Society Annual Symposium on VLSI*, April 25-26, 2000, Pittsburgh, Pennsylvania.
[23] Majid Haghparast and Keivan Navi "A Novel Reversible Full Adder Circuit for Nanotechnology Based Systems" *Journal of Applied Sciences*, Vol. 2(24), pp. 3995-4000, 2007.
[24] R. Aradhya, R, Chinmaye, and K. Muralidhara, "Design, Optimization and Synthesis of Efficient Reversible Logic Binary Decoder," *International Journal of Computer Applications*, Vol. 46, pp. 45-51, 2012.
[25] H. P. Shukla, A. G. Rao, P. Mall, "Design of low power comparator circuit based on reversible logic technology", 1st *International Conference on Emerging Trends and Applications in Computer Science (ICETACS), IEEE*, pp. 6-11, 2013.
[26] Irina Hashmi and Hafiz Md. HasanBabu, "An Efficient Design of a Reversible Barrel Shifter", 23rd *International Conference on VLSI Design*, 2010, pp.93-98.
[27] M. M. Mano (1979), *Digital logic and computer design*, Prentice-Hall, Inc. (New York).
[28] William I. Fletcher (1980), *An engineering approach to digital design*, PHI Learning Private Limited, (India).