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Design and Implementation of Recursive Least Square Adaptive Filter Using Block DCD approach

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ABSTRACT

Due to the explosive growth of multimedia application and tremendous demands in Very Large Scale Integrated (VLSI), there is a need of high speed and low power digital filters for digital signal processing applications. In Digital Signal Processing (DSP) systems, Finite Impulse Response (FIR) filters are one of the most common components which is used, by convolving the input data samples with the desired unit sample response of the filter. The proposed work deals with the design and implementation of RLS adaptive filter using block DCD approach. The evaluation of speed, area and power for proposed work will be done. Also, the comparison of the proposed design with the existing will be carried out for various input combinations.

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1. INTRODUCTION

An adaptive filter is a computational device that attempt to model the relational device between two signals in real time environment in an iterative manner. Adaptive filter are often realise either as a set of program instruction running on an arithmetical processing device such as microprocessor or DSP (digital signal processor) chip or as set of logic operation implemented in FPGA or in semicustom or custom VLSI circuit however ignoring any error introduced by numerical precision effect. In this implementation, the fundamental operation of an adaptive filter can be characterised independently of specific physical realization that it take. For this reason proposed method focuses on their specific realization in software and hardware [1-3].

The demand and popularity of portable electronics is driving designers make great efforts to achieve for small silicon area, higher speeds, and power dissipation and reliability. The proposed work deals with the design and performance analysis of Adaptive Filter in VLSI. Figure1 shows the basic concept of the adaptive filter which uses Least Mean Square Algorithm for minimizing the error [4-5].

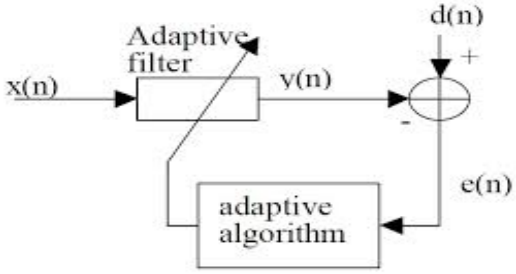

Figure 1. Generalized structure of adaptive filters

The disadvantage of LMS algorithm is that, it cannot meet the requirement of fast rate of convergence and minimum MSE. The best choice is to use the block recursive least squares (RLS) algorithm to overcome the above difficulty. Block Recursive Least Square-DCD (Dichotomous Coordinate Decent) algorithms are known to exhibit better performances. And is one of the variants algorithm in which the updating of weights is done at block level and the error values are calculated at every clock cycle. The weights are updated once per every block data instead of updating on every clock cycle of input data. The error values are calculated at every clock cycle [6-9]. Figure 2 RLS adaptive filter shows u (n) is the input and y (n) is the output of the filter. d (n) desired response of Adaptive filter Error denoted by e(n) this error is subtract with filter output and desired output i.e. e(n) = y(n)-d(n) and it's called as estimation error. The aim of this filtration is to remove the estimation error. λ is step-size which is used for adaptation of the weight vector, the tap-weight vector *w(n)* and the tap-input vector *u(n)* is defined as follows

$$W(n) = [w_0(n), w1(n), \ldots, wn_{-1}(n)]^T$$

$$u(n) = [u(n), u(n-1), \ldots, u(n-N+1)]^T$$

$$k(n) = \frac{\lambda^{-1}P(n-1)u(n)}{1+\lambda^{-1}u^H(n)P(n-1)u(n)}$$

$$\xi(n) = d(n) - \hat{w}(n-1)u(n)$$

$$\hat{w}(n) = \hat{w}(n-1) + k(n)\xi^*(n)$$

$$P(n) = \lambda^{-1}P(n-1) - \lambda^{-1}k(n)u^H(n)P(n-1).$$

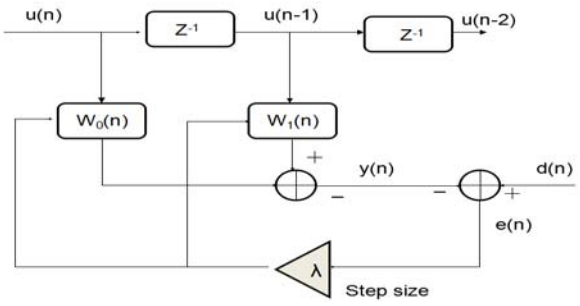

Figure 2. RLS Adaptive filter

The Z-inverse is a delay element used for controlling the input of filter. Whenever the first input is given to the filter u(n) at that time other input have stand-by condition then second input are given to filter that is u(n-1) at a time many inputs not proccess becouse of delay. The proposed dissertation work deals with the design of simple architecture for the implementation of a variant of Block DCD RLS-algorithm where the weight updating and error calculation are both calculated in block wise fashion.

2. RELATED WORK

Adaptive filter is forms the important basis for many real time digital signal processing applications. Many researchers have worked on adaptive filters for various diverse applications. The detail literature survey for the proposed dissertation is as follows:

The Important work is carried out by Jafar Saniie et al., in which author proposed the Hardware and Software Design for QR Decomposition Recursive Least Square Algorithm. An embedded hardware and software system was design and implementation for QR Decomposition Recursive Least Square (QRD-RLS) algorithm using Given's Rotation method for optimizing the area and power [1].

Dr. C. Vijaykumar et al. presented one of most important implementation of low power systolic base adaptive filter by deigning the RLS Adaptive Filter architecture using FPGA technology with clock getting. Systolic array architecture were used to reduce the circuit scale into half without impairing the processing speed and clock gating which results in the considerable reduction in power[2].

Md. Zulfiquar Ali et al., author suggest the New Improved Recursive Least-Square Adaptive-Filtering Algorithms. In this paper two new improved recursive least-squares adaptive-filtering algorithms, one with a variable forgetting factor and the other with a variable convergence factor are proposed. Optimal forgetting and convergence factors are obtained by minimizing the mean square of the noise-free a posterior error signal [3].

Author Cristian Stanciul et al., says that in Numerical Properties of the DCD-RLS Algorithm for Stereo Acoustic Echo Cancellation, Modern teleconferencing systems have been developed in recent years to use multiple acoustic channels (stereo communication). This feature improves the quality of Communication (e.g., in terms of spatial localization), but the classic problem of the acoustic echo cancellation becomes more complicated. In this context, the dichotomous coordinate descent (DCD) - recursive least-squares (RLS) algorithm can be an attractive choice for hardware implementation [5].

Other work carried by Yuriy Zakharovt, et al., in which Fast RLS algorithm using dichotomous coordinate descent iterations in this the Recursive Least Squares (RLS) adaptive filtering problem is expressed in terms of auxiliary normal equations with respect to increments of the filter weights. By applying this approach to the exponentially weighted case, a new structure of the RLS algorithm is derived. For solving the auxiliary equations, dichotomous coordinate descent (DCD) iterations with no explicit division and multiplication are used [8].

From the review of various papers, it is found that DCD algorithm is used for minimizing the iteration with greater speed and it can be very useful for Hardware implementation also. Existing methods is base on matrix inversion problem. However, the proposed method can be used to overcome the problem of matrix inversion by using Block DCD-RLS algorithm.

3. CONCLUSION

Adaptive filtering techniques can be used in many applications in different fields, such as wireless communication and channel equalization, noise cancelling, channel estimation.

The serial implementation of the real-valued Block DCD algorithm will be the smallest hardware implementation and it is notable for smaller than any other methods requiring multiplication operations. However, the update rate is limited as the residual vector is updated sequentially.

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