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# Design of Low Power Dual Dynamic Node Flip-Flop Using Sleep Transistor with NMOS

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**ABSTRACT**

This paper introduces a Low Power Dual Dynamic Node Flip Flop(DDFF) using Sleep Transistor with NMOS. The proposed design retains the logic level till the end of evaluation and pre-charge mode. The low power DDFF architecture that combines the advantages of dynamic and static CMOS structures. The sleep transistors approach is used for leakage power reduction. It reduces leakage current in ideal mode. The performance of the proposed flip flop was compared with the conventional dual dynamic node flip flop (DDFF) in 90nm CMOS technology with 1.2v supply voltage at room temperatures. Also, conventional DDFF and DDFF using Sleep Transistor with NMOS are compared with other complicated designs and realizes by a 4-bit Johnson up and down counter. The performance improvements indicates that the proposed designs are suited for modern high-performance CMOS circuits where leakage power and power delay product overhead are of major concern.



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## 1. INTRODUCTION

The low power chip and system are using for both industrial and educational purposes. The industry for low power electronic products are increasing rapidly in market. At the same time, newly emerging CMOS processing technologies present more requirements to the power dissipation of digital system due to increased device count, speed and complexity. Power dissipation of VLSI chips has been continuously increasing. For high performance low power CMOS chip-design the choice of method has a significant effect, on the design time and cost. Large no of gates are present in the VLSI CMOS system and gates are having different parameters due to process variation.

Power dissipation in CMOS structures comes from two components 1) Static dissipation is due to tunnelling current through gate oxide, leakage current through reverse-biased diodes, contention current in ratioed circuits and current conduction through OFF transistors. Static power consumption is given by [3]

$$P_{static} = I_{static} * Vdd$$

Where $I_{static}$ is the current that flow in the absence of switching. (2) Dynamic dissipation is due to charging and discharging of load capacitances. If gate is switched on and off per second then power consumption is given by [3]

$$P_{dynamic} = f * C * Vdd^2$$

Where f is the clock frequency, C is load capacitance and Vdd is supply voltage.

In synchronous system we are using flip flops. High speed has been achieved using pipelined techniques [1]. In progressive, deep-pipelined architectures, pushing the speed excepting demands a lower pipeline overhead. This overhead is latency analogous with the pipeline elements, similar as flip-flops and latches. Substantially, work has been dedicated to improve the performance of the flip-flops in the past few decades. The factors which are recommendable in latches and flip-flops are (1) High speed, (2) Low power consumption, (3) Robustness and noise stability, (4) Small area and less number of transistors, (5) Supply voltage scalability, (6) Less internal activity in ideal condition.

Hybrid latch flip-flop (HLFF) and semi dynamic flip-flop (SDFF) are observing the classic high-performance of flipflops [1]. Flip-flops can be designed by two type (1) Static logic, (2) Dynamic logic style. Dynamic logic occupies less area and high speed, on otherhand static logic cannot have charge sharing problem. Now we consider a hybrid flip flop which is working like dynamic and static logic [1], [3]. Hybrid design has an internal dynamic node and static output node, in flip flop design. On other hand semi dynamic flip-flop (SDFF) works efficiently and have different capabilities. It helps to reduce the latency in flip flop design. Power, delay and area are main concerns.

In recent year other new flip-flops were introduced like cross charge control flip-flop (XCFF), which has many advantages over other types of flip-flops in speed and power [1]. But this architecture still has some drawbacks because of redundant power dissipation and large hold time. High performance flip- flop will have a high clock frequency to speed up the system. Due to high clock frequency of system having large amount power dissipation. Today this is challenging for electronic engineers.

This paper is divided as follows: (2) Study of existing flip flop, (3) Proposed low power DDFF architecture and operation of proposed flip-flop, (4) Proposed ELM, (5) Simulation setup and result, (6) conclusion.

## 2. EXISTING FLIP-FLOPS

Dual dynamic node flip-flop is a classic high-performance flip-flop. Conventional hybrid latch and semi dynamic flipflops are some kind of hybrid flip-flops. The speed of HLFF is slow but it consumes less power. Charge sharing problem can be reduced using splitting internal capacitance. Semi dynamic flip-flop is faster, with shorter hold time and a better input noise rejection but more power is consumed. New hybrid flipflop is given below which is better than above one. Which is operated under two mode (1) evaluation phase (2) pre-charge phase [1].

### A. Evaluation phase

In this phase if CLK =1 then it works in evaluations phase. And input data (D) =0 than node is discharged through the N1, N2, N3. The logic value will be 0. This latching occurs during the 1-1 overlapping of CLK and CLKB. The logic value zero is maintained by the inverter pair INV1 and INV2 till evaluation phase gets over. The node X1B is high in all process and QB (QBAR) discharge to zero. The output maintained by inverter pair INV3 and INV4 till next evaluation phase. The node X2 is high when input data (D) = 1 throughout the evaluation phase. If input data (D) = 0, Then X1 node will be logic 1 and X2 will be at logic 0. QB will be charged through P2. X2 remain zero till end[1].

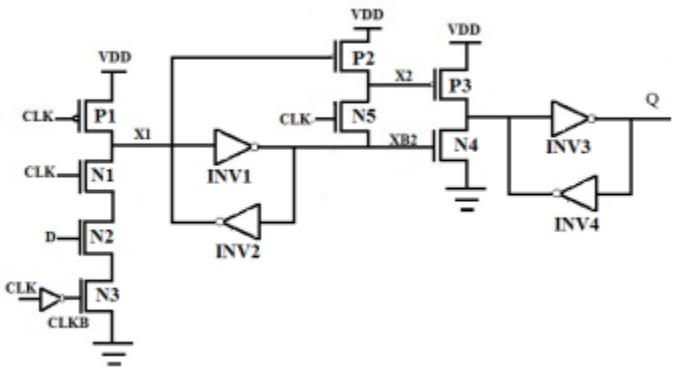


Figure 1. DDFF

**B. Pre-charge phase**

In this CLK=0 and input data (D) could be either zero or one. It can also be called as holding phase. The X1 node remains logic 1 and X1B will be logic 0. N1 transistor stops the taking of next value of input data (D) until the end of precharge phase [1]. So the previous value of output will be held. This design has negative setup time and positive hold time. It has short transparency period because of 1-1 overlapping of CLK and CLKB. This eliminates race condition. The inverter pair INV1, INV2 and INV3, INV4 were designed with static CMOS. Due to this inverter pair large leakage current is present in the flip-flop. When technology scales down to 90nm and below then it consume unnecessary power.

## 3. PROPOSED FLIP FLOP

In the proposed flip flop the inverter pairs are designed using leakage power reduction technique known as sleep transistor approach with NMOS. The static CMOS inverter pair is replaced by sleep transistor approach with NMOS. When a static CMOS inverter is used below 90nm technology, the supply voltage is reduced which causes threshold voltage reduction that will further increases leakage current. This technique is a combination of the sleep transistor and NMOS stack technique. It uses the high threshold transistors i.e., multi-threshold technique [3], [4].

The sleep transistor approach with NMOS is shown in the Figure 3 P1, N2, are high threshold and N1, P2, N3 are low threshold voltage transistors. It works in two mode (1) Active mode, (2) Sleep mode

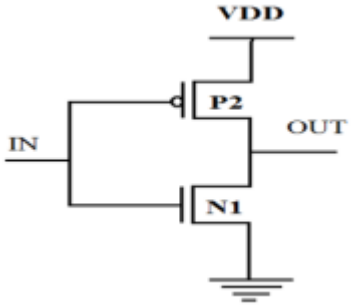


Figure 2. Basic Inverter

Sleep Transistors are high threshold transistors connected in series with low threshold logic as shown Figure 3. When the main circuit consisting of low threshold devices are ON the sleep transistors are also ON resulting in normal operation of the circuit.

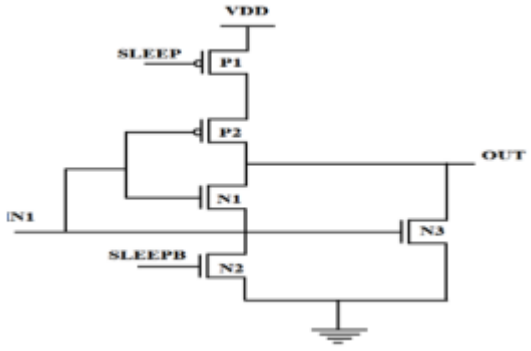


Figure 3. Sleep Transistor with NMOS

When the circuit is in Standby mode even high threshold transistors are OFF. Since high threshold devices appear in series with low threshold circuit the leakage current is determined by high threshold

devices and is very low. So the net static power dissipation is reduced.in addition one low transistor parallel is added in pull down networks which increases the threshold voltage and improves the leakage current.

The proposed flip flop is shown in figure 3. When this Sleep Transistor with NMOS is used in the flip flop, then power reduction in flip flop can be done by operating the flip flop in sleep mode. The total power is also reduced in active mode. This operates in evaluation phase and pre-charge phase. The latching of data input occurs in evaluation phase and holding of the output data occurs in pre-charge phase.

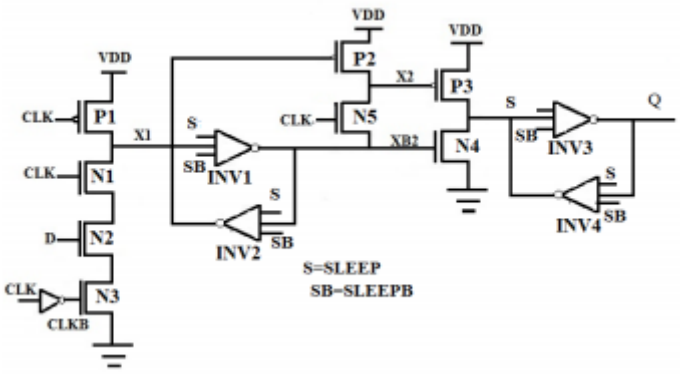


Figure 4. Proposed DDFF using Sleep Transistor approach with NMOS

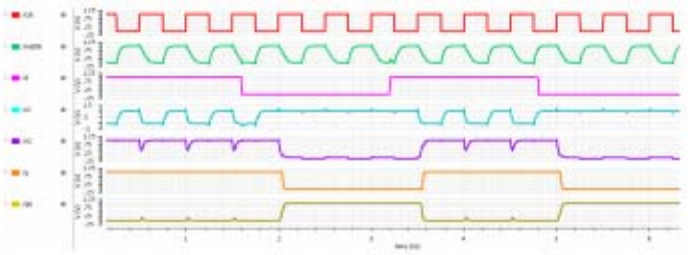

Figure 5. Output Waveform of Proposed DDFF

## 4. PROPOSED ELM

The proposed dual dynamic hybrid flip flop with embedding logic is shown in figure 5. Note that in proposed embedding logic model, the input data (D) is replaced by pull down network of CMOS and the clocking scheme is charge sharing. Charge sharing problem occurrs in the model due to the clocking. Which becomes insubordinate as the number of NMOS transistor in the pull down network increases.

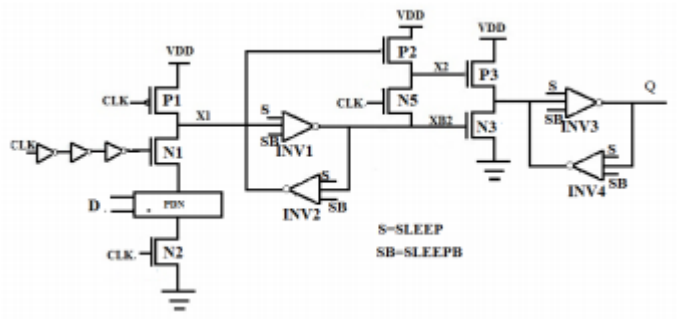


Figure 6. Proposed DDFF Embedded

It has been simulated and examined with different embedded logic and the amount of worst case charge sharing has been calculated.

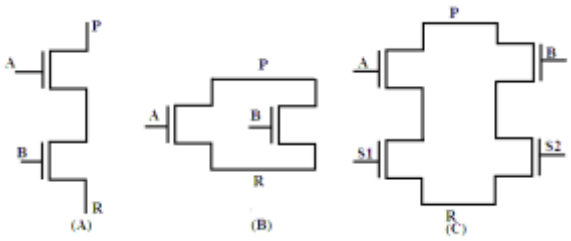


Figure 7. Embedded Function (A) AND. (B) OR. (C) 2:1 MUX

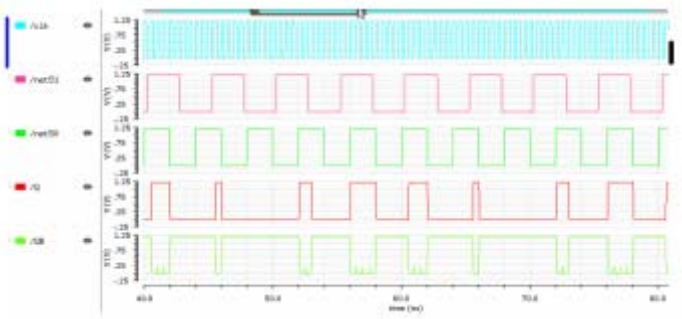

Figure 8. Output Waveform of 2 Input AND

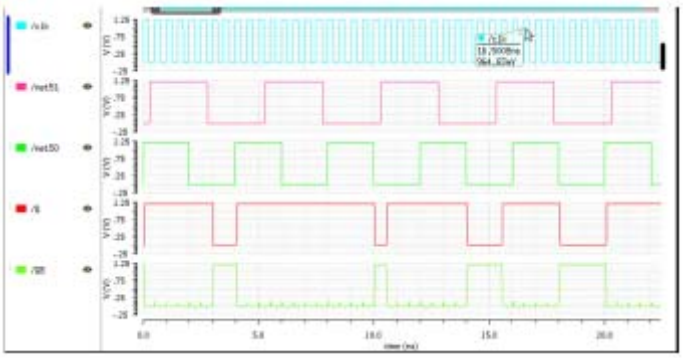

Figure 9. Output Waveform of OR

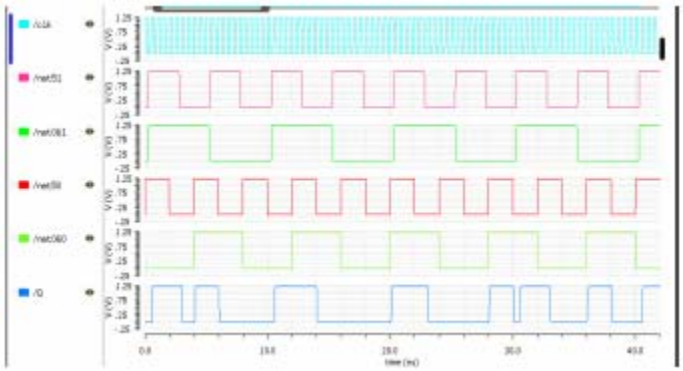

Figure 10. Output Waveform of MUX

## 5. SIMULATION SETUP AND RESULTS

Cadence is leading provider of PC based electronic design automation software solution. Power consumption and speed performances are examined for existing and proposed model.

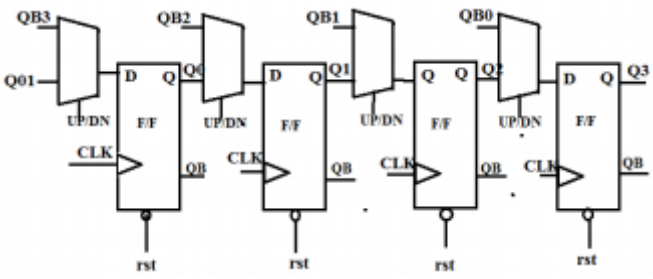


Figure 11. 4-bit Johnson up and down counter

The simulation were performed in 90nm technology. The supply voltage is given as 1.2v for the simulation. The flip flop operated at 2 GHz clock frequency. It has negative set up time and positive hold time with respect to CLK and CLKB. Finally a 4-bit Johnson up and down counter is designed for the performance analysis of DDFF using sleep transistor approach with NMOS. The reason of choosing a counter is that the internal data activity at each bit is known.

Table I. Inverter performance

| Inverter Name | Leakage Power | Total Power |
|---|---|---|
| CMOS Inverter | 5952.5pW | 458nW |
| Sleep Transistor with NMOS | 1863pW | 325nW |

Table II. Performance of DDFF

| Flip Flop | Leakage Power | Total Power | Dealy | PDJ |
|---|---|---|---|---|
| DDFF | 5059nW | 55.86uW | 4.6899ns | 202.4fJ |
| Proposed DDFF | 20.74nW | 53.70uW | 3.008ns | 168fJ |

Table III. Total power consumption at different data activity by DDFF

| Flip Flop/Total Power | 100% | 50% | 25% | 0% |
|---|---|---|---|---|
| DDFF | 78.23 | 70.00 | 65.01 | 13.13 |
| Proposed DDFF | 74.03 | 68.13 | 60.00 | 12.65 |

Table IV. Performance of embedded function

| Embedded Function | Leakage Power | Total Power | Delay | PDJ |
|---|---|---|---|---|
| 2 input AND | 54.59nW | 64.81uW | 88.78ns | .0057fJ |
| 2 input OR | 70.81nW | 108.75uW | 82.49ns | .009fJ |
| Mux | 110nW | 185.6uW | 70.06ns | .013fJ |

## 6. CONCLUSION

The results are compared with the existing techniques. The proposed DDFF using sleep transistor approach with NMOS eliminates the leakage power. The overlap period of clock that is required to select proper width has been provided in order to make design simpler. The experiment result shows an improvement in leakage power and delay. The better case of internal data activity has been found out. The input vectors reduces leakage power. The efficiency of DDFF using sleep transistor approach with NMOS has been highlighted using a 4-bit Johnson up and down counter. The speed of the proposed DDFF is same as the existing.

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