International Journal of Reconfigurable and Embedded Systems (IJRES)
Vol. 4, No. 2, July 2015, pp. 129~141
ISSN: 2089-4864

An Integrated Architectural Clock Implemented Memory Design Analysis

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Article Info

Article history:

Received Jan 12, 2015
Revised Mar 28, 2015
Accepted Apr 22, 2015

Keyword:

ASIP
High performance
ISA
Semiconductor devices
Simulators
SRAM simulation

ABSTRACT

Recently Low power custom memory design is the major issue for embedded designer. Micro wind and Xilinx simulator performs efficient cache simulation and high performances with low power consumption. SRAM efficiency analyzed with 6-T architecture design and analyzed the simulation performance for specific application. We have implemented clock based memory architecture design and analyzed internal clock efficiency for SRAM. Architectural clock implemented memory design that reduces access time and propagation delay time for embedded devices. Internal semiconductor material improvement increases simulation performance and these design implemented for application specific design architecture.

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1. INTRODUCTION

Custom architecture design analyzes the behavior of memory used for high performance and low power consumption. Various simulators used for High performance that simulates cache design. We have used some simulators as micro wind, Xilinx. These simulators involved in the designing of memory architecture. Micro wind simulator produces the architectural memory design and simulates an integrated circuit. Micro wind contains a library of common logic and analog ICs to view and simulate logic circuits. Electric extraction of this circuit is automatically performed analog simulation curve immediately. Sense amplifier plays dominant role in SRAM cell used to sense the stored data. Sense amplifiers are used to read the contents of SRAM cells and perform amplification, delay reduction and power reduction. Xilinx simulator used to verifies the functionality and timing of integrated circuit designs. Xilinx simulation process is allowed as to creating and verifying complex circuit's functions.

Recently transistor technology increases the SRAM capability usually 6-12 transistors used for high performance but the cell size gradually increases is major issue. When we reduce the no. of transistors and implemented clock based memory architecture design that reduces the meta-stability and data losses for SRAM. M. Kuldar, K. Fan, M. Chu and S. Mahlke [1] proposed a technique to synthesize the local memory architecture of a clustered accelerator using a phase-ordered approach. P. Merolla, J. Arthur, F. Akopyan, N. Imam, R. Manohar, proposed a technique to synthesize the local memory architecture of a clustered accelerator using a phase-ordered approach. P. Merolla, J. Arthur, F. Akopyan, N. Imam, R. Manohar, D.S. Modha [2] designed fabricated key building block of modular neuromorphic architecture, a neurosynaptic core, with 256 digital integrated, fire neurons and a 1024x256 bit SRAM CROSSBAR memory design architecture. P. R. Panda, N. D. Dutt and A. Nicoulau [3] Proposed scratch-pad memory architecture design

for application specific processor and used optimization technique for customize embedded system. J. Park And P. C. Diniz [4] designed Static RAM and synchronous Dynamic RAM with efficient latency and access modes. The synthesis methods [5] used for FPGAs utilize advanced memory structure, such as “smart buffer”, that require recovery of additional high-level information about loops and array. Sense amplifier [7] design improves the sensing delay and performs excellent tolerance to process variations. Three novel cache models [9] using Multiple-Valued Logic (MVL) to reduces the cache data storage area and cache energy consumption for embedded systems. Spin-transfer torque RAM (STT-RAM) [10] is an emerging nonvolatile memory technology that has low-power and high-density advantages over the SRAM.

2. ARCHITECTURAL SRAM DESIGN

The 6-T Static SRAM contains access transistor. RAM design architecture has implemented with PN diffusion, metal contatness data unit, bit line etc (see figure 1). Micro wind [8] simulator used to design and simulate SRAM design architecture. Theses access transistors are connected to the word line at their specific gate terminals, and the bit line at their source/drain terminals. Word line is used to select the cell while the bit lines are used to perform read/ write operation on the SRAM cell. Memory controller generates the proper signals to verify the specific memory location needs to be accessed, and then having the data show up on the data bus. Internal architecture of Static SRAM (see figure 2) has implemented with semiconductor material. Simulation speed depends upon semiconductor material design and metal contectness (see figure 3). We improve the semiconductor materials for SRAM and analyze its internal clock efficiency. Semiconductor material design improve the SRAM capability and reduces the gap between p-n substrates. The 4 sets of 6-T SRAM design have implemented with silicide (salicide) material and analyze its clock based memory architecture (see figure 4) design. Clock maintain the memory operations so memory can perform scheduled write and read operations.We have implemented CLOCK based sram design with the help of xilinx simulator (see figure 15).

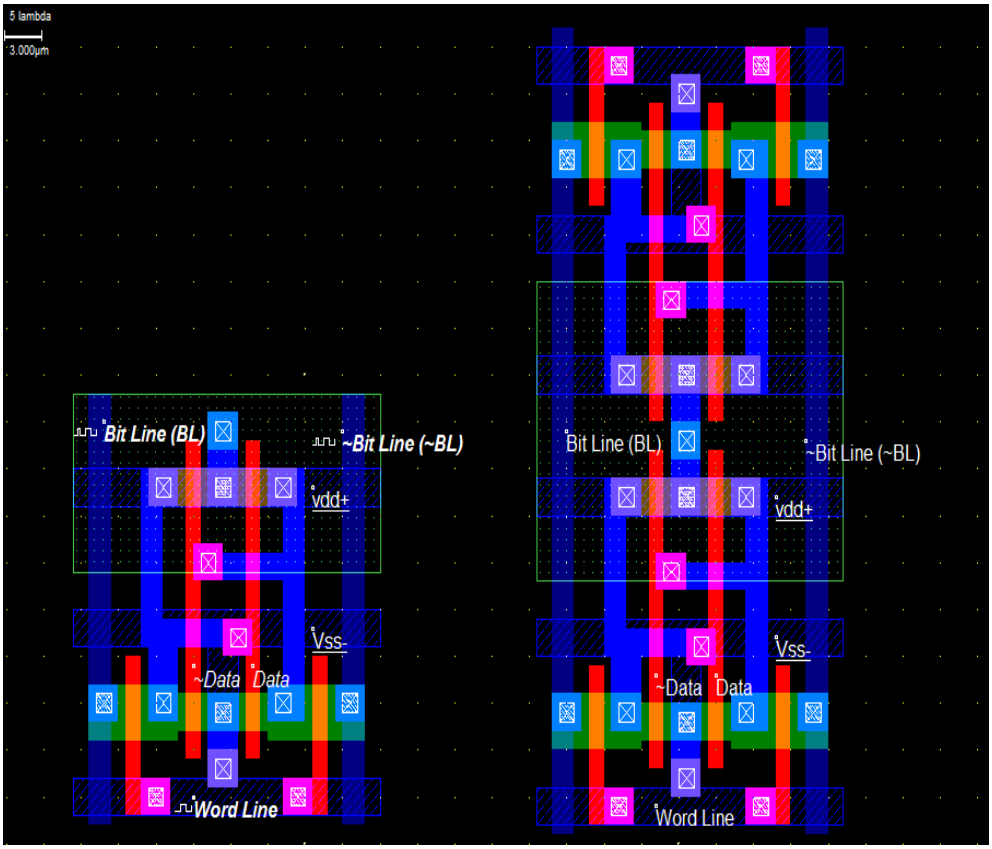

Figure 1. CMOS 6-T SRAM Circuit structure

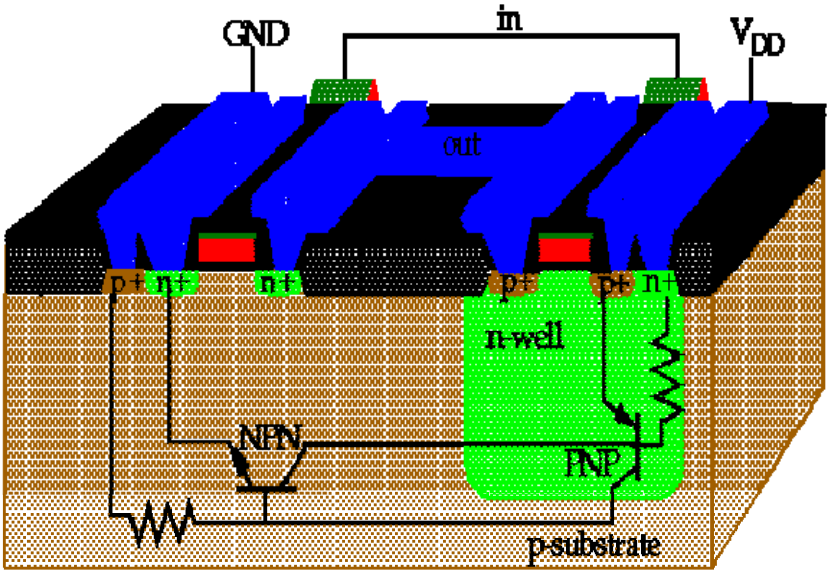

Figure 2. Basic Internal architecture of CMOS SRAM

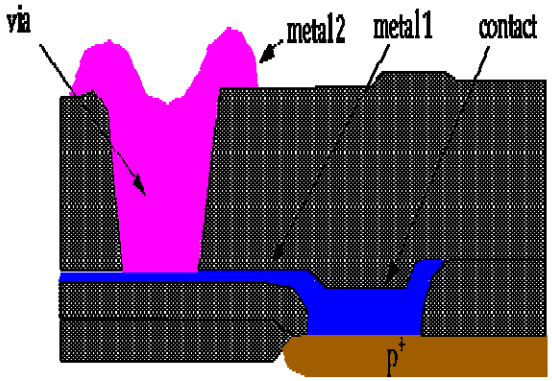

Figure 3. Metal contactetness analysis in SRAM

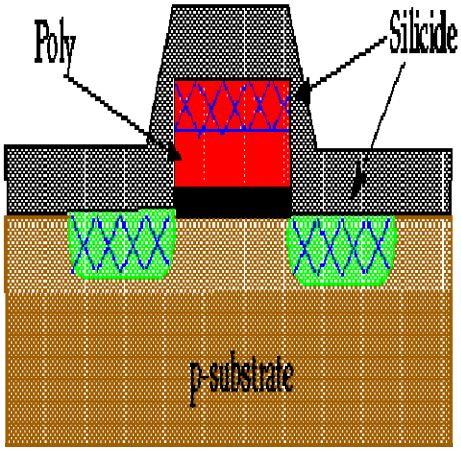

Figure 4. Silicide material in SRAM cell

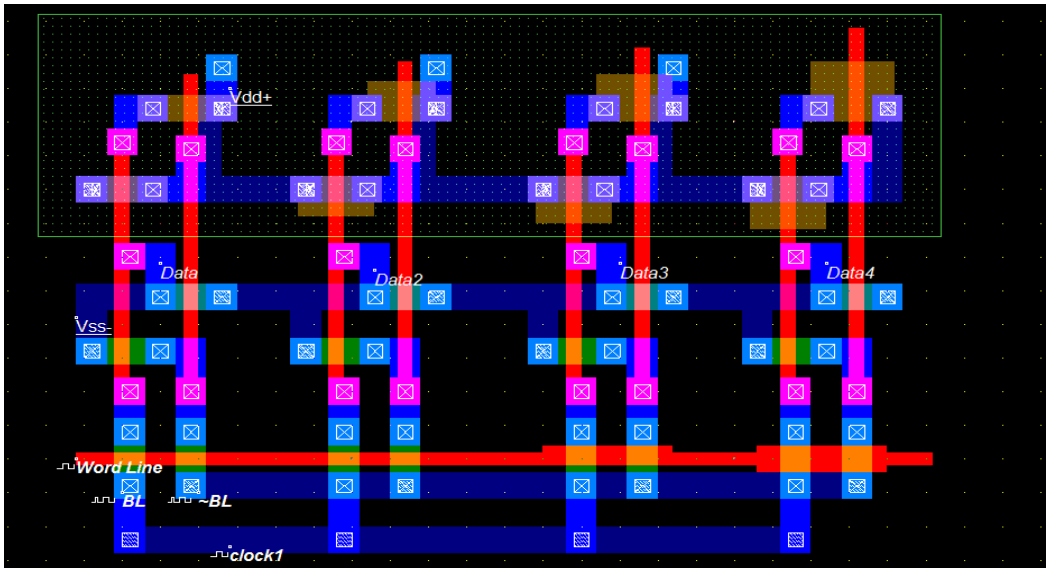

Figure 5. Clock based SRAM design architecture

a. Sense Amplifier

Sense amplifier used to generate low power signals from a bit line that stored in a memory cell, and amplifies with small voltage swing to recognizable logic levels so the data can be easily interpreted. The sense-amplifier circuits (see figure 6) consist of 6 (usually 4) transistors and one sense amplifier used for each column of memory cells, so there are usually thousands or millions of identical sense amplifiers used for performance improvements. We have improved the sense amplifier circuit with silicide to salicide material. These materials improve SRAM capability and increased the simulation performance. Sense amplifier unit contains data unit, sense unit, pre-charge unit etc. Cell internal material improves the simulation performance for specific application and gradually reduces the power consumption.

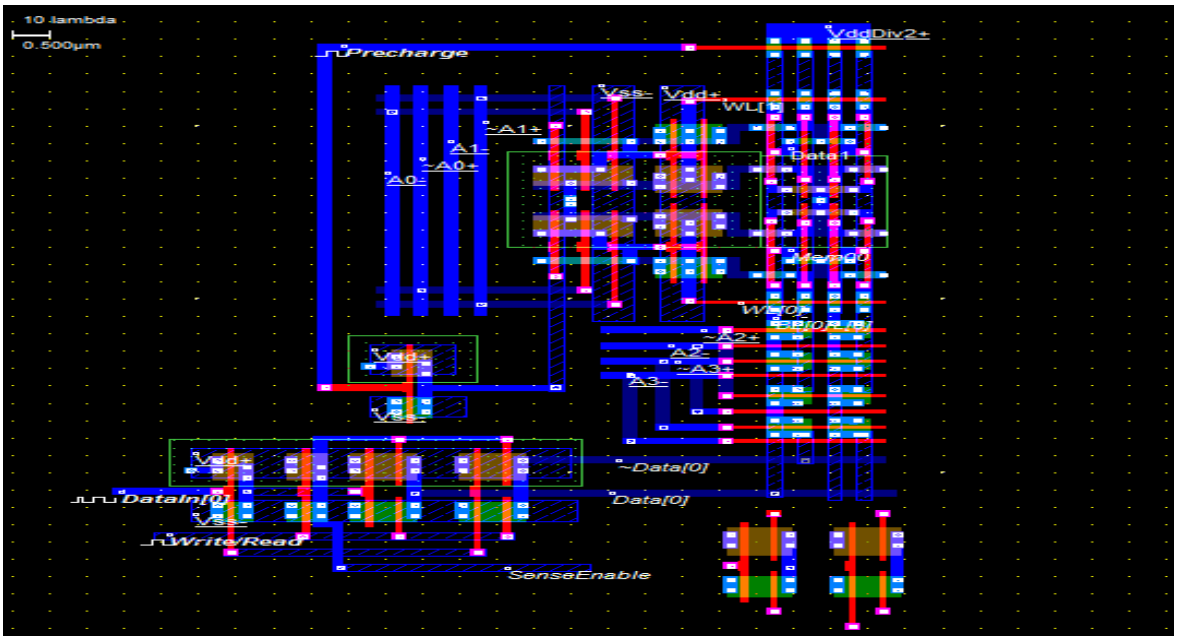

Figure 6. Sense amplifier architetcure design

b. SRAM Cell Analysis for Low Power

The 64-T Static SRAM design implemented with access transistors. 64-T Static SRAM circuits have sense amplifier unit that provides low power signals from a bit line which represents a data bit stored in a sram cell. 64-T implemented with Data IN unit, Data OUT unit, Chip selection unit and sense amplifier circuits (see figure 7). When we have enabled chip and sense amplifier can performs memory operation. We have implemented silicide material quantity then it can gradually reduce the power consumption and performs efficient simulation. Salicide material improves the simulation performance with low power consumption and reduces the gap between pn substrate. We have implemented sram design with clock based memory architecture and analyze its simulation efficiency (see figure 8).

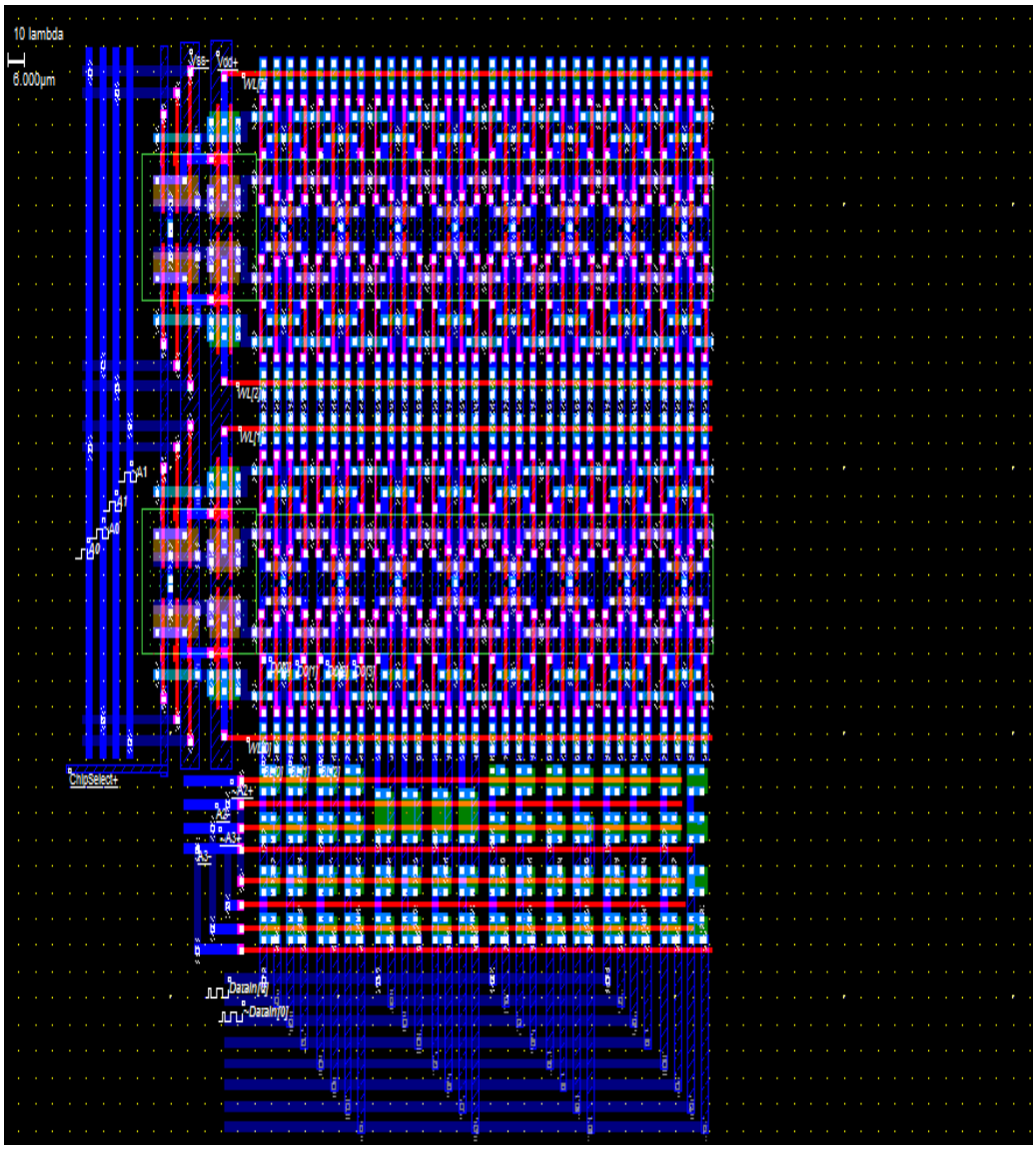

Figure 7. Complex 64-T SRAM cell design

3. CLOCK BASED MEMORY ARCHITECTURE DESIGN

Xilinx [6] simulator provides the interpretation of VHDL or VERILOG code into circuits functionally and performs the logic results of the HDL to determine circuit operations. During the HDL synthesis mechanism, XST analyzes the HDL code and attempts to infer the specific design building blocks. SRAM design implemented with clock based design single clock controlling the write & read operation with the help of inverter (see figure 8) when signal activated then it performs memory operations. When write enabled activated write address is used for input data transfer and clock activated for write operations. When

clock read is activated then it can produce the output data form and performs read operations. These architectural clock based synthesize design implemented with LUTs, mux, and buffer etc (see figure 9 & 10).

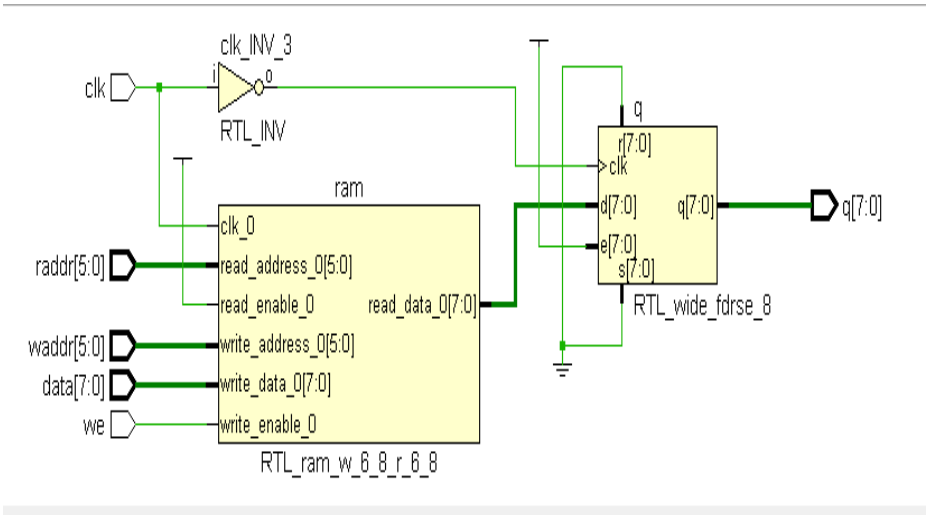

Figure 8. SRAM cell design

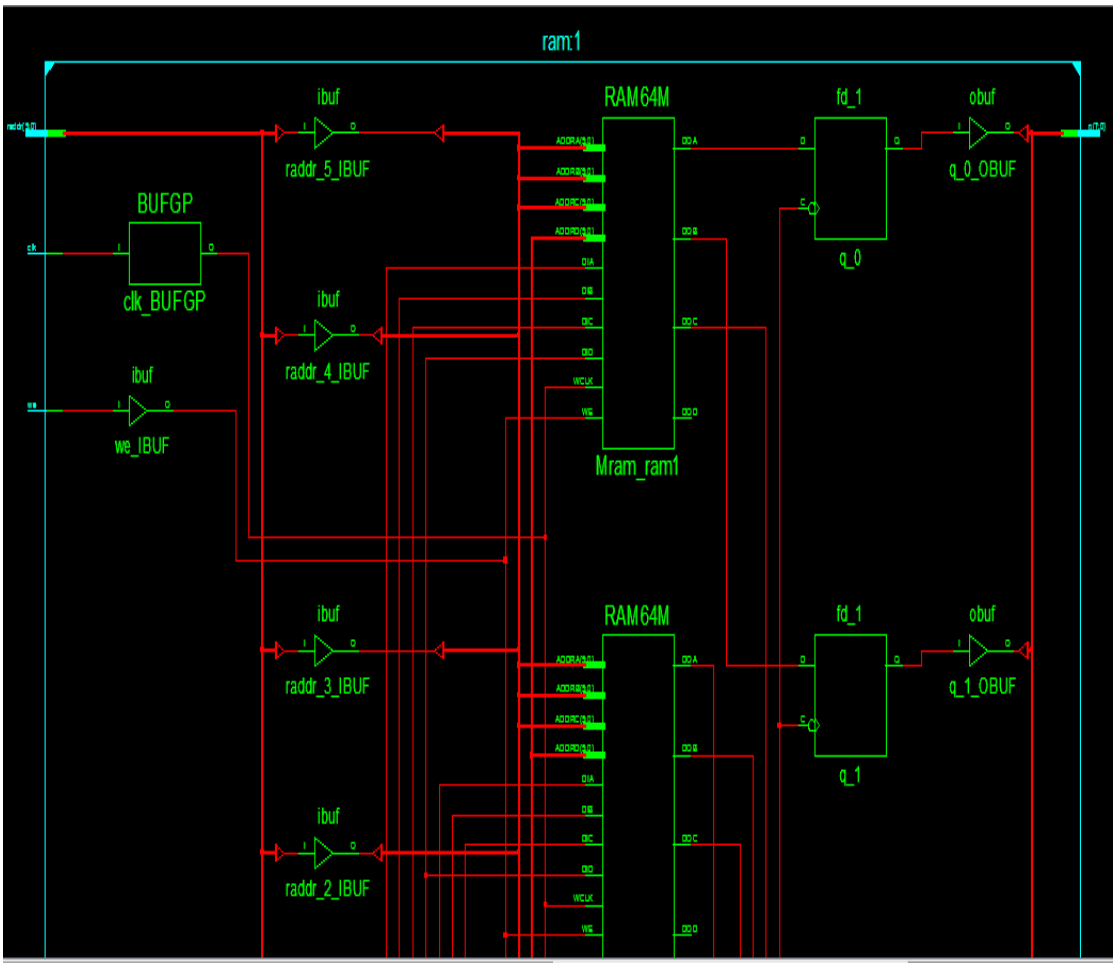

Figure 9. RTL design of SRAM

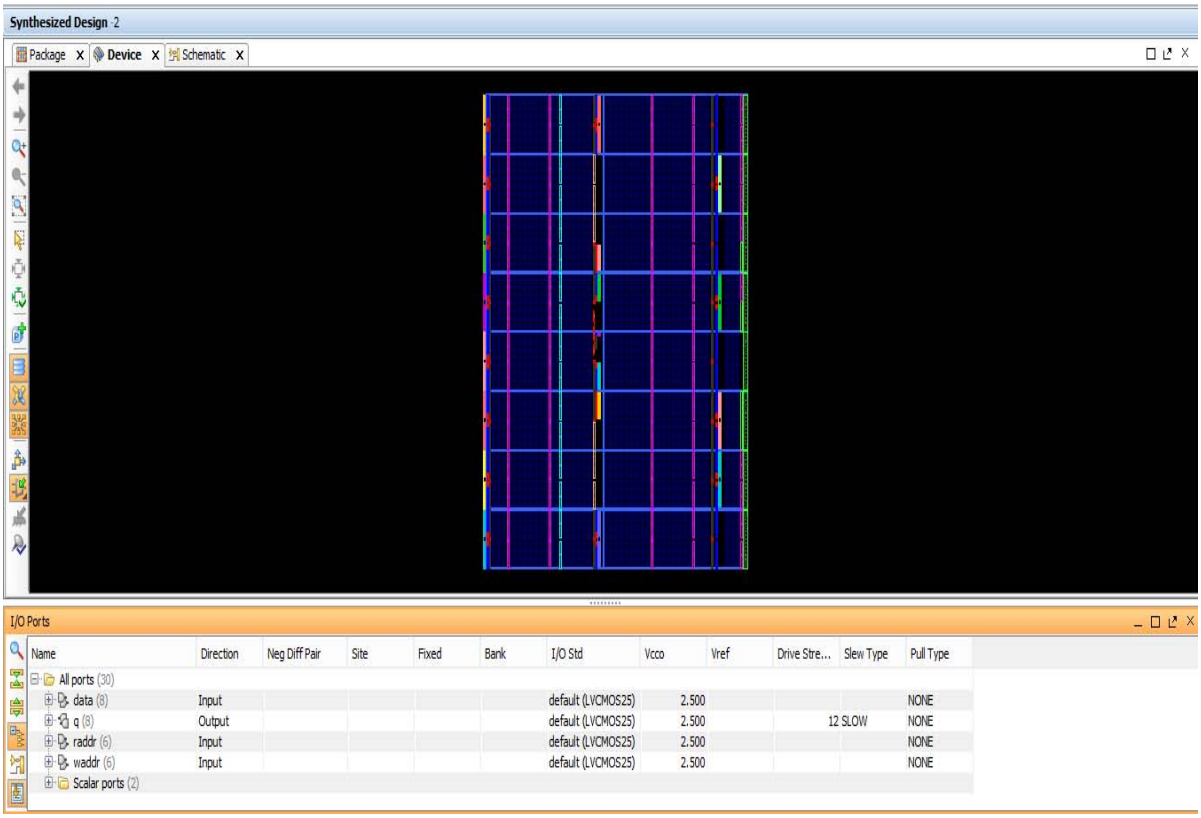

Figure 10. Synthesize design analysis of SRAM

3.1 Dual Clock SRAM Design

Dual clock implemented cache design contains separate read clock and writes clock when signal activated then it can perform memory operations. When write enabled then activated the write address for input data transfer and separate write clock activated for write operations. Another read clock is activated then it can produce the output data and performs read operations. Dual clock Architectural sram design implemented with ffd, buffer etc (see figure 11& 12).

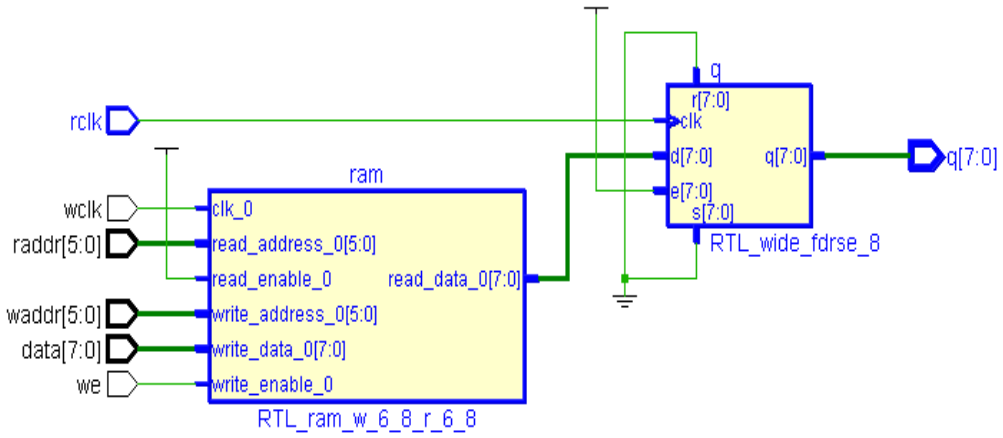

Figure 11. Dual Clock SRAM design

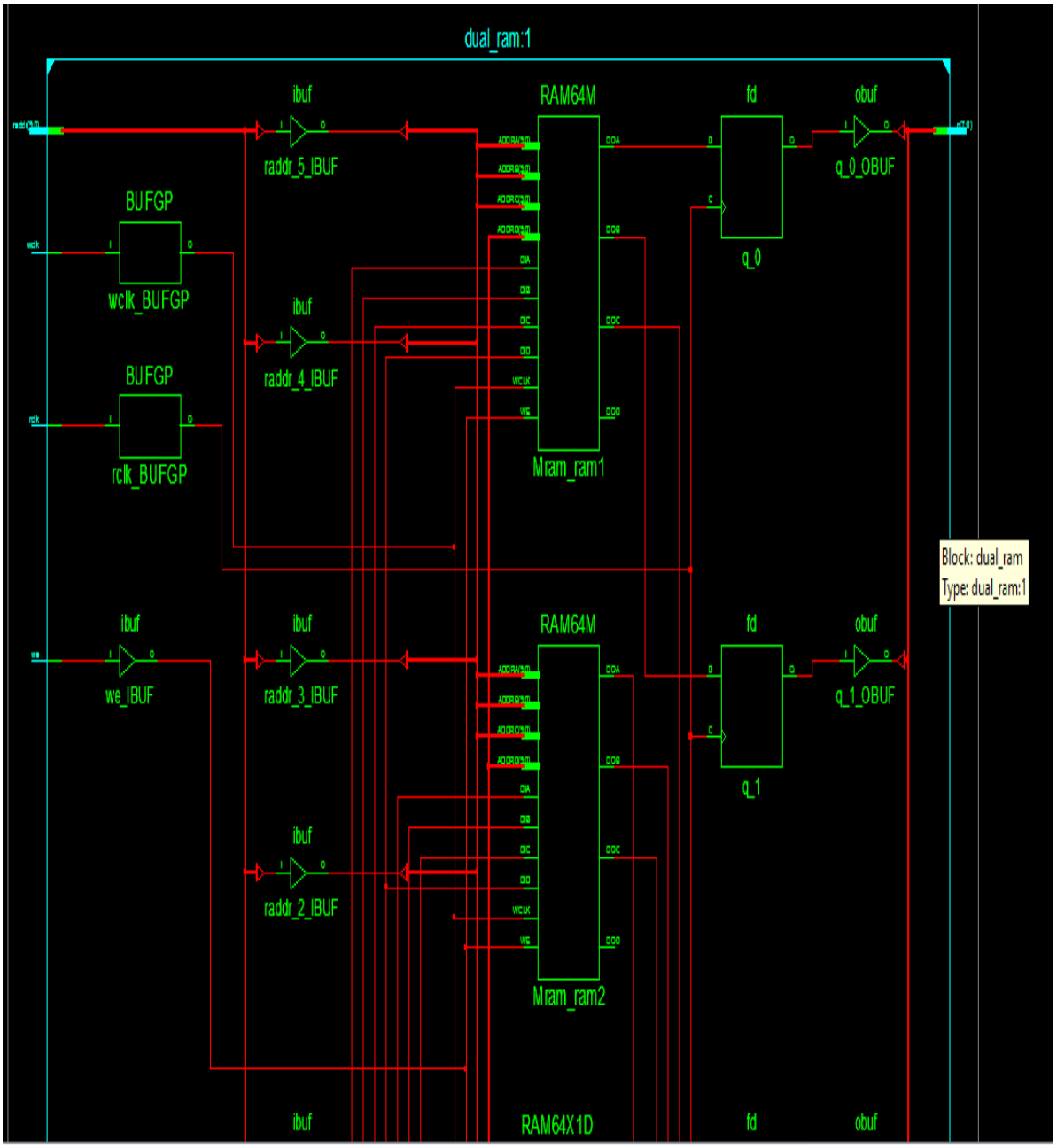

Figure 12. Dual clock SRAM architectural design

3.2 Clock Implemented SRAM Design

We have implemented clocks with subdivision mechanism and used counters which are associated with a stream of ticks that represent time periods. Clock manage read and write operations with help of clock subdivision mechanism. Architectural clock based SRAM design implemented with counters, buffer etc (see figure 13 &14). Clock based counter manage all operation with proper schedule and reduces propagation delay time of SRAMs. Clock implemented SRAM (see figure 15) improve internal clock mechanism that reduces the power consumption and performs scheduled write /read operation so it can reduces the access time and propagation delay time. Single clock SRAM have access time as 1ns and dual clock sram contains simulation access time as 0.8 ns, clock implemented memory architecture mechanism reduces the propagation delay time as 0.2ns in efficient manner (see figure 16&17).

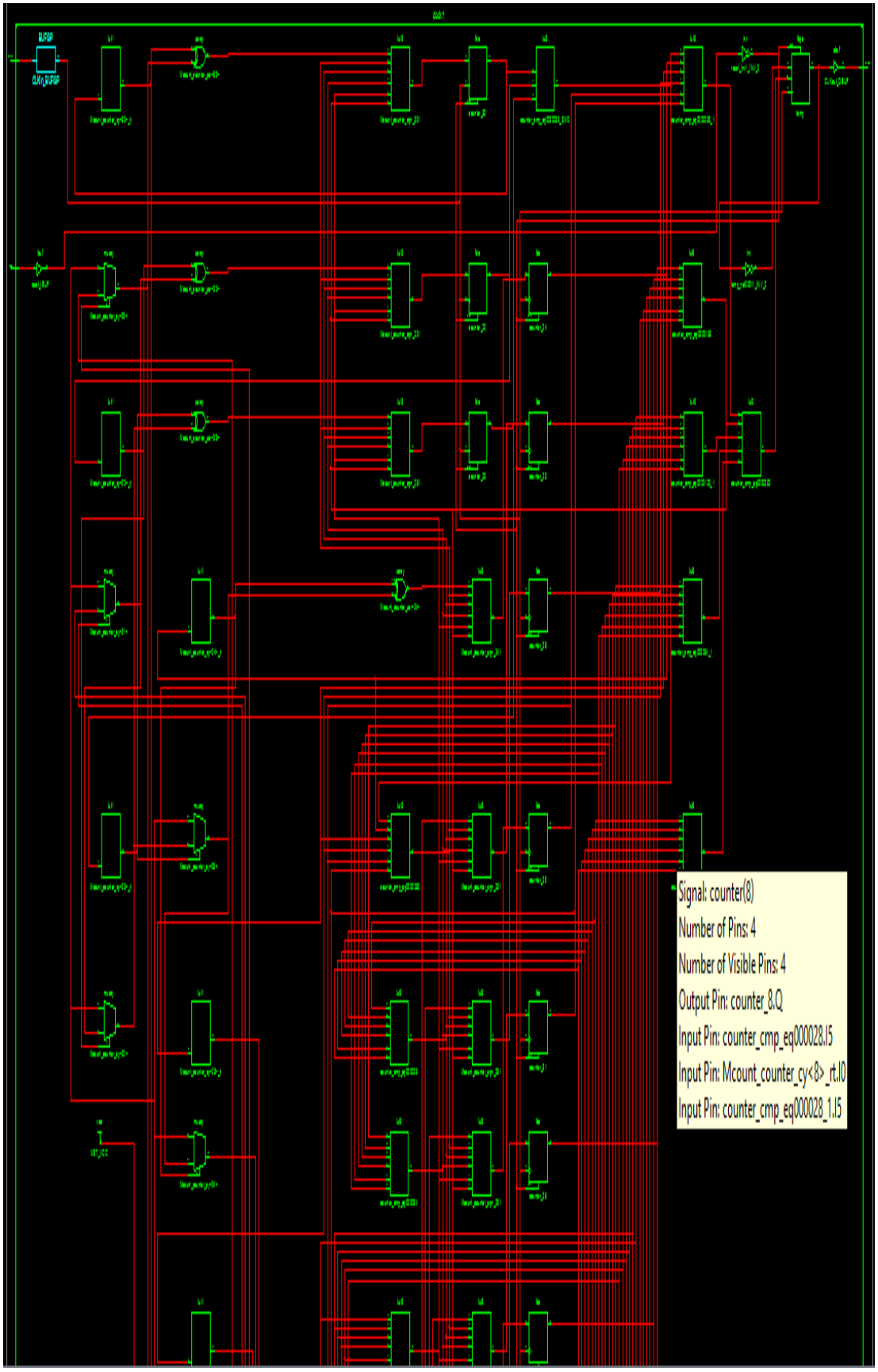

Figure 13. Clocks implementation in SRAM

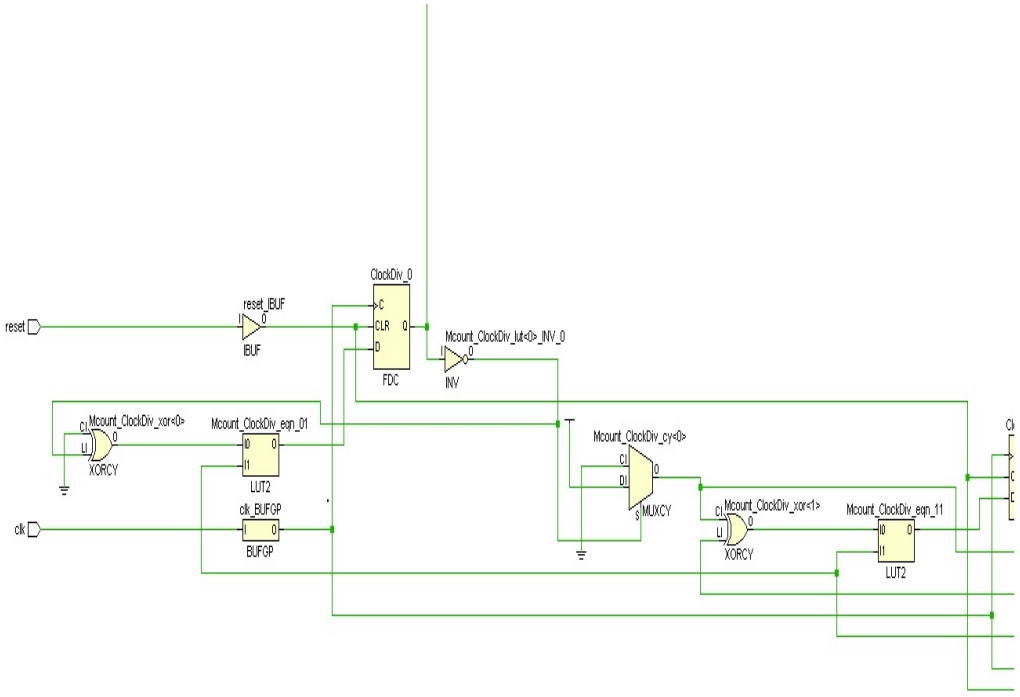

Figure 14. Clock dividend section implementation for SRAM cell

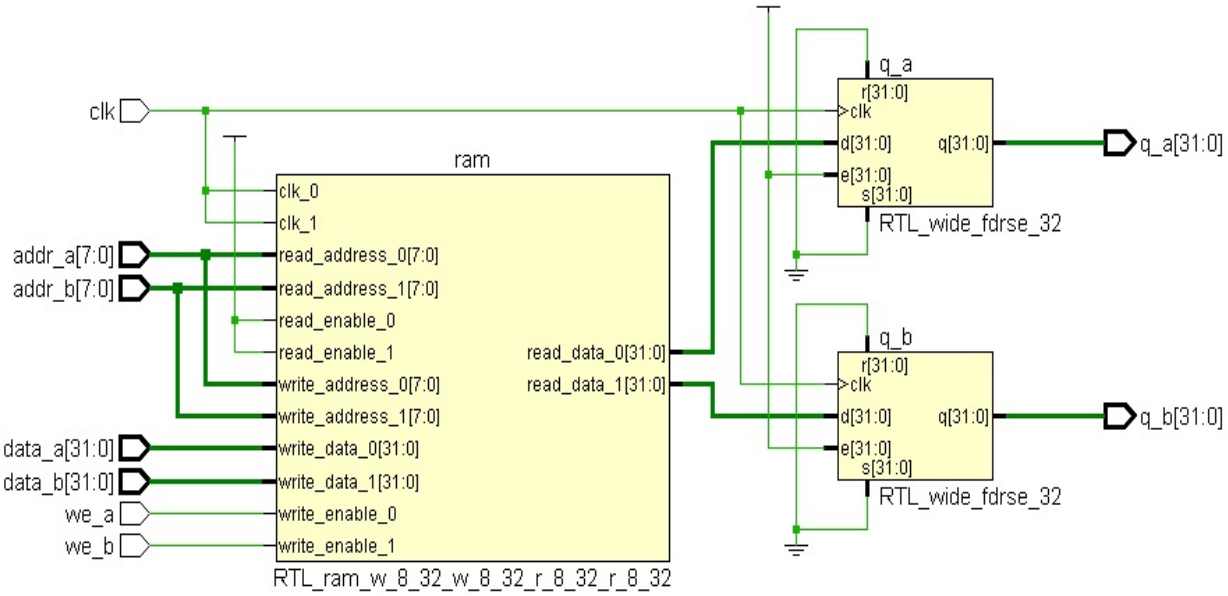

Figure 15. Clock implemented SRAM cell design

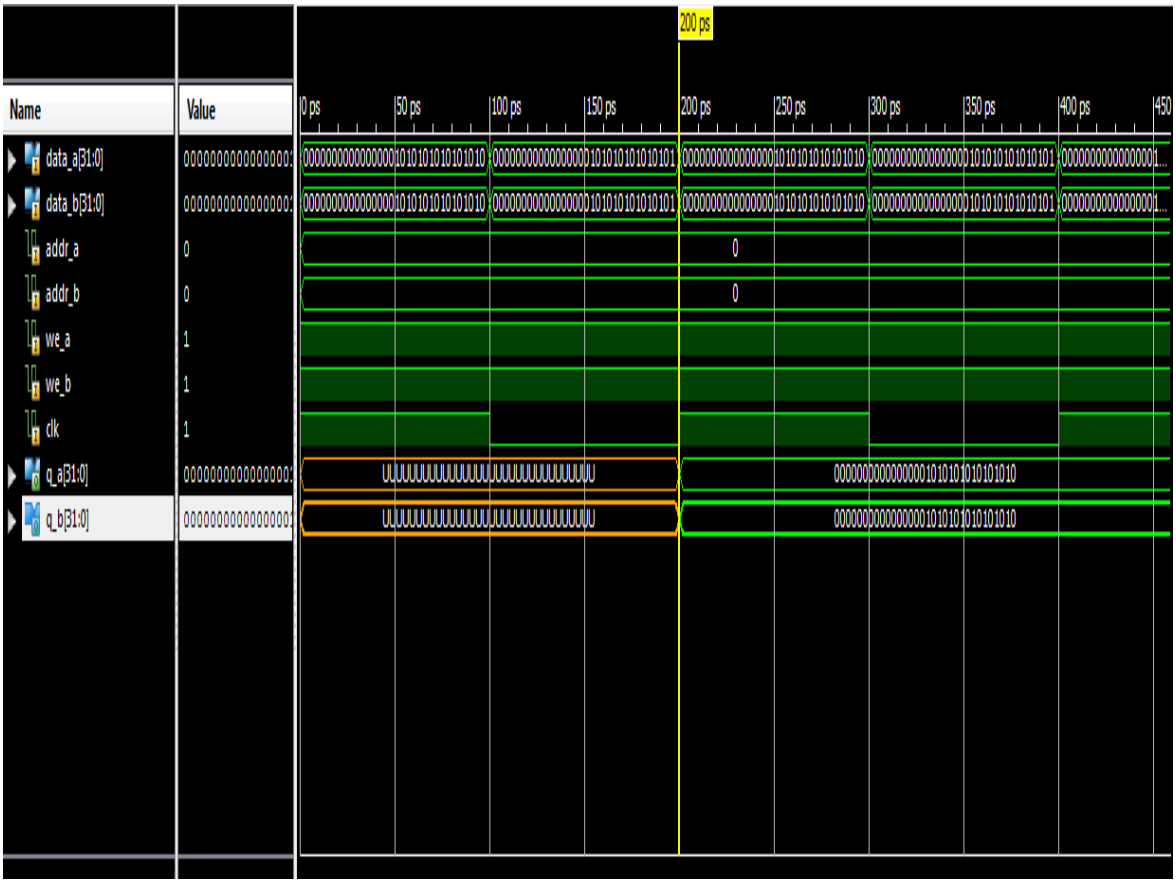

Figure 16. Clock Implemented Memory Simulation

Propagation delay provides the maximum delay between a change in the input and the correct value appearing in the output. Efficient common timing requirement are the setup and hold time which are the minimize duration that the data input to a flip-flops has to be at the desired value appear in before and after the relevant clock edge.

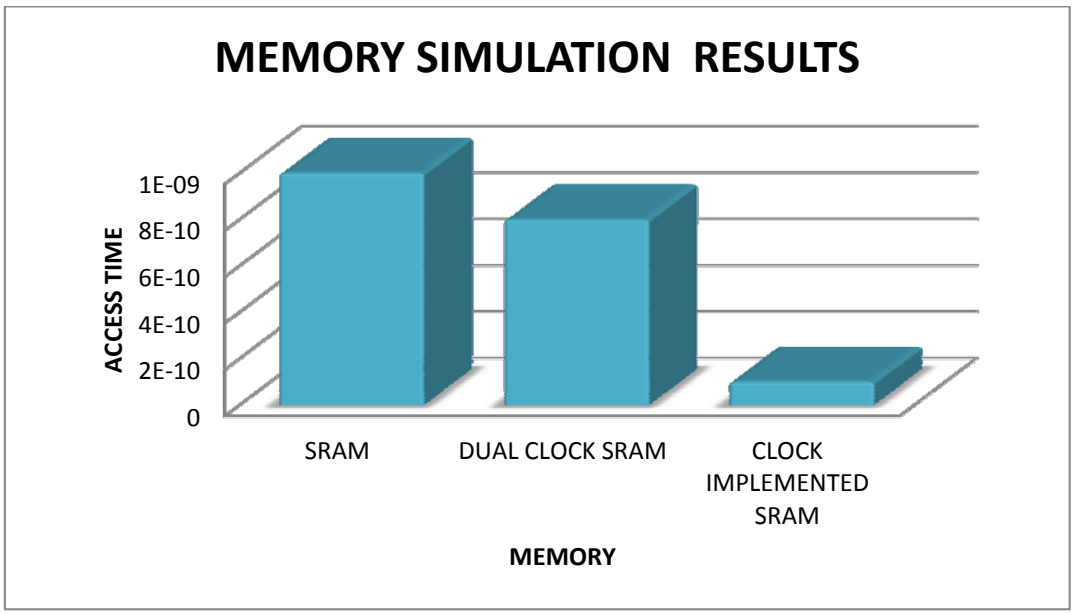

Figure 17. Clock Implemented sram analysis

4. APPLICATION SPECIFIC ARCHITECTURAL MEMORY SIMULATION

We have implemented efficient Memory architectural design according to specific application. We have used standard Dhrystone application on target hardware environment and analyzed the ISA simulation behaviour (see figure 18) with integrate efficient clock implemented memory architecture design. During these simulations processes we have analyzed the ISA result for specific application with XUP-5 FPGA hardware platform. Clock implemented memory design analyzed for various ASIP simulation process and low power consumption design architecture.

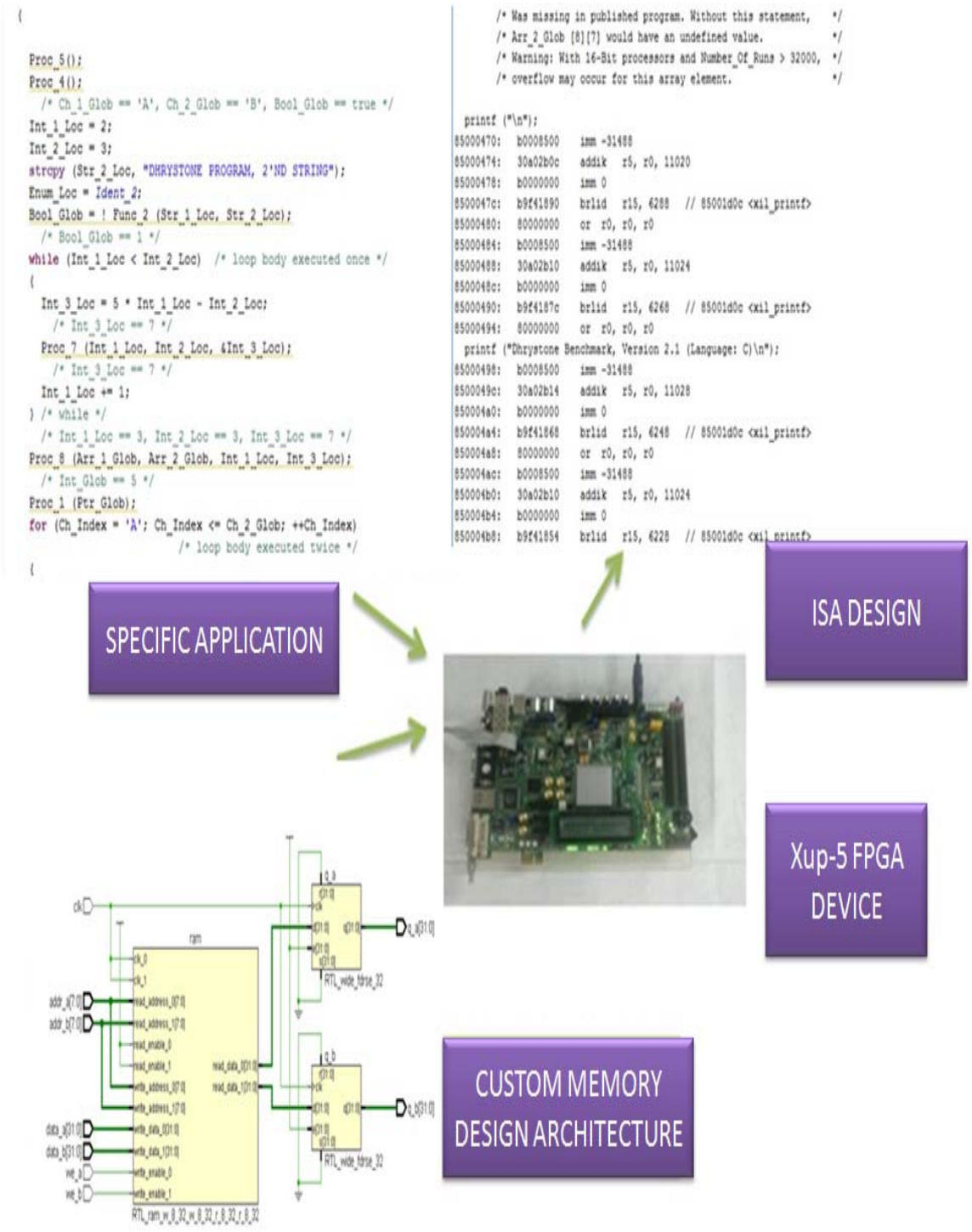

Figure 18. Clock implemented application specific architectural memory design simulation

5. CONCLUSION

Custom Cache architecture behaviour & its efficiency analyzed with various simulators. Our main focus in this paper is to analyze the simulation effciency of SRAM and analyzed internal clock based architecture behaviour. Application specific memory architecture design reduces the propagation delay time as well as increases the system performances. Semiconductor material implemented SRAM design also reduces access time and improve the simulation performance.After doing these simulation we can get efficient simulation results and its effective innovation for low power embedded wireless devices Clock implemented architecture memory design contains clock subdivision mechanism and its implementes for recently low power consumption and high perfromance medical devices.

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