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FPGA Based Multichannel Bit Error Rate Tester for Spacecraft Data Acquisition System

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ABSTRACT

Bit Error Rate (BER) is a principle measure of data transmission link performance. BER tester (BERT) consists of a Pattern Generator and an Analyzer that can be set to the same pattern. The payload data transmitted from the spacecraft consists of one, two or three channels per carrier based on the modulation scheme. The traditional equipments can do BER analysis for only one channel at a time. In order to support multichannel BER analysis, a Personal Computer (PC) based system is designed and implemented in Altera Stratix II (EP2S130F1508C5N) FPGA. Ethernet is configured using WIZnet 5300 (Ethernet Controller) and it is used for communication between FPGA and PC with an application. Application is used to transmit the Pattern Generator's configurations from PC to FPGA and to receive Analyzer's status. Packet processing is done for this communication using User Datagram protocol (UDP). On the whole, traditional equipments are replaced by the designed and implemented bit error rate tester.

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1. INTRODUCTION

Bit error rate (BER) of a transmission link is calculated as follows.
BER = No of bit errors/ Total no of bits received
Example:
No of bit errors = 1
Total no of bits transmitted = 10^6
BER = 1×10^{-6}

In a noisy channel, BER is expressed as a function of normalized carrier-to-noise measure denoted by Eb/N0, (energy per bit to noise power spectral density ratio). BER curves are plotted to describe the functionality of a digital communication system. In digital communication, BER vs. Received Power (dBm) is usually used; while in wireless communication, BER vs. SNR (dB) is used [4]. Such a plot is shown in Figure 1.

1.1. Bit Error Rate Tester (BERT)

BERTs use predetermined data patterns consisting of a sequence of logical ones and zeros generated by a test pattern generator to test digital communication circuits. Generator and Analyzer can be used in pairs, with one at either end of a transmission link, or singularly at one end with a loopback at the remote end. Common types of BERT patterns are pseudorandom binary sequence (PRBS), Quasi Random Signal Source (QRSS), Bridgetap, Multipat etc. In this project PRBS is used [2] [3].

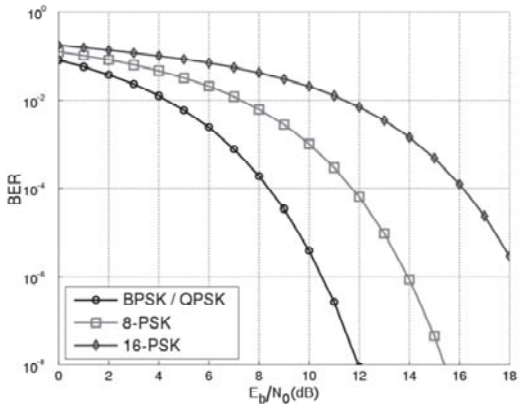


Figure 1. Bit-error rate curves for BPSK, QPSK, 8-PSK and 16-PSK, AWGN channel

1.2. PRBS Pattern Generator

Pseudorandom Binary Sequence Pattern Generator is used for the data generation. Linear Feedback Shift Registers (LFSR) are used to create this pattern. Various international standards [1] are used to create this pattern as shown in table 1.

Table 1. PN Sequences

n	Label	Polynomial	Reference Standard	Taps	Sequence Length (2^n – 1 bits)
7	PN7	x^7+x^6+1	Not Standard	6,7	127
15	PN15	$x^{15}+x^{14}+1$	ITU-T O.150	14,15	32767
17	PN17	$x^{17}+x^{14}+1$	OIF-CEI-P-02.0	14,17	131071
20	PN20	$x^{20}+x^3+1$	ITU-T O.150	3,20	1048575
23	PN23	$x^{23}+x^{18}+1$	ITU-T O.150	18,23	8388607

1.3 PN7 Sequence

The data for PN7 is generated by doing XOR operation of 6th and 7th bits and the XOR output is fed back to the 1st bit [1] which is shown in figure 2.

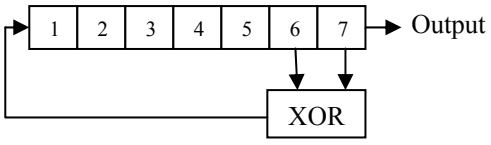


Figure 2. PN7 Sequence

The seed word and the data for PN7 is as follows.
PN7 Seed word = 1111111
PN7 data = 1111 1110 0000 0100 0001 1000 0111 .... (binary)
F E 0 4 1 8 7 … (hex)
Similarly for other Pseudorandom Number (PN) sequences, the data can be generated.

2. RESEARCH METHOD

2.1. Block Diagram

For generator, the inputs are from the PC with application. For three channels namely CH1, CH2 and CH3, the various input configuration parameters are clock, reset, PN selection (PN7, PN15, PN17, PN20 and PN23), error rate injection and manual error. The output of generator is clock and the PRBS data. The outputs are available in the LVDS O/P interface. For analyzer, the inputs are clock and PRBS data of the three channels. The outputs are clock presence, BER lock, PN detected, no of bits elapsed during lock, no of bits elapsed during unlock for each channel. The PCI-X card consists of Altera Stratix II (EP2S130F1508C5N) FPGA, WIZnet 5300 (Ethernet Controller), LAN Port, LVDS I/O interfaces. A PC with a GUI is connected to the PCI-X Card through LAN port. The block diagram is shown in figure 3.

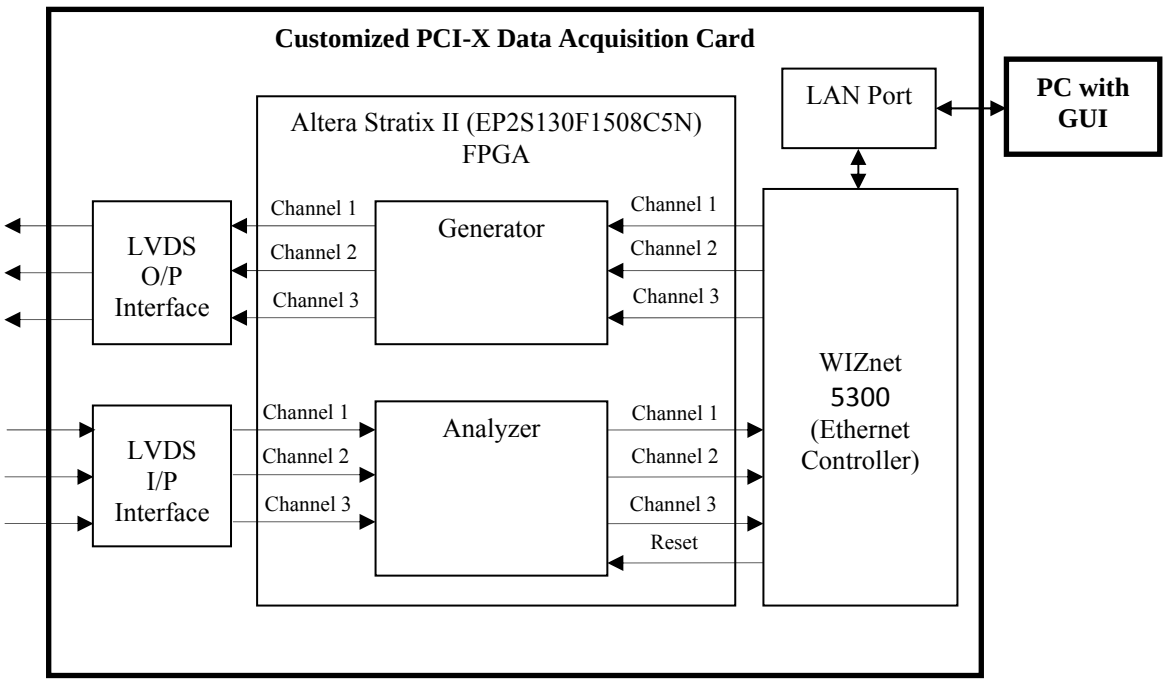


Figure 3. Block Diagram

2.2. Hardware

2.2.1. Customized PCI-X Card

Peripheral Component Interconnect eXtended (PCI-X) is a 64 bit computer bus and expansion card standard that enhances the 32-bit PCI Local Bus for higher bandwidth demanded by servers. The customized card (64 bit/ 100 MHz) is of the type as shown in figure 4. 94 pins are there in the card.

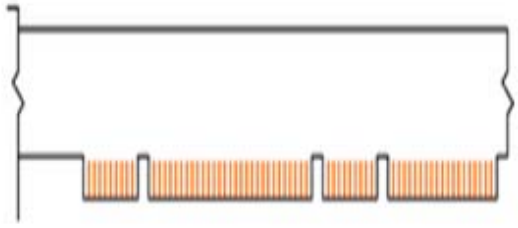


Figure 4. Universal (3.3V & 5V) 64-bit PCI Card

Table 2. Features

Features	Quantity
Adaptive logic modules (ALMs)	53,016
Adaptive look-up tables (ALUTs)	106,032
Equivalent logic elements	132,540
M512 RAM blocks	699
M4K RAM blocks	609
M-RAM blocks	6
Total RAM bits	6,747,840
DSP blocks	63
18-bit × 18-bit multipliers	252
Enhanced PLLs	4
Fast PLLs	8
Total pins	1,126

2.2.2. Altera Stratix II (EP2S130F1508C5N) FPGA

The clock frequency of this FPGA is 640 MHz. The features are shown in the Table 2 [5].

2.2.3. WIZnet 5300 (Ethernet Controller)

In this Ethernet controller memory is extended to 128Kbyte and 16 bit bus interface is supported. It consists of eight hardware sockets which can be used simultaneously. In this project only one is used. Communication can be established using Protocols such as Transmission Control Protocol (TCP), User Datagram Protocol (UDP), IPRAW and MACRAW. TCP is a connection-oriented protocol. UDP is a connection-less protocol. UDP supports unicast, broadcast and multicast methods. In this project UDP (unicast method) is used [6]. Socket status transition for UDP (Unicast method) and UDP operation flow are shown in figure 5 and 6 respectively.

Direct addressing mode is implemented. For 16bit data bus width, ADDR [9:1] is used and ADDR0 is connected to ground or floated. 'BIT16EN' is internally pulled-up, so it is no problem if it is allowed to float. The connections are shown in figure 7.

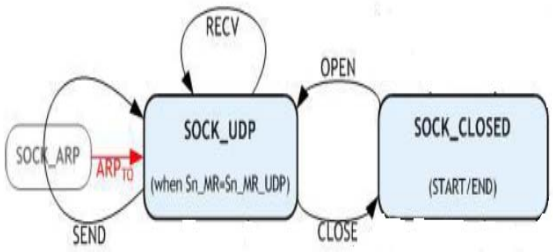


Figure 5. Socket Status Transition for UDP Protocol (Unicast method)

Table 3. Error Rate Injection

Rate Selection	BER
2	$1x10^{-2}$
3	$1x10^{-3}$
4	$1x10^{-4}$
5	$1x10^{-5}$
6	$1x10^{-6}$
7	$1x10^{-7}$

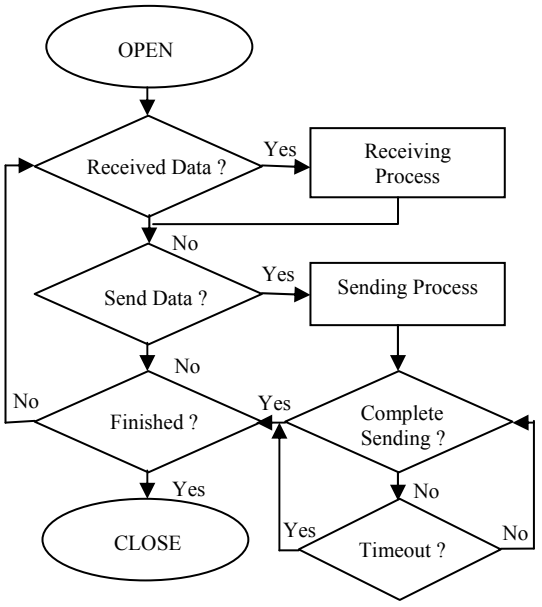


Figure 6. UDP Operation flow

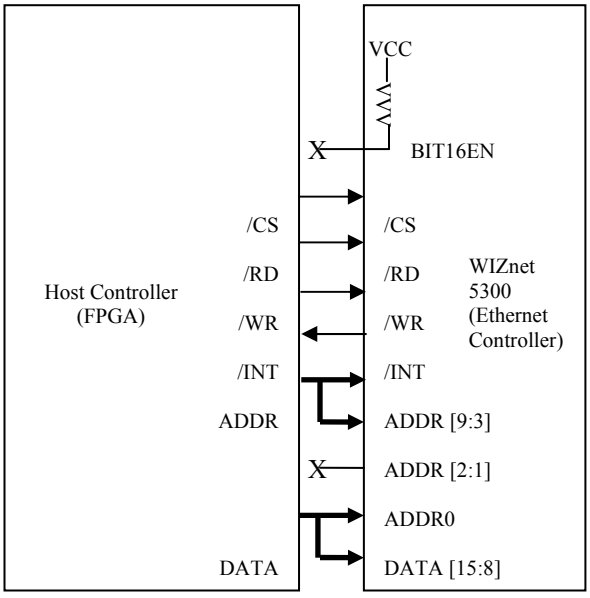


Figure 7. Direct Address Mode with 16 bit data bus width

2.3. Software

Altera Quartus II 13.0 is used for FPGA programming [7]. Verilog coding is done for this project. Microsoft Visual Basic (VB) is used for Graphical User Interface (GUI). Packet processing is done in VB. 010 Editor is used to convert bytes of data into characters in order to transmit the data from PC to FPGA in VB based GUI. Wireshark (Network Protocol Analyzer) is used to analyze the data transmitted and received

with information such as IP addresses of the sender and receiver, number of bytes, communication protocol used, etc.

2.4. Verilog Programming

For the three channels, clock, reset, PN type selection, the error rate injection, manual error injection are taken care in the programming. The error rate injection is mentioned in table 3. In order to analyze the serial input of the analyzer, an algorithm is used and the same is used in verilog programming. Flow chart of the algorithm is shown in the figure 8.

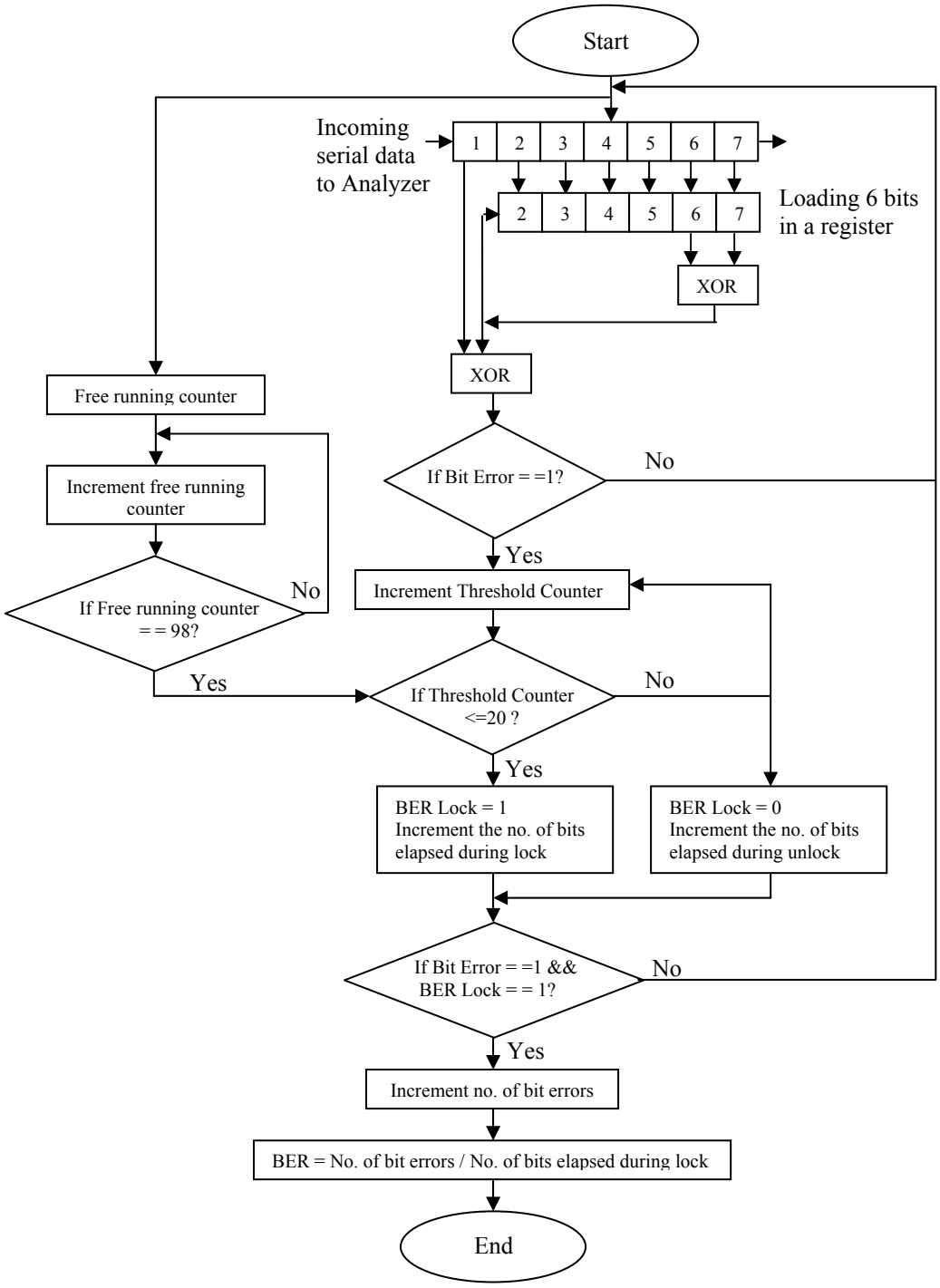
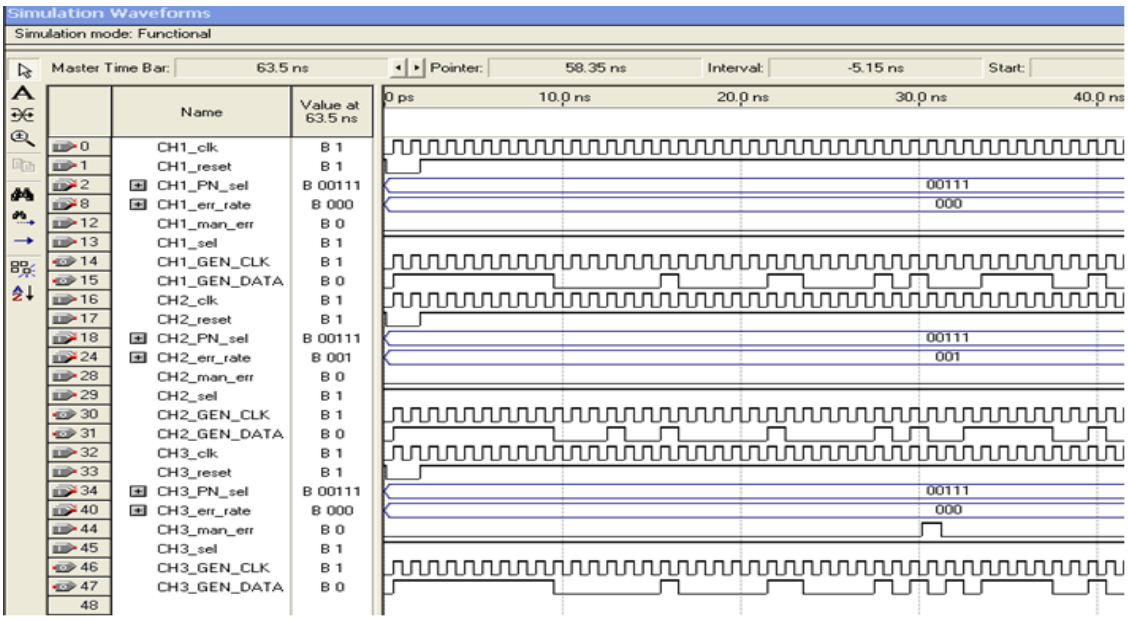


Figure 8. PN7 Data Analyzer Flow Chart

3. RESULTS AND ANALYSIS

The simulation result of three channel PRBS generator is shown in Figure 9.



CH1_GEN_DATA - PN7 data without error
CH2_GEN_DATA - PN7 data with 10^{1} error rate injection
CH3_GEN_DATA - PN7 data with manual error

Figure 9. PRBS Generator Simulation Result

3.1. Packet Processing and Implementation in Altera Stratix II (EP2S130F1508C5N) FPGA

The data packet sent from PC to FPGA is of 14 bytes. But along with the UDP data format it is of 22 bytes (4 bytes-Destination IP address, 2 bytes-Destination port number, 2 bytes-Byte size of the data packet and 14 bytes-data packet). The UDP data format is shown in figure 10. The data received from FPGA to PC is of 72 bytes comprising of all the three channels information such as no. of bit errors, no. of bits elapsed during lock, no. of bits elapsed during unlock, etc. The received data packets are shown in figure 11. The PC based application used for this project is shown in figure 12.

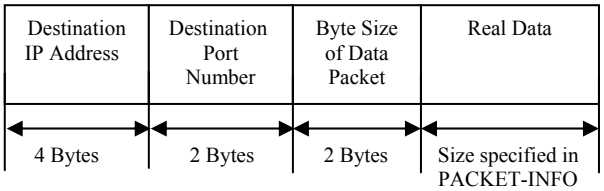


Figure 10. UDP data format

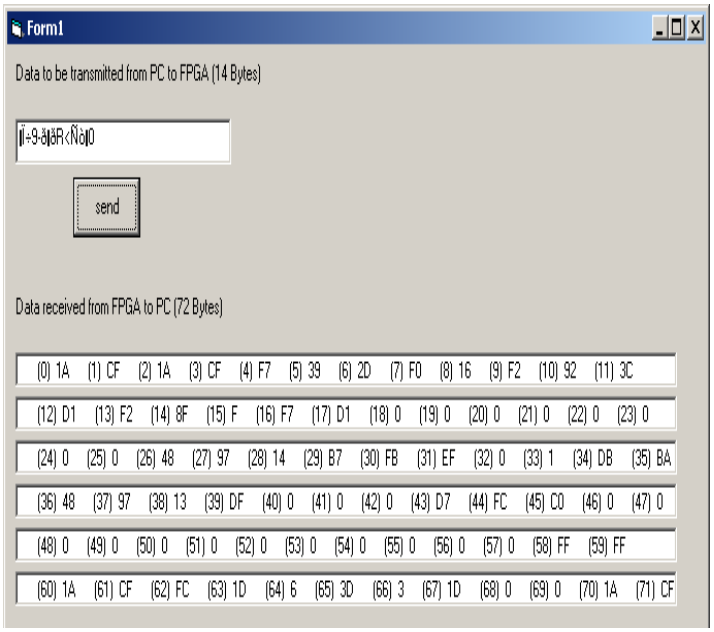


Figure 11. GUI used for packet display

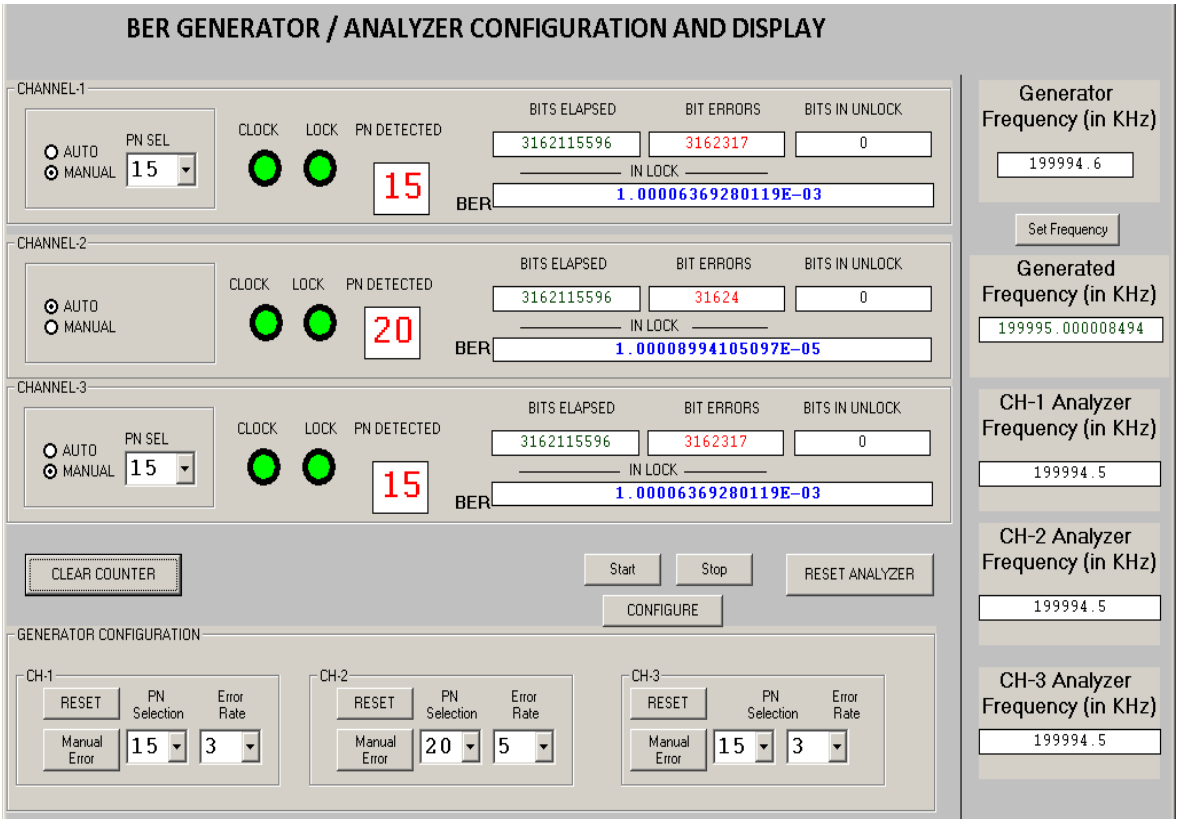


Figure 12. BER Tester GUI

3.2. Testing with Tektronix GigaBERT™ 700 Generator and ANALYZER

The designed and implemented BERT is tested with the standard equipments and it is found that the designed BERT results and the standard equipments results are matching. The setup is shown in figure 13 and Figure 14.

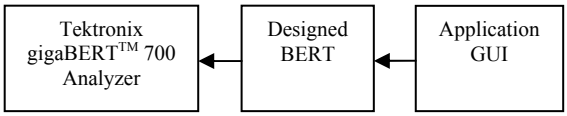


Figure 13. Testing designed Generator with Tektronix gigaBERT™ 700 Analyzer

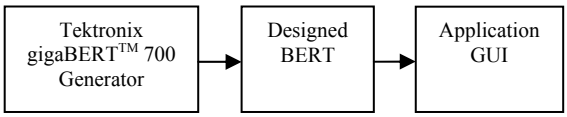


Figure 14. Testing designed Analyzer with Tektronix gigaBERT™ 700 Generator

4. CONCLUSION

A custom BER tester is designed and implemented to characterize and validate a transmission link. The hardware platforms are the customized PCI-X card consisting of Altera Stratix II (EP2S130F1508C5N) FPGA, WIZnet 5300 (Ethernet Controller), LAN port and LVDS interfaces. The system operates upto 200 MHz. User interface is implemented for data acquisition and test analysis. UDP transmission protocol is experimented. These experience show the benefits of FPGA based BER tester in system prototyping and customization.

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