International Journal of Reconfigurable and Embedded Systems (IJRES)
Vol. 3, No. 2, July 2014, pp. 62~75
ISSN: 2089-4864

Design and Development of ARM9 Evaluation Kit for Embedded Applications

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Article Info

Article history:

Received Mar 4, 2014
Revised May 11, 2014
Accepted Jun 2, 2014

Keyword:

ARM9
CADSTAR
Evaluation kit
OrCAD
PCB
SDRAM

ABSTRACT

In contrast with low end microprocessor, ARM9 core is quite a sophisticated processor. The Evaluation kit plays an important role in the prototype development and verification of the system design before taking to its actual system development hence it's provide better confidence to the designer. In this paper a project for the Evaluation kit has been designed for embedded system engineer to implement and confirm the functionality of their operating systems which could lead to a comfortable deployment. The independent modules for the interfaces of the ARM9 processor have been designed and the schematics have been developed using OrCAD. From the tested schematics designed in OrCAD, the related PCB is designed using CADSTAR. An eight-layer board is designed for its signal integrity and complexity of the schematic designed. The designed PCB layer is then calibrated and Gerber files are then made and passed on the PCB board manufacturer for PCB fabrication. The PCB board made is then tested for interconnection continuity using multi-meter as the components are loaded on to the board.

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1. INTRODUCTION

Over the past few decades, embedded systems have become increasingly common in everyday life. Television remotes, alarm clocks, cars and mobile phones contain just a minute handful of the embedded systems people encounter daily. Embedded systems are often required to perform tasks within a bounded time frame. For a simple device such as a remote control, this is not a particularly demanding requirement. However, for devices that are required to process large volumes of data, much more attention needs to be given to performance.

The ARM9 Evaluation Kit is a complete system-on-chip built around the ARM9 Thumb processor. It incorporates a rich set of system and application peripherals and standard interfaces in order to provide a single-chip driven solution for a wide range of compute-intensive applications that require maximum functionality at minimum power consumption at lowest cost. Atmel Corporation had announced the AT91SAM9260, the first member of a pin-compatible ARM9-based microcontroller family that shares the same programming model as ARM7-based controllers, allowing direct migration between controllers based on different ARM cores. The AT91SAM9260 also supports deterministic, real-time operation, offers supervisory functions, and has third-party RTOS support comparable to those of 8-bit controllers. Developed for highly-connected image-processing applications such as point-of-sale terminals, Ethernet-based IP

cameras, and bar code readers, the AT91SAM9260 integrates a 200 MIPS ARM926EJ-S core with: a camera interface; seven USARTs; 10/100 Ethernet MAC; 12 Mbps USB device and host controller with on-chip transceivers; external bus interface supporting SDRAM, Flash, NAND Flash with built-in ECC, SD, SDIO, and Multimedia Card interface (MMC); three synchronous serial controllers (SSC); two master/slave Serial Peripheral Interfaces (SPI); a three-channel 16-bit timer/counter; two-wire interface (TWI); and IEEE 1149.1 JTAG Boundary Scan on all digital pins as shown in Figure 1.

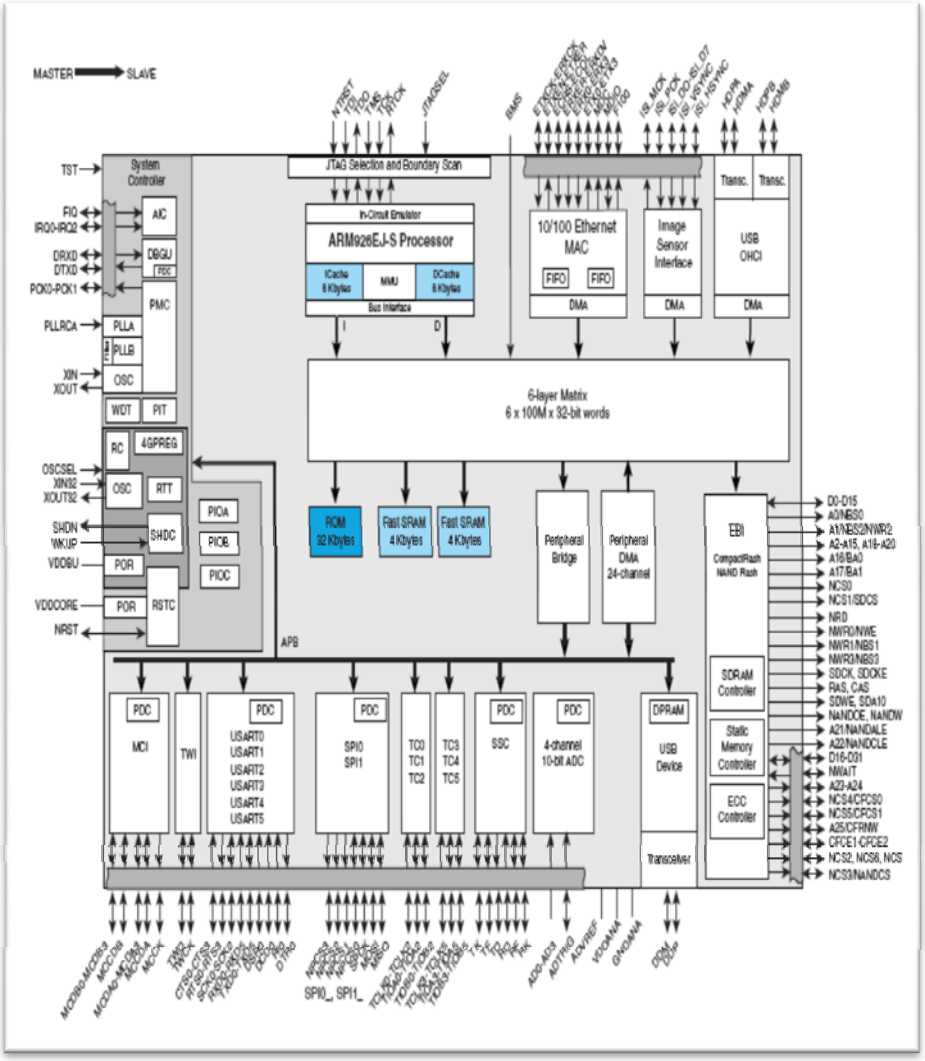

Figure 1. Block Diagram of AT91SAM9260 [1]

The internal bus bandwidth of the AT91SAM9260 is maximized by 24 DMA channels and a five-layer high-speed bus matrix. It connects all masters and slaves in the system in a parallel fashion and enables data transfers between peripherals and on- and off-chip memories without any CPU intervention. A programmable arbiter manages the priorities between the bus masters. Highly critical interrupt routines can be locked in the 16 kByte instruction cache, guaranteeing a deterministic response time to interrupts. A system controller provides a full complement of supervisory functions that includes an 8-level priority interrupt controller, RC-oscillator, PLLs, real-time periodic interval and watchdog timers, reset and shutdown controllers, and backup registers. The shutdown controller puts the processor in an ultra-low power mode, typically less than 10 uA. Atmel's SAM9 microcontrollers are the first ARM9-based microcontrollers with Flash memory integrated on the same chip. The AT91SAM9260 has third-party RTOS support from Green Hills Software, Mentor Graphics and Micrium. Compiler/debuggers are available from Green Hills Software,

ARM, Keil, IAR Systems and any compliant ARM926EJ-S compiler. Windows CE and Linux operating system support is also provided.

The Evaluation kit enables real time code development and evaluation. It supports the AT91SAM9260 Arm9 Based 32 bit RISC Microcontroller. The ARM9 Evaluation Board will be built with the Atmel AT91SAM9260 ARM9 Microcontroller. The evaluation board would features interfaces like USB, Serial and Ethernet.

2. REQUIREMENT ANALYSIS AND DESIGN

The primary goal of this project is to develop a hardware platform primarily targeted at operating system testing. The ARM9 Evaluation Kit enables the evaluation of and code development for applications running on an AT91SAM9260 device. The Atmel AT91SAM9260 is based on the ARM926EJ-S processor, with 8K byte instruction and 8K byte data cache memories. AT91SAM9260 operates at 210 MIPS with a 190 MHz clock. Features of AT91SAM9260 include 8K bytes of SRAM and 32K bytes of ROM with single cycle access at maximum processor or bus speed, together with an external bus interface with controllers for SDRAM and static memories including NAND Flash and CompactFlash AT91SAM9260 processor's extensive peripheral set include USB Full Speed Host and Device interfaces, a 10/100 Base T Ethernet MAC, Image Sensor Interface, Multimedia Card Interface (MCI), Synchronous Serial Controllers (SSC), USARTs, Master/Slave Serial Peripheral Interfaces (SPI), a three-channel 16-bit Timer Counter (TC), a Two Wire Interface (TWI) and four-channel 10-bit ADC. The AT91SAM9260 has a fully featured system controller for efficient system management, including a reset controller, shutdown controller, clock management, advanced interrupt controller (AIC), debug unit (DBGU), periodic interval timer, watchdog timer and real-time timer. The AT91SAM9260 is available in a 217-ball LFBGA and 208 QFP RoHS-compliant packages.

The board as shown in Figure 2 is designed to provide the following interfaces

- 64 MB SDRAM
- 256 MB Of NAND Flash Memory
- 1 USB Host and 1 USB Device Port Interface
- 1 RS232 Serial communication Port
- 1 PHY Ethernet 100 base TX with three status LEDs
- 1 Data-Flash, SD/MMC Card Slot
- 1 External Bus Interface (EBI) signals routed through 96 Pin Euro Connector
- 1 Lithium Coin Cell Battery Retainer for 12mm Cell Size
- JTAG /ICE Debug Interface

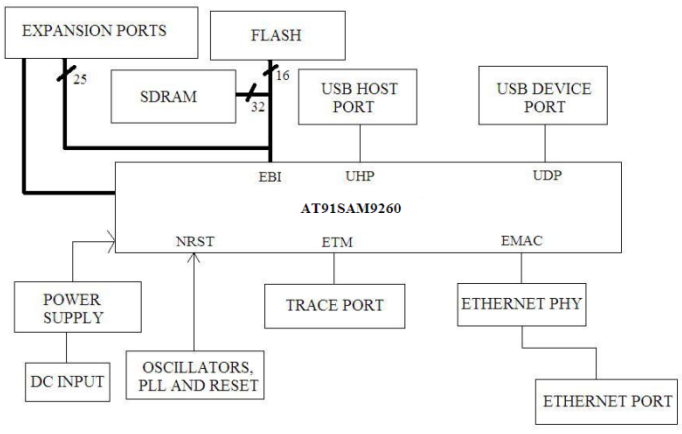

Figure 2. Evaluation Kit Block Diagram

3. SCHEMATIC DESIGN

To stay competitive in today's market, engineers must take a design from engineering through manufacturing with shorter design cycles and faster time to market. OrCAD is a suite of tools from Cadence for the design and layout of printed circuit boards (PCBs). So for the design of the schematics for our evaluation kit we used OrCAD Capture.

a. Power Supply

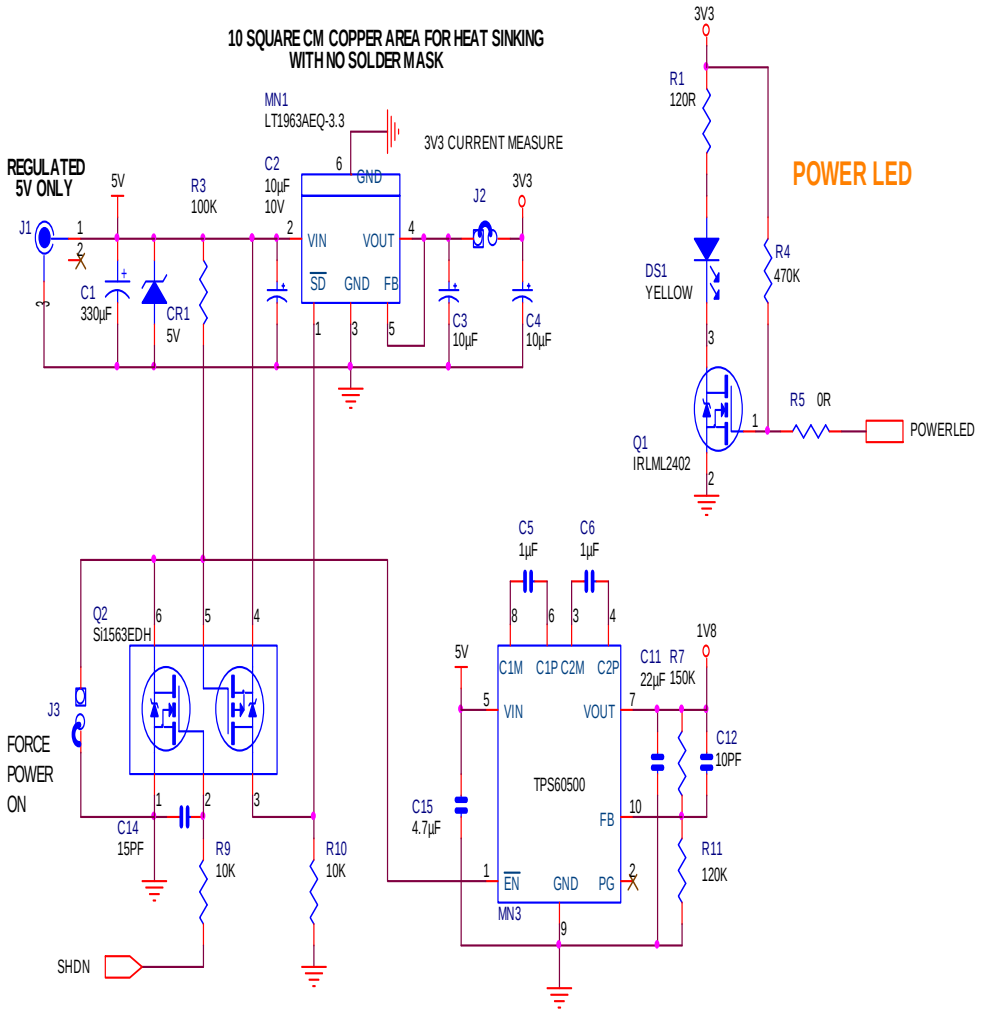

Figure 3. Power Supply Schematics

The Power Supply for the evaluation kit consists of 1.8V High Efficiency step-down charge pump regulator and 3.3V linear regulator with shutdown control as shown in Figure 3. The TPS6050x devices are a family of step-down charge pumps as in Figure 3, that generate a regulated, fixed 1.8-V. Only four small ceramic capacitors are required to build a complete high efficiency dc/dc charge pump converter. The TPS6050x charge pumps provide a regulated output voltage in the range of 1.8V from an input voltage of 5V. The devices use switched capacitor fractional conversion to achieve high efficiency over the entire input and output voltage range. Regulation is achieved by sensing the output voltage and enabling the internal switches as needed to maintain the selected output voltage. The circuits consist of an oscillator, a voltage reference, an internal resistive feedback circuit (fixed voltage version only), an error amplifier, and two charge pump stages with MOSFET switches, a shutdown/startup circuit, and a control circuit. The capacitor values are closely linked to the required output current, output noise, and ripple requirements. The input capacitor improves system efficiency by reducing the input impedance, and it also stabilizes the input current. The value of the output capacitor, Co, influences the stability of the voltage regulator. The minimum required capacitance for C11 is 10 PF. The FB pin must be connected externally with the output. For maximum output current and best performance, 4 ceramic capacitors are recommended. For lower currents or higher allowed output voltage ripple, other capacitors can also be used. Flying capacitors lower than 1 Micro-Farads can be used, but this decreases the maximum output power. This means that the device works in linear mode with lower output currents. To get an output of V0 that is 1.8V in this case we use the formula.

V0= (R7+R11)/R11 * VFB Where VFB is Voltage at the pin FB which is measured to be 0.8V. And R7 = 1.25 R2 so the calculations comes as R7 = 150K Ohms and R11= 120K0hms.

The input voltage from a single or dual NiCd, NiMH or alkaline cell is boosted to 3.3 V. This voltage is used as system supply for the application and as an input voltage for the step-down charge pump which is used to provide the core voltage for a DSP. A circuit for driving a gate of a MOS transistor to a non-conductive state, comprising: a voltage input node for receiving a positive voltage; a signal input node for receiving an ENABLE signal; and a negative voltage generator, responsive to an ENABLE signal from the signal input node to apply a negative voltage to the gate of the MOS transistor to prevent MOS transistor current conduction, wherein the negative voltage generator comprises: a capacitor having a first electrode and a second electrode; a first switching device connected between the first capacitor electrode and the input node; a second switching device connected between the second capacitor electrode and a common potential; a third switching device connected between the second capacitor electrode and the gate of the MOS transistor; a fourth switching device connected between the first capacitor electrode and a current source; and a monitoring circuit responsive to the voltage of the first capacitor electrode for controlling the first to fourth switching devices to charge the capacitor and drive the gate voltage of the MOS transistor negative.

b. MMC/SD Card Interface

The Multimedia Card Interface (MCI) supports the Multimedia Card (MMC) Specification V3.11, the SDIO Specification V1.1 and the SD Memory Card Specification V1.0. The MCI includes a command register, response registers, data registers, timeout counters and error detection logic that automatically handle the transmission of commands and, when required, the reception of the associated responses and data with a limited processor overhead.

The MCI supports stream, block and multi-block data read and write, and is compatible with the Peripheral DMA Controller (PDC) channels, minimizing processor intervention for large buffer transfers.

The MCI operates at a rate of up to Master Clock divided by 2 and supports the interfacing of 2 slot(s). Each slot may be used to interface with a Multimedia Card bus (up to 30 Cards) or with a SD Memory Card. Only one slot can be selected at a time (slots are multiplexed). A bit field in the SD Card Register performs this selection.

The SD Memory Card communication is based on a 9-pin interface (clock, command, four data and three power lines) and the Multimedia Card on a 7-pin interface (clock, command, one data, three power lines and one reserved for future use). The SD Memory Card interface also supports Multimedia Card operations. The main differences between SD and Multimedia Cards are the initialization process and the bus topology.After a power-on reset; the cards are initialized by a special message-based Multi Media Card bus protocol. Each message is represented by one of the following tokens:

- Command: A command is a token that starts an operation. A command is sent from the host either to a single card (addressed command) or to all connected cards (broadcast command). A command is transferred serially on the CMD line.
- Response: A response is a token which is sent from an addressed card or (synchronously) from all connected cards to the host as an answer to a previously received command. A response is transferred serially on the CMD line.
- Data: Data can be transferred from the card to the host or vice versa. Data is transferred via the data line.

Card addressing is implemented using a session address assigned during the initialization phase by the bus controller to all currently connected cards. Their unique CID number identifies individual cards.

There are different types of operations. Addressed operations always contain a command and a response token. In addition, some operations have a data token; the others transfer their information directly within the command or response structure. In this case, no data token is present in an operation. The bits on the DAT and the CMD lines are transferred synchronous to the clock MCI Clock.

As per the above Figure 4, AT45DB642D is used which is a 2.7-volt, dual-interface sequential access Flash memory. The AT45DB642D is enabled through the chip select pin (CS) and accessed via a three-wire interface consisting of the Serial Input (SI), Serial Output (SO), and the Serial Clock (SCK). This is initiated by the ARM9 Processor. The SO pin is used to shift data out from the device. Data on the SO pin is always clocked out on the falling edge of SCK. When the WP pin is asserted, all sectors specified for protection by the Sector Protection Register will be protected against program and erase operations regardless of whether the Enable Sector Protection command has been issued or not. The WP pin functions independently of the software controlled protection method. If a program or erase command is issued to the device while the WP pin is asserted, the device will simply ignore the command and perform no operation. The device will return to the idle state once the CS pin has been de-asserted. The Enable Sector Protection command and Sector Lockdown command, however, will be recognized by the device when the WP pin is asserted. The WP pin is internally pulled-high and may be left floating if hardware controlled protection will

not be used. The ARM9 can reset the serial flash by sending a high signal to (Reset) reset pin to reset its operations.

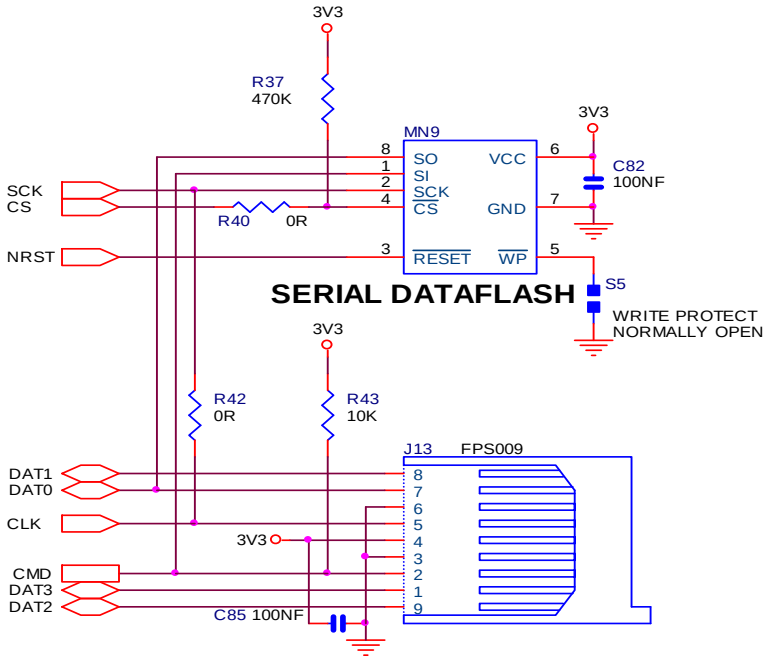

Figure 4. Schematics for MMC/SD Card Data Flash

c. Ethernet MAC Interface

The EMAC module implements a 10/100 Ethernet MAC compatible with the IEEE 802.3 standard using an address checker, statistics and control registers, receive and transmit blocks, and a DMA interface. The address checker recognizes four specific 48-bit addresses and contains a 64-bit hash register for matching multicast and unicast addresses. It can recognize the broadcast address of all ones, copy all frames, and act on an external address match signal.

The statistics register block contains registers for counting various types of event associated with transmit and receive operations. These registers, along with the status words stored in the receive buffer list, enable software to generate network management statistics compatible with IEEE 802.3.

The Ethernet MAC is the hardware implementation of the MAC sub-layer OSI reference model between the physical layer (PHY) and the logical link layer (LLC). It controls the data exchange between a host and a PHY layer according to Ethernet IEEE 802.3u data frame format. The Ethernet MAC contains the required logic and transmit and receive FIFOs for DMA management. In addition, it is interfaced through MDIO/MDC pins for PHY layer management. The Ethernet MAC can transfer data in media-independent interface (MII) or reduced media independent interface (RMII) modes depending on the pinout configuration. The major features of the EMAC are:

- Compatibility with IEEE Standard 802.3
- 10 and 100 Mbits per second data throughput capability
- Full- and half-duplex operation
- MII or RMII interface to the physical layer
- Register interface to address, status and control registers
- DMA interface
- Interrupt generation to signal receive and transmit completion
- 28-byte transmit and 28-byte receive FIFOs
- Automatic pad and CRC generation on transmitted frames
- Address checking logic to recognize four 48-bit addresses
- Supports promiscuous mode where all valid frames are copied to memory
- Supports physical layer management through MDIO interface control of alarm and update time/calendar data in.

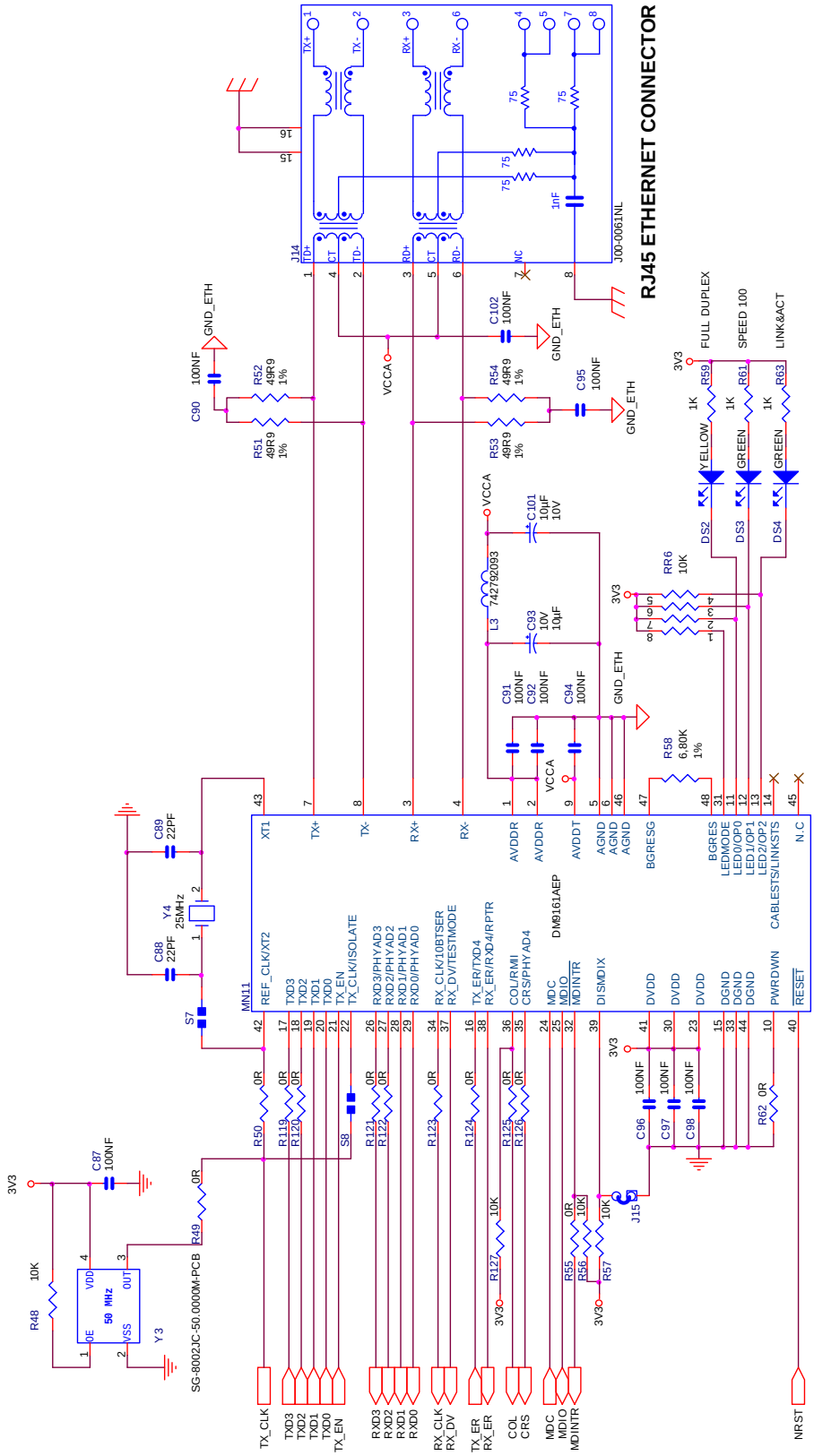

Figure 5.Schematics for Ethernet MAC

The EMAC has an interrupt line connected to the Advanced Interrupt Controller (AIC) as shown in Figure 5. Handling the EMAC interrupt requires programming the AIC before configuring the EMAC.

- The Ethernet is clocked through the Power Management Controller (PMC).

- The Ethernet has an interrupt line connected to the Advanced Interrupt Controller (AIC).
- ETXEN pin is used for Transmit Enable
- ECOL Signal Pin is used Collision Detect
- ETX0 - ETX3 pins are used for 4-bit data transmit
- ERX0 - ERX3 pins are used for 4-bit data reception
- ECRS pin is used for Carrier Sense
- Uses 2 bits for transmit (ETX0 and ETX1) and two bits for receive (ERX0 and ERX1). There is a Transmit Enable (ETXEN), a Receive Error (ERXER), a Carrier Sense (ECRS_DV), and a 50 MHz Reference Clock (ETXCK_REFCK) for 100Mb/s data rate.
- The transmit and receive bits are converted from a 4-bit parallel format to a 2-bit parallel scheme that is clocked at twice the rate. The carrier sense and data valid signals are combined into the ECRS_ECRSDV signal.

LEDs flash once per 200ms after power-on reset or software reset by writing PHY register. All LED pins are dual function pins, which can be configured as either active high or low by pulling them low or high accordingly. If the pin is pulled high, the LED is active low after reset. Likewise, if the pin is pulled low, the LED is active high.

d. USB Interface

A USB 2.0 full-speed pad is embedded and controlled by the Serial Interface Engine (SIE). The signal external_resume is optional but allows the USB Device Port **(**UDP) peripheral to wake-up once in system mode. The host will then be notified that the device asks for a resume. This optional feature must be also negotiated with the host during the enumeration. The main features of the UDP are:

- USB V2.0 Full-speed Compliant, 12 Mbits per second
- Embedded USB V2.0 Full-speed Transceiver
- Embedded Dual-port RAM for Endpoints
- Suspend/Resume Logic
- Ping-pong Mode (2 Memory Banks) for Isochronous and Bulk Endpoints

The Figure 6 shows the schematics for the USB Device Port **(**UDP) and USB Host Port (UHP). The UDP schematics is explained as following

- UDP_CNX is an input signal used to check if the host is connected
- UDP_PUP is an output signal used to enable pull-up on DP
- PD4 is an input signal pin used to check if the host is connected
- PD5 is an output signal pin used to enable pull up on DDP
- DDM : USB Device Port Data on low operating speed
- DDP : USB Device Port Data on high operating speed

A bus-powered peripheral requires a 3.3V regulator, both to power the logic and to supply the proper voltage to a USB pins. This pull-up resistor signals the host that a device is connected, and indicates the device's operating speed.

There are two communication channels between the Host Controller and the Host Controller Driver. The first channel uses a set of operational registers located on the USB Host Controller. The Host Controller is the target for all communications on this channel. The operational registers contain control, status and list pointer registers. They are mapped in the ASB memory mapped area. Within the operational register set there is a pointer to a location in the processor address space named the Host Controller Communication Area (HCCA). The HCCA is the second communication channel.

- As device connection is automatically detected by the USB host port logic, a pull-down must be connected on DP and DM on the board. Otherwise the USB host will permanently detect a device connection on this port.
- HDMA : USB Host Port A Data on a low operating speed
- HDPA USB Host Port A Data on a high operating speed
- HDMB USB Host Port B Data on a low operating speed
- HDPB USB Host Port B Data on a high operating speed

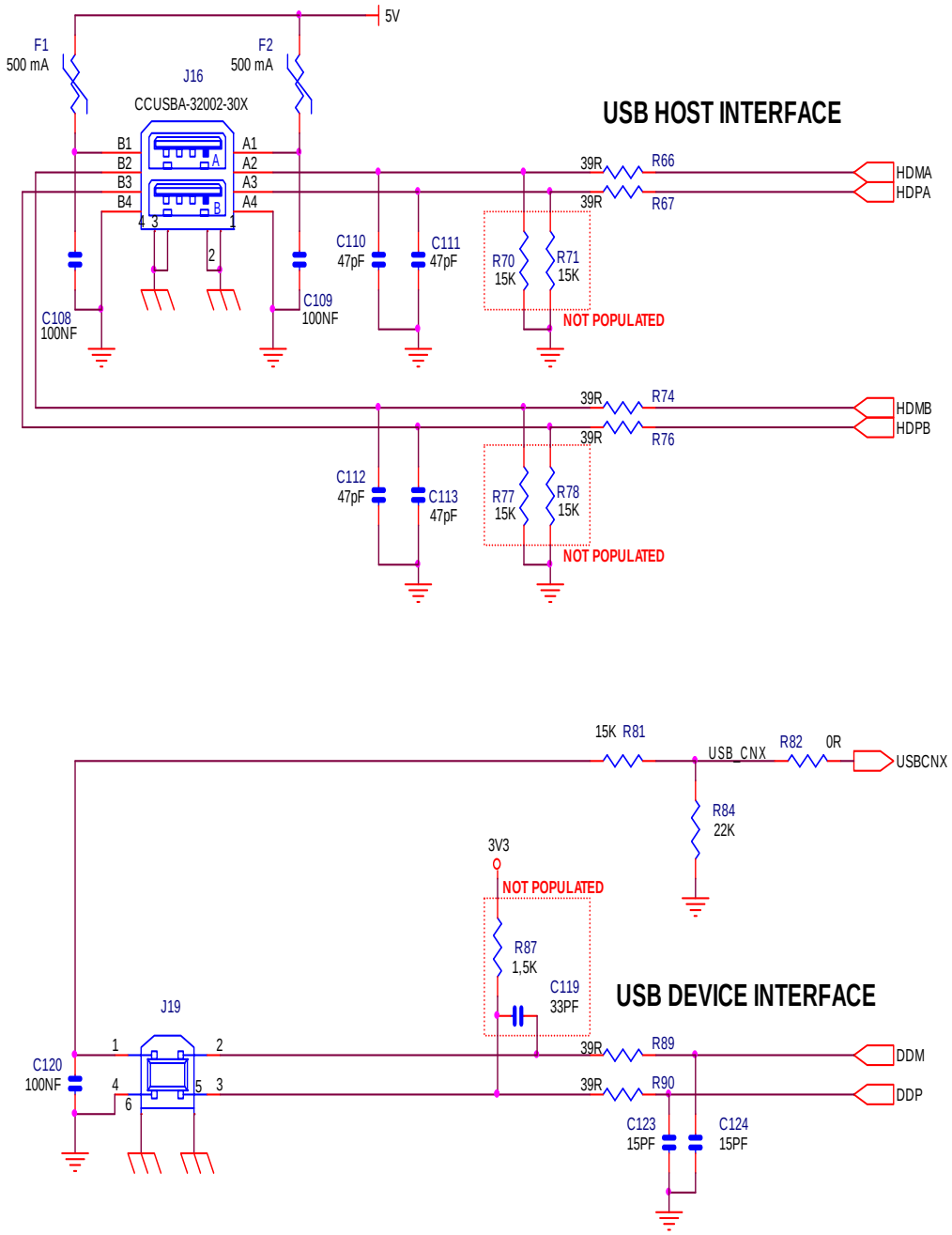

Figure 6. Schematics for USB Interface

e. Serial Interface

The Universal Synchronous Asynchronous Receiver Transmitter (USART) provides one full duplex universal synchronous asynchronous serial link. Data frame format is widely programmable (data length, parity, number of stop bits) to support a maximum of standards. The USART interrupt line is connected on one of the internal sources of the Advanced Interrupt Controller. Using the USART interrupt requires the AIC to be programmed first. Note that it is not recommended to use the USART interrupt line in edge sensitive mode. The receiver implements parity error, framing error and overrun error detection. The receiver timeout enables handling variable-length frames and the transmitter time guard facilitates communications with slow remote devices. Multi-drop communications are also supported through address bit handling in reception and transmission as shown in Figure 7.

The MAX3241E is selected as the RS-232 trans-receiver which is a +3.0V powered EIA/TIA-232 and V.28/V.24 communications interface devices feature low power consumption, high data-rate capabilities, and enhanced electrostatic-discharge (ESD) protection. A proprietary low-dropout transmitter output stage

delivers true RS-232 performance from a +3.0V to +5.5V power supply, using an internal dual charge pump. The charge pump requires only four small 0.1µF capacitors for operation from a +3.3V supply. All transmitters were driven simultaneously at 120kbps into RS- 232 loads in parallel with 1000nF. Here 3v is applied to Vcc with the bypass capacitor of 100NF.

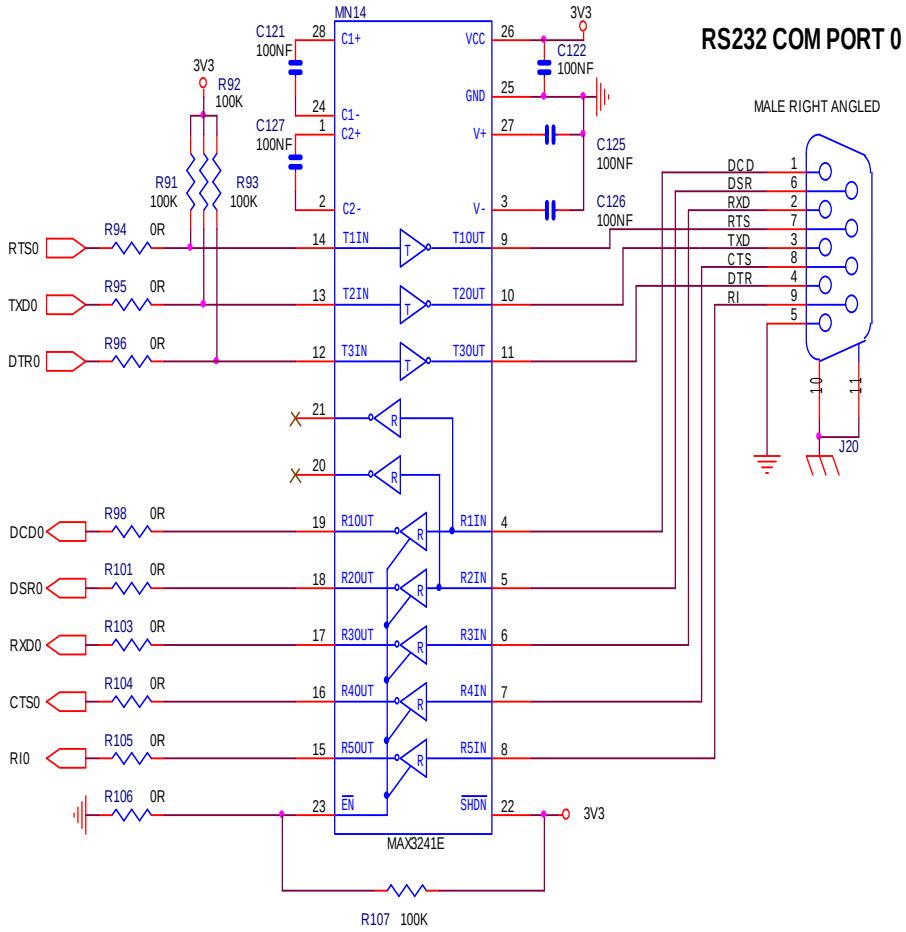

Figure 7. Schematics for RS232 Interface

f. SDRAM Interface

The AT91SAM9260 Evaluation kit has been incorporated by 64 Mbytes of SDRAM memory. There are two 256Mbits memory connected serially to form 64Mbytes of memory. The SDRAM uses the SDRAMC (SDRAM Controller) which is already present in the processor. The SDRAM Controller (SDRAMC) extends the memory capabilities of a chip by providing the interface to an external 16-bit or 32-bit SDRAM device. The page size supports ranges from 2048 to 8192 and the number of columns from 256 to 2048. It supports byte (8-bit), half-word (16-bit) and word (32-bit) accesses. The SDRAM Controller supports a read or write burst length of one location. It does not support byte Read/Write bursts or half-word write bursts. It keeps track of the active row in each bank, thus maximizing SDRAM performance, e.g., the application may be placed in one bank and data in the other banks. So as to optimize performance, it is advisable to avoid accessing different rows in the same bank. As per figure 8, MT48LC8M16A2 is selected for its s a high-speed CMOS, dynamic random access memory

- The A(0-14) is used as the address bus for specifying the address to the SDRAMs. D(0-31) is used as the data bus between the SDRAMs and the ARM9 processor. SDCS is used as chip select which selects which SDRAM needs to be enabled for data passage between the processor and the SDRAM
- SDCK pin is used to pass the clock signals to SDRAM
- SDCLK pin is used control the enabling and disabling the clock signals to the SDRAM
- RAS Pin to used as row signal

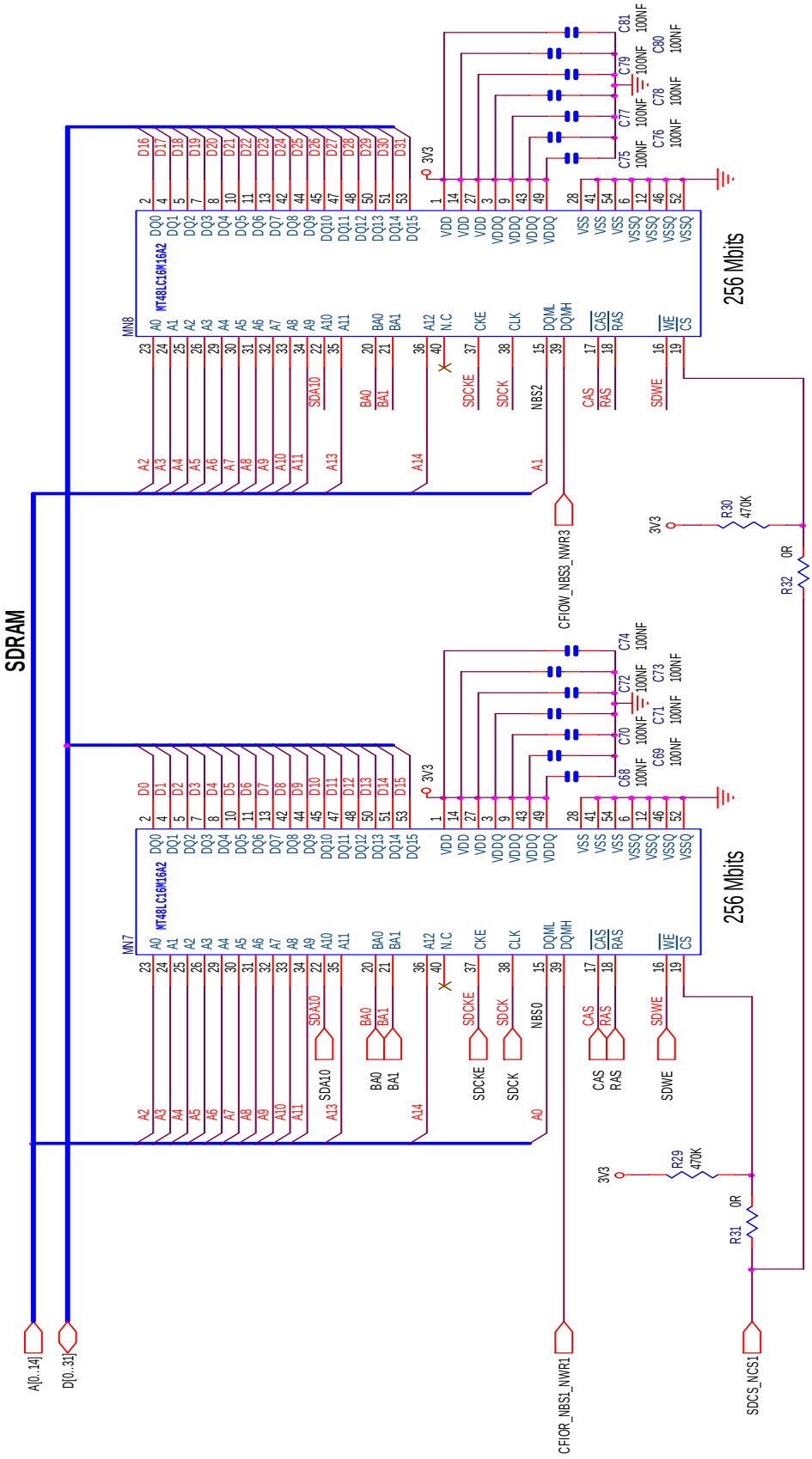

Figure 8. Schematics for SDRAM Interface

- CAS pin is used as Column signal
- SDWE pin used for SDRAM Write Enable.
- Uses four Banks of 2M x 32 bit SDRAM

g. NAND Flash Memory

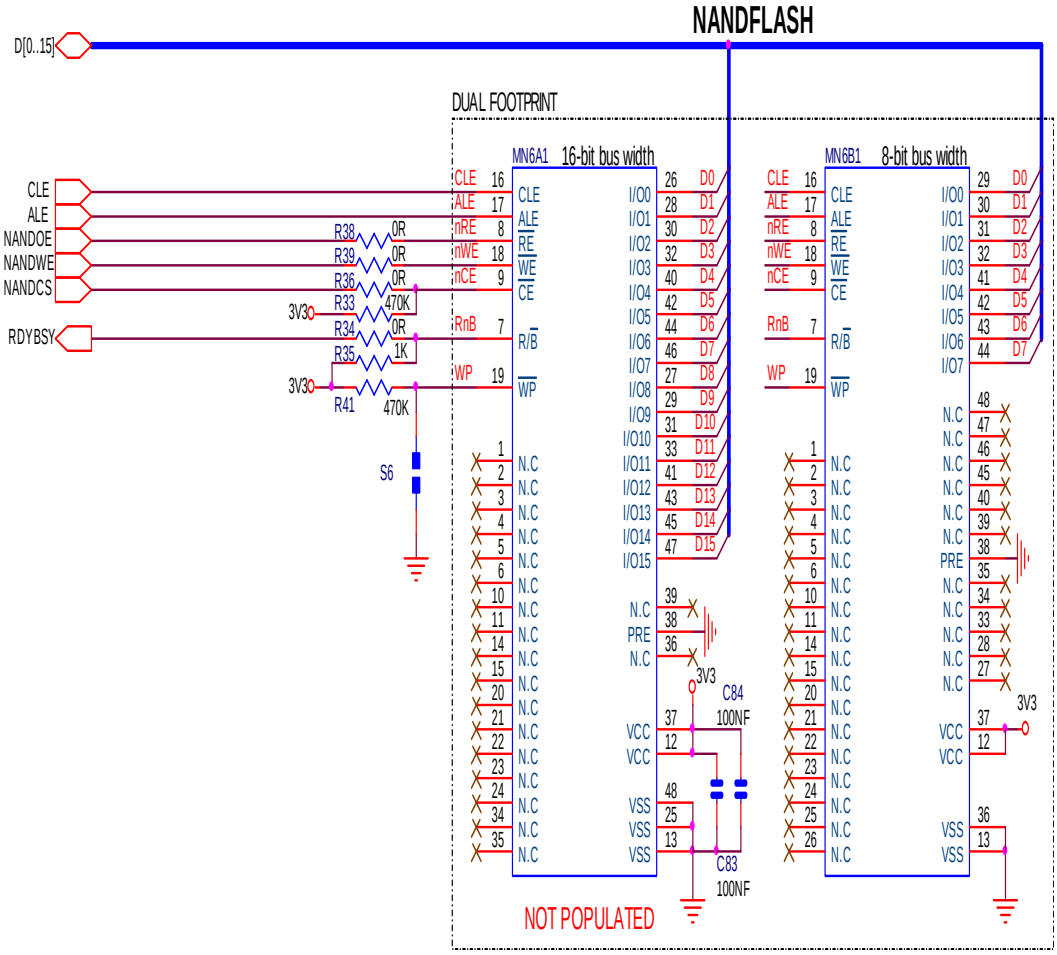

Figure 9. Schematics for NAND Flash Memory Interface

The EBI integrates circuitry that interfaces to NAND Flash devices. The NAND Flash logic is driven by the Static Memory Controller on the NCS3 address space. As per figure 9, MN6A1 is selected NAND Flash Memory. The address latch enable and command latch enable signals on the NAND Flash device are driven by address bits A22 and A21 of the EBI address bus. The user should note that any bit on the EBI address bus can also be used for this purpose. The command, address or data words on the data bus of the NAND Flash device are distinguished by using their address within the NCS3 address space. The chip enable (CE) signal of the device and the ready/busy (R/B) signals are connected to PIO lines. The CE signal then remains asserted even when NCS3 is not selected, preventing the device from returning to standby mode. Some functional limitation with the supported burst Flash device will occur when the NAND Flash device is activated due to the fact that the SMOE and SMWE signals are multiplexed with BFRDY and BFBAA signals respectively.

- D(0-15) is being used as Data bus to MN6A1 and MN6B1
- The chip enable (CE) signal of the device and the ready/busy (R/B) signals are connected to PIO lines
- NANDOE is used to enable the ARM9 Processor to read the data from NAND Memory
- NANDOW is used for writing the data on to the memory
- NANDCS is used for selecting the memory to which ARM9 wants to communicate with.
- Bypass capacitance of 100nf is connected to the power source along with a supply voltage of 3Volts

4. TESTING AND SIMULATION OF EVALUATION KIT

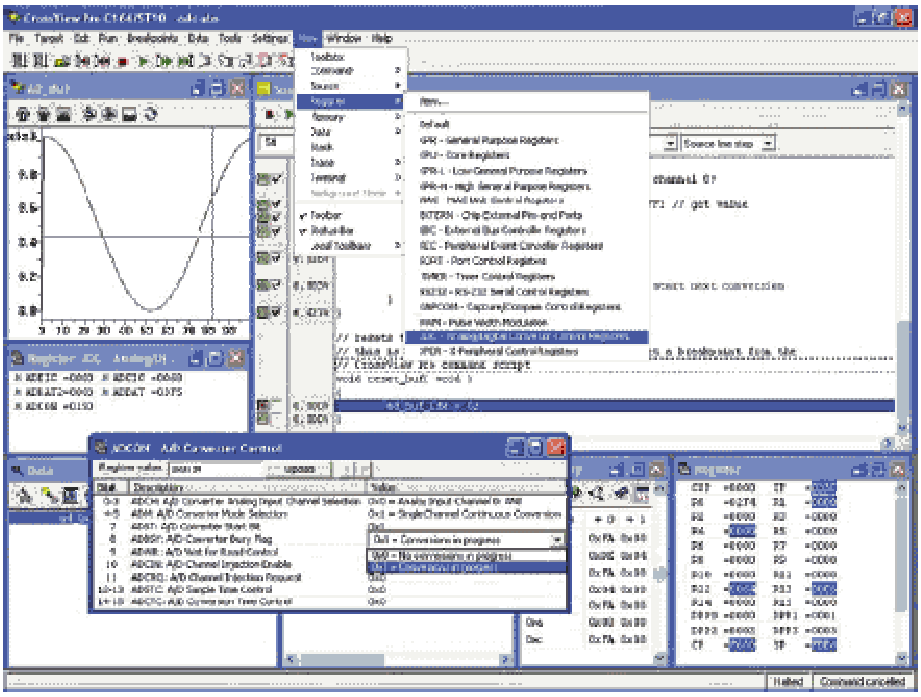

Figure 10. Pspice Cross View Simulator

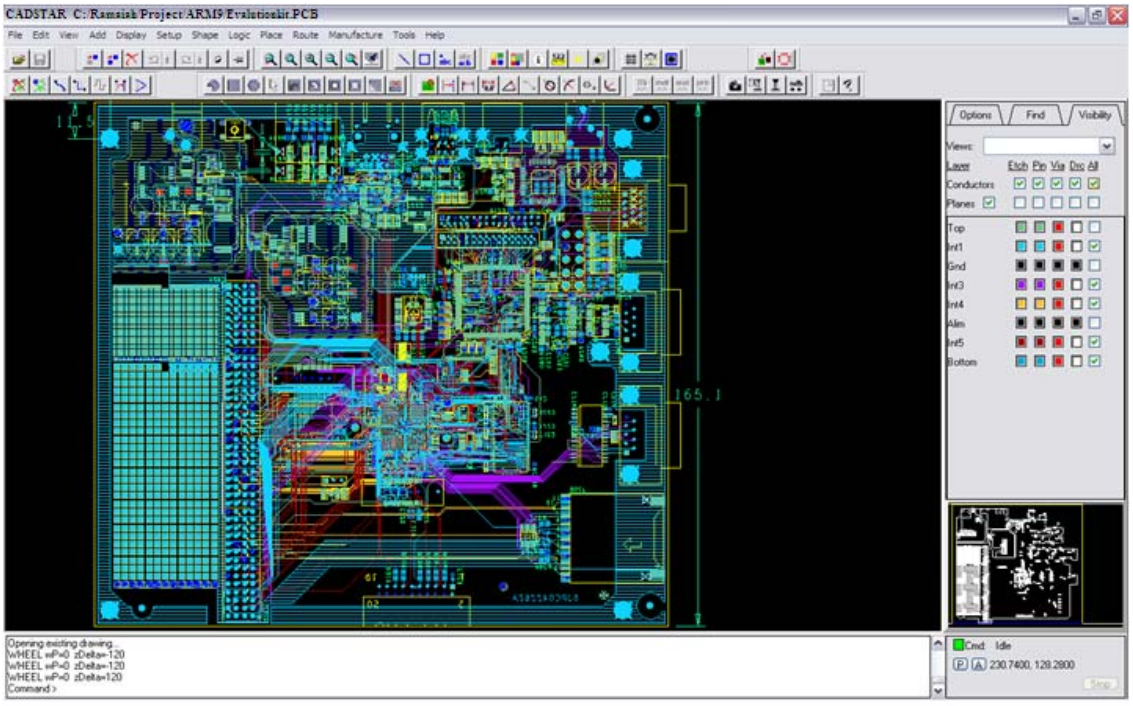

Figure 11. PCB layout and Routing

The circuit was simulated and tested using Pspice Cross View simulator as shown in Figure 10. The Input voltages with the basic circuit design needs to be provided to tool and then it would calculate the output voltage and current which is then verified. However due to complexity of the few schematics it could not be

tested on this tool. For few simple circuits it was tested on a general purpose board. CADSTAR is Zuken's powerful PCB design solution allowing an intuitive work flow, guiding the designers easily through their design process. CADSTAR incorporates all the technologies necessary for a complete electronic development process in one environment. The PCB Layout for our Evaluation kit is also made from CADSTAR as shown in Figure 11. Due to signal integrity and the schematics complexity of an 8 layer PCB board is designed

5. CONCLUSION

The evaluation kit enables the evaluation of and code development for applications running on an AT91SAM9260 device. The Evaluation kit has been designed by AT91SAM9260 PQFP208 package which uses pin grid array.

- There was a difficulty in selecting the right kind of ARM9 processors. During the initial design the AT91RM9200 processor which was later changed due to unavailability and complications of Board Design.
- The schematics was designed using ORCAD and finding the database for the ARM9 processor was difficult and needed to be downloaded and added to the ORCAD Library.
- The power supply needed to be redesigned as initial design did not fulfill all the signal integrity issues.
- The Designed evaluation kit requires 5V DC (±5%). DC power is supplied to the board via the 2.1 mm by 5.5 mm. The user has the possibility to plug a battery (3V Lithium Battery CR1225 or equivalent) in order to permanently power the backup part of the device.

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