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New Schmitt Trigger with Controllable Hysteresis using Dual Control Gate-Floating Gate Transistor (DCG-FGT)

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ABSTRACT

This paper presents different low voltage adjustable CMOS Schmitt trigger using DCG-FGT transistor. Simple circuits are introduced to provide flexibility to program the hysteresic threshold in this paper. The hysteresis can be controlled accurately at a large voltage range. The proposed Schmitt trigger have been designed using 90nm 1.2V CMOS technology and simulated using Eldo with PSP device models. The simulation results show rail-to-rail operation and adjustable switching voltages V_{TH-} (low switching voltage) and V_{TH+} (high switching voltage).

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1. INTRODUCTION

Schmitt triggers are basic circuits that convert a varying voltage into a stable signal (V_{DD} or Gnd). They have been used extensively to improve on/off control, and reduce the sensitivity to noises and disturbances. The Schmitt trigger is used in buffer [1], sub-threshold SRAM [2], sensors [3], [4] and pulse width modulation circuits [5].

The main difference between Schmitt triggers and comparators lies in the DC transfer characteristics. The comparator shows only one switching threshold, while Schmitt trigger shows different switching thresholds for positive-going and negative-going input signals. This characteristic is called hysteresis. If the noise magnitude of the input signal is lower than the switching threshold difference, Schmitt trigger will not respond, thus making Schmitt trigger immune to the undesired noise.

These blocks find their way into many instrumentation and test measurement systems. The demand for implementation of controllable hysteresis Schmitt triggers has increased in such systems. However, most of the previous proposed hysteretic comparators do not provide the flexibility to program the hysteretic threshold after the circuit design is completed [6]-[8]. But, it might be not effective since measurement environment may vary. To solve this problem, Very Low voltage Schmitt triggers based on CMOS inverter were proposed [9], [10]. The structure proposed in [9] uses body biasing technique to achieve different switching thresholds for positive going and negative-going input signals, while two static inverters with distinct threshold voltages were employed in [10]. We propose to solve this problem with coupled inverter based on DCG-FGT transistor.

2. The Dual Control Gate Floating Gate Transistor concept

Figure 1 presents DCG-FGT architecture, as proposed by Regnier*et al.*in previous work [11].This paper focuses on the threshold voltage adjustable mode, where the DCG-FGT behaves like a MOS transistor with an electrically adjustable threshold voltage **(**V_{TH}).

(a) (b)

Figure 1. (a) DCG-FGT architecture, (b) Cross section view of a DCG-FGT

The DCG-FGT transistor threshold voltage V_{TH} can be controlled electrically by applying static bias on one of the gate (G1 or G2). By applying Gauss's law on the floating gate, we demonstrated that V_{TH} is given by [12]:

$$V_{TH} = V_{TH0} - V_{G2} \cdot \frac{L_{G2}}{L_{G1}}$$

Where V_{TH0} is the threshold voltage of the DCG-FGT transistor for V_{G2}=0V, L_{G1} and L_{G2} are respectively the lengths of the gate G1 and gate G2. The threshold voltage variation clearly depends on the gate G2 bias voltage (V_{G2}) and the gate length ratio. Figure 2 shows a good correlation between simulated and measured values of the threshold voltage V_{TH} versusV_{G2}, for various sizes of DGC-FGT transistor.

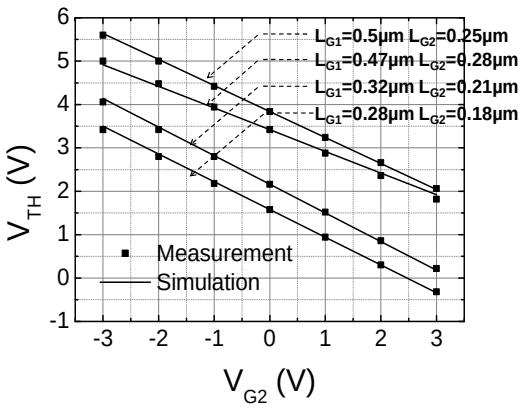

Figure 2. Measured and calculated threshold voltage values versus V_{G2} for different length ratio configurations

Charge neutrality approach coupled with the PSP formulation [13] has been used for the DCG-FGT electrical modeling. In this approach, the charge neutrality, including the charge stored in the floating-gate, is applied to determine the floating gate potential from which all the variables can be computed in the PSP model formulation. The electrical equivalent circuit of DCG-FGT transistor is shown in Figure 3.

The model is running under electrical simulator (ELDO) and is characterized through ICCAP software. It has been validated on 90nm FLASH technology from STMicroelectronics. An accurate and scalable model is available in design framework [14]. The DCG-FGT transistor has been implemented on a FLASH technology to get a uniform tunnel oxide (removal of thick oxide).

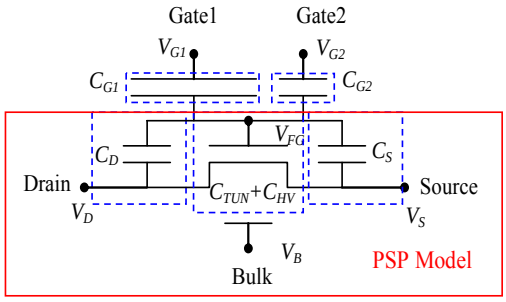

Figure 3. Electrical equivalent circuit of DCG-FGT transistor.

3. Traditionnal Schmitt Trigger

The Figure 4 presents three traditional electric scheme of Schmitt trigger, in the scheme Figure 4(a) the positive feedback is introduce by transistor bulk voltage, this voltage alters the transistor threshold voltage and so forming a hysteresis [15]. In the scheme Figure 4(b) the contention between the strong inverter (M1-M2) and the weak inverter (M3-M4) on node X constitutes the basic operating principle of that Schmitt Trigger [16].

In scheme Figure 4(c) the P3 and N3 transistor are the positive feedback. P3 and N3 modify the inverter current and the inverter threshold, creating a hysteresis [17].

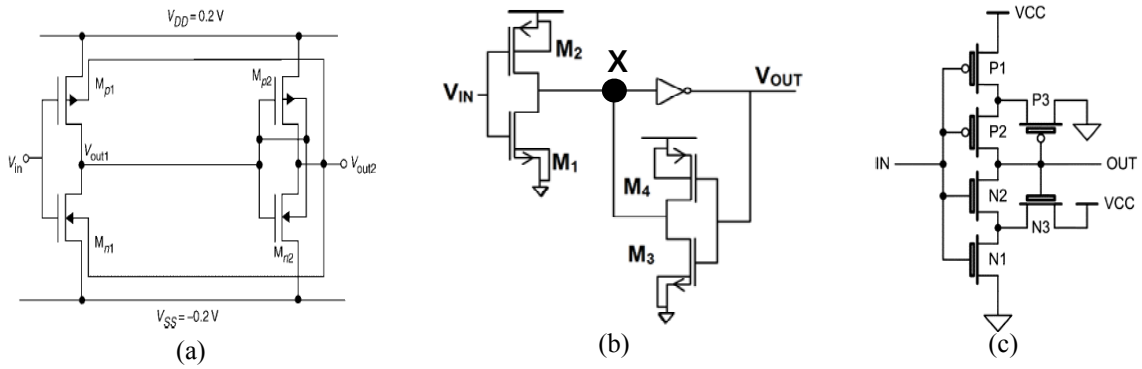

Figure 4. Traditional electric scheme of Schmitt trigger.

The characteristic of Schmitt trigger is illustrated Figure 5. If the input voltage increase, the threshold voltage of comparator is high threshold voltage V_{TH+} and if the input voltage decrease, the threshold voltage of comparator is low threshold voltage V_{TH-}. We define the offset and the window of hysteresis:

$$offset = \frac{V_{TH+} + V_{TH-}}{2} \qquad window = V_{TH+} - V_{TH-}$$

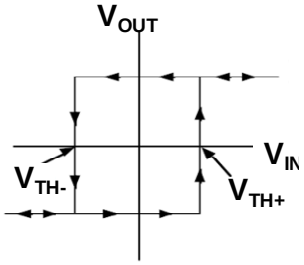

Figure 5. Characteristic of Traditional electric scheme of Schmitt trigger.

4. Adjustable Schmitt trigger based on DCG-FGT transistor

New Schmitt trigger designs are shown in the Figure 3. The circuit Figure 3(a) consists of two CMOS inverters and the positive feedback is realized with one DCG-CGT transistor and the hysteresis is controlled by the gate 2 of DCG-FGT transistor.

The circuit Figure 3(b) is composed of two CMOS inverters stages, where NMOS are replaced by DCG-FGT. The positive feedback is introduced by the DCG-FGT composed the first inverter and the hysteresis is ordered by the DCG-FGT transistor composed the second inverter.

The circuit architecture Figure 3(c) is designed with three inverters stages, where NMOS are replaced by DCG-FGT. The output of the first inverter is connected to the output of second inverter and the input of the third inverter. The feedback loop connects, the gate G2(0) of first DCG-FGT transistor, the input of the second inverter and the output of the third inverter to create the hysteresis. The inputs G2(1) and G2(2) is shorted and allow to control respectively the switching voltage of inverter 2 and 3. DCG-FGT is employed to speed up the switching process, and to control the feedback level.

The electric scheme Figure 3(d) is the same that the circuit Figure 3.c with the gate G2(1) and G2(2) is disconnected. We have two electrical controls on the hysteresis.

To verify these circuits (Figure 3) functionality, simulations are performed under Eldo with 1.2V of supply voltage. A triangular signal is applied in the input, the output is simulated. The switching threshold voltages can be extracted from the crossing points between the input signal and output signal. According the characteristic Figure 7(a), with the electric scheme Figure 6(c), the hysteresis offset can be controlled by the gate 2 voltage. In the Figure 7(b), only the low threshold voltage VTH- can be ordered with the gate 2 bias voltage. The hysteresis window (Figure 7(c)) can be driving with the gate 2 polarization of circuit Figure 6(c).

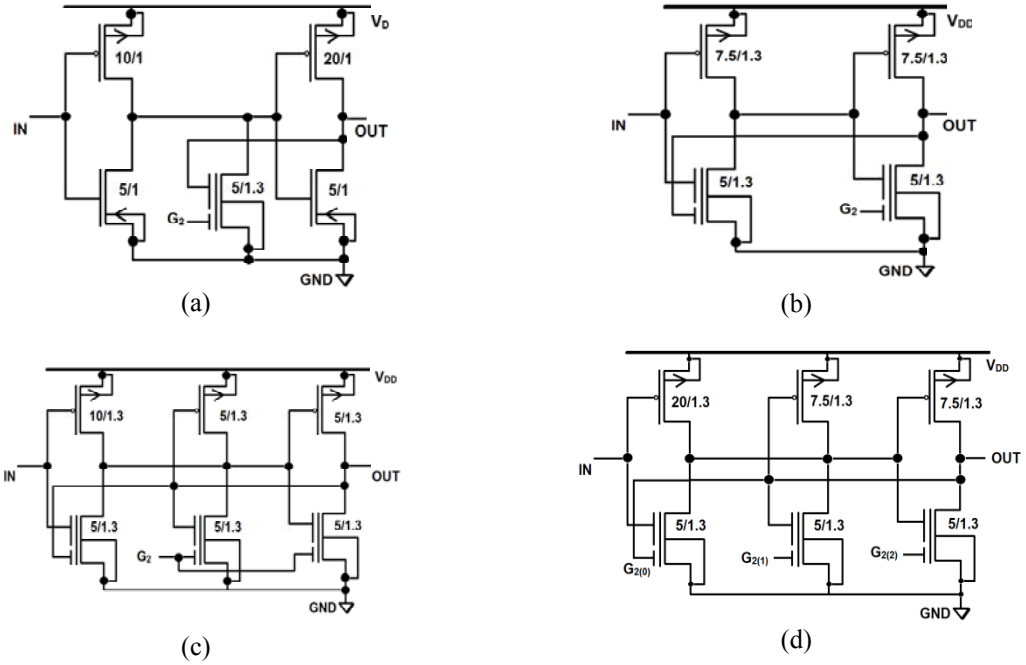

Figure 6. Electrical Scheme of Schmitt Trigger based on DCG-FGT.

In the Figure 7(d) and Figure 7(e), the switching threshold voltages of the Schmitt trigger proposed Figure 6(d) can be independently adjusted. Indeed, the V_{TH-} depends only on $G_{2(1)}$ biasing, whereas V_{TH+} depends only on $G_{2(2)}$ biasing.

Figure 7(d) and (e) show the switching threshold voltage versus $V_{G2(1)}$ and the switching threshold voltage versus $V_{G2(1)}$, respectively. The switching threshold voltages V_{TH-} and V_{TH+} can be adjusted from 0.10V to 0.46V and from 0.67V to 1.1V, which is approximately 30 % of the supply voltage.

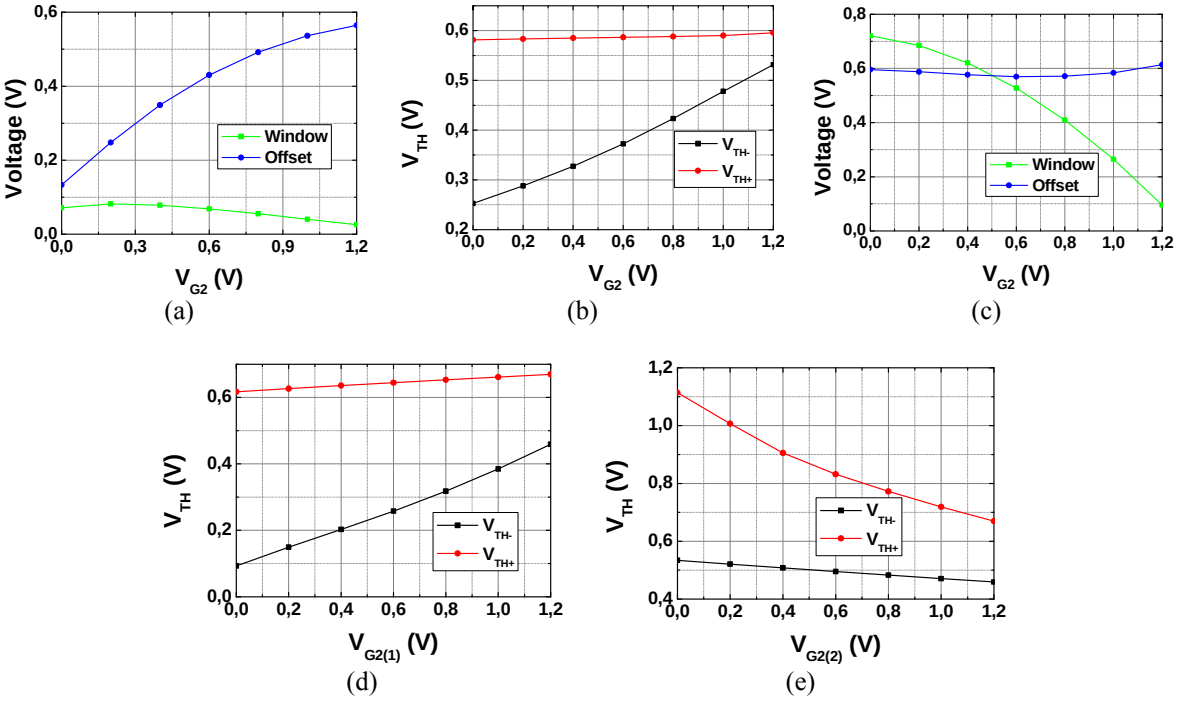

Figure 7. Simulations of the Schmitt triggers based on DCG-FGT transistor

5. Conclusion

New adjustable Schmitt trigger circuits using DCG-FGT transistor are presented. These circuits allow controlling different parameter of hysteresis like offset, window, low and high threshold voltage. The last circuit consists of three stage inverters, where NMOS transistor are replaced by DCG-FGT. Independent tuning of switching thresholds can be obtained by controlling the gate (G2) potential of the DCG-FGT transistors of the two last stages. Simulation results demonstrate that the circuit can operate at 1.2V and the switching threshold voltages can be independently adjustable of 30 % of the supply voltage by setting $V_{G2}(1)$ and $V_{G2}(2)$.

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